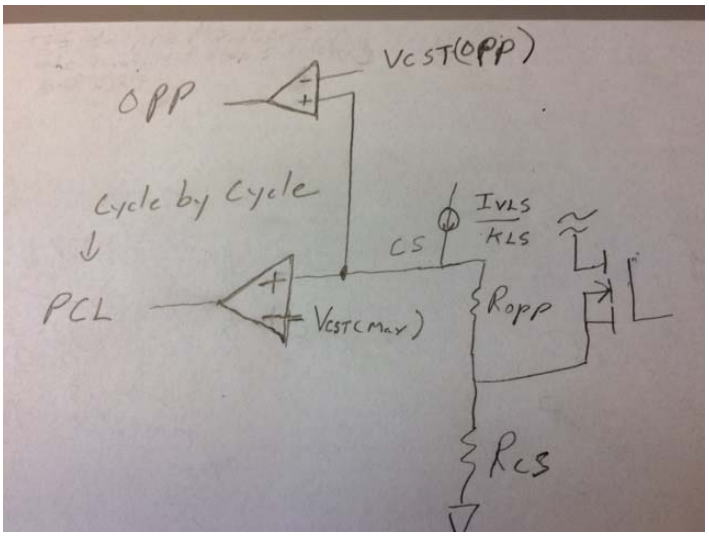
Hello Eleven,

This is a good question and I had to track to down the systems engineer who defined the device for clarification on how these functions worked.

Think of the peak current limit (PCL) comparator and the over power protection comparator being sensed off the CS pin. The PCL is a cycle by cycle current limit that is required for peak current mode control. The OPP if tripped longer than 160 ms will cause the device to stop switching and VDD UVLO cycle between $V_{VDD(OFF)}$ and $V_{VVD(ON)}$. Please refer to figure 1 and 35 below for details.



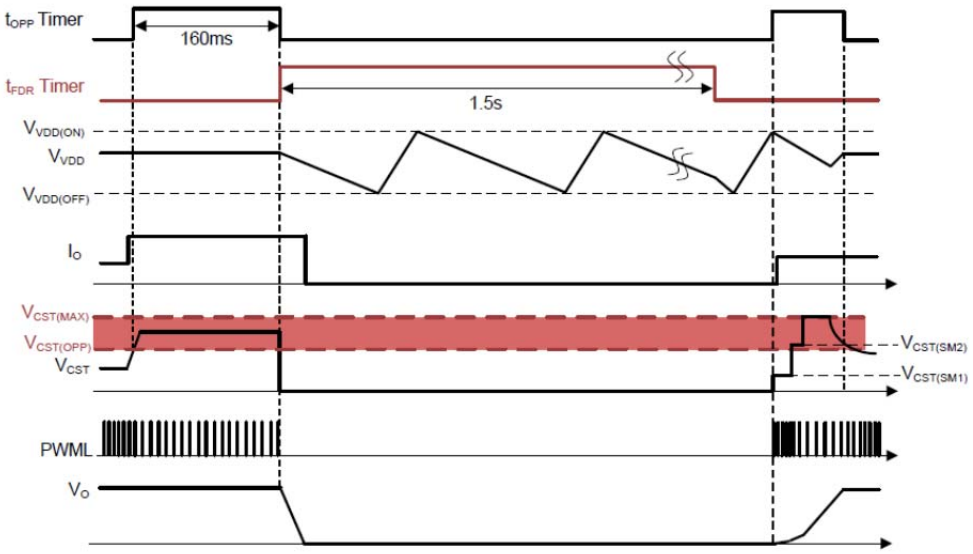


Figure 35. Timing Diagram of OPP

The data sheet for this device recommends selecting the current sense resistor (R_{CS}) set the over power protection at 0.6V and the minimum bulk voltage ($V_{BULK(MIN)}$).

The highest threshold of OPP curve ($V_{CST(OPP1)}$) of 0.6 V helps to determine R_{CS} value at $V_{BULK(MIN)}$.

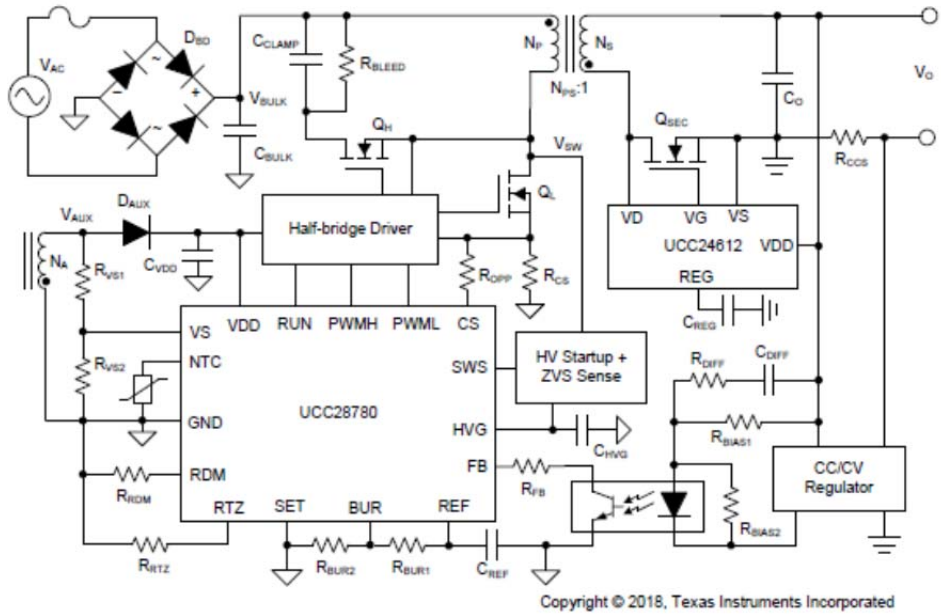
$$R_{CS} = \frac{V_{CST(OPP1)}}{\frac{P_{O(OPP)}}{V_{BULK(MIN)}\eta}\frac{2}{D_{MAX}} - \frac{V_{BULK(MIN)}t_{D(CST)}}{L_M}}$$

If the design is done this way during a large signal transient the converter will deliver ($V_{CST(max)}/V_{CST(OPP)}$)X100% more power. At the minimum bulk voltage the converter should be able to deliver 120% more power for 160ms. Please note that $V_{CST(OPP)}$ moves with the bulk voltage. The bulk voltage is sense when the main FET is on.

I_{VSL} = Vbulk*(Ns/Np)(1/R_{VS1})

$V_{CST(OPP)}$	Over-power threshold on CS pin	I_{VSL} = 0 µA	574	600	627	mV
		I_{VSL} = -333 µA	492	545	595	
		I_{VSL} = -666 µA	426	460	492	
		I_{VSL} = -1.25 mA	405	425	452	
K_{OPP}	OPP threshold voltage ratio	$V_{CST(OPP)}$ ratio between I_{VSL} = 0 µA and I_{VSL} = -1.25 mA	1.36	1.4	1.44	V/V

Simplified Schematic



I hope this helps,

Mike