EyeQ4 SoC Digital 1.0V Core Power Rail

Power Integrity and Thermal Design Guidelines

Application Notes

Revision History

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Table of Contents

1. Introduction 5
- **1.1** Acronyms and Terminology 5
- **1.2** Related Documents 5
- **1.3** Roles 6

2. EyeQ4 Digital Core and DDR Rails Specification 7
- **2.1** Digital Core Power Rail Requirements 7
  - 2.1.1 PCB PDN Simulation—Digital Core S-Parameter Model 7
- **2.2** DDR 1.1v Power Rail Requirements 8

3. Thermal Considerations 9
- **3.1** System Thermal Model 9
- **3.2** EyeQ4 Thermal Model 9
- **3.3** System Thermal Resistance 9
- **3.4** EyeQ4 Mission Profile 9
- **3.5** Utilizing EyeQ4H Full Capabilities 10
- **3.6** Difference Between Max Current Spec and Max Thermal Spec 10

4. Pre-PCB Simulations 11
- **4.1** Thermal Simulation 11
- **4.2** Power Integrity Simulation 11

5. Board Bring-up 12
- **5.1** Validating Digital Core Power Rail Performance 12
  - 5.1.1 Measurement Setup 12
  - 5.1.2 Measurement Method 12
- **5.2** Validating Product Thermal Performance 12
  - 5.2.1 Measurement Setup 12
  - 5.2.2 Measurement Method 13

Appendix A Digital Core Power Rail Test Software 14

List of Figures

Figure 1: Parameter File Ports 8

List of Tables

Table 1: Acronyms and Terminology 5

Table 2: Related Documents 5

Table 3: Roles 6

Table 4: EyeQ4H Requirements 7

Table 5: EyeQ4M Requirements 7

Table 6: EyeQ4H DDR 1.1v Requirements 8

Table 7: EyeQ4M DDR 1.1v Requirements 8

Table 8: EyeQ4H/M 1V, 1.1v, 1.8v, and 3.3V Power Rails TDP 9

Table 9: EyeQ4 Mission Profile 10

1. Introduction

This document introduces key EyeQ4 digital 1.0V core rail specification concepts and thermal considerations, including the EyeQ4 digital core rail specification and guidance for PCB bring-up measurements.

1.1 Acronyms and Terminology

The following terms and abbreviations are defined either by Mobileye or industrial convention.

Table 1: Acronyms and Terminology

Term	Definition
DDR	Double Data Rate
PDN	Power delivery network
PMA	Programmable Macro Array CMMI, ISO, SPICE
TDP	Thermal design power
VMP	Vector Microcode Processor - EyeQ vector processing unit [

1.2 Related Documents

The table below lists resources of information that are relevant to the current document.

Table 2: Related Documents

f	Name	Location
1	EyeQ4 Datasheet	https://mobileye.sharepoint.com/EyeQ4/EyeQ4-SoC/EyeQ4_DataSheet_noTRK.pdf
2	EyeQ4 System Thermal Application Note	https://mobileye.sharepoint.com/EyeQ4/Application%20Notes/EyeQ4_System_Thermal_AppNote.pdf
3	EyeQ4 Bring UP – Workflow Specification	https://mobileye.sharepoint.com/EyeQ4/BringUp/EyeQ4_BringUp_WORKFLOW.pdf
4	EyeQ4H Cut-2 S-Parameter Model	https://mobileye.sharepoint.com/EyeQ4/EyeQ4-SoC/EyeQ4H/Core%20Voltage%20S_Parameter
5	EyeQ4H FloMCAD Bridge Thermal Model	https://mobileye.sharepoint.com/EyeQ4/EyeQ4-SoC/EyeQ4H/fcTEBGA23x23_6L_EyeQ4.sat
6	EyeQ4M FloMCAD Bridge Thermal Model	https://mobileye.sharepoint.com/EyeQ4/EyeQ4-SoC/EyeQ4M/fcTEBGA23x23_EyeQ4mid_pkg.zip

1.3 Roles

Table 3: Roles

Name	Responsibilities
Technology Expert(s)	
Technology Manager	

2. EyeQ4 Digital Core and DDR Rails Specification

2.1 Digital Core Power Rail Requirements

The tables below presents the digital 1V core power rail requirements for the EyeQ4H and EyeQ4M.

Table 4: EyeQ4H Requirements

Parameter	Max Value
Voltage* under all operating conditions including load transient, temperature, DC accuracy and IR drop	1V ±3%
TDP	See Table 8
Continuous current	12A
Current change transient	8A
Current change rate	8A/us

Table 5: EyeQ4M Requirements

Parameter	Max Value
Voltage* under all operating conditions including load transient, temperature, DC accuracy and IR drop	1V ±3%
TDP	See Table 8
Continuous current	7.5A
Current change transient	6A
Current change rate	6A/us

*The voltage is specified on the BGA balls.

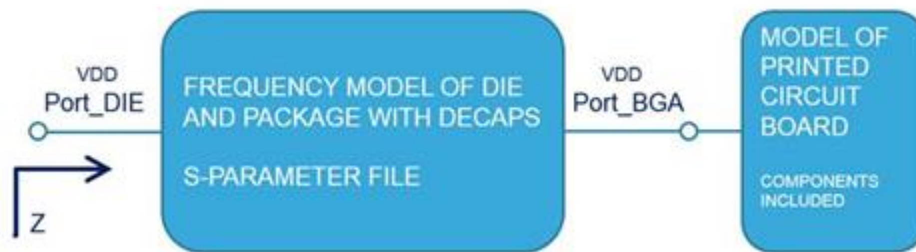
2.1.1 PCB PDN Simulation—Digital Core S-Parameter Model

A two-port S-parameter file for EyeQ4H cut-2 enables simulating the digital core package and die capacitance and the inductance effect on the PCB PDN. This file is available on SharePoint.

The two ports of the S-parameter file are:

- Port_BGA on the package ball side
- Port_DIE on the die side

Figure 1: Parameter File Ports



2.2 DDR 1.1v Power Rail Requirements

The tables below presents the requirement for the DDR 1.1v power rail:

Table 6 for EyeQ4 High with two DDRs connected at a frequency of 2400Mb/s, and,

Table 7 for EyeQ4 Mid with one DDR connected at a frequency of 2400Mb/s.

Table 6: EyeQ4H DDR 1.1v Requirements

Parameter	Max Value
Voltage range* under all operating conditions including load transient, temperature, DC accuracy and IR drop	1.06v to 1.17v
TDP	See Table 8
Continuous current	3A
Current change transient	1.5A
Current change rate	300mA/us

Table 7: EyeQ4M DDR 1.1v Requirements

Parameter	Max Value
Voltage range* under all operating conditions including load transient, temperature, DC accuracy and IR drop	1.06v to 1.17v
TDP	See Table 8
Continuous current	2A
Current change transient	1A
Current change rate	200mA/us

*The voltage is specified on the BGA balls.

3. Thermal Considerations

3.1 System Thermal Model

When constructing the system-level thermal model all internal and external heat sources should be included. It is not sufficient to use a single resistor model to represent the entire system, or even the entire board.

Examples of internal heat sources: DCDC converters, MCU, and EyeQ4.

Examples for external heat sources: sun radiation, air conditioner, nearby systems.

Refer to the "EyeQ4 System Thermal Application Note" for information about the thermal architecture of a typical EyeQ4 system.

3.2 EyeQ4 Thermal Model

For an accurate thermal model it is recommended to include the EyeQ4 1V, 1.1V, 1.8V, and 3.3V power rails TDPs. See the table below.

Table 8: EyeQ4H/M 1V, 1.1v, 1.8v, and 3.3V Power Rails TDP

	TOTAL**	1V*	1.1V	1.8V	3.3V
EyeQ4H	10W	8.5W	1W	0.25W	0.25W
EyeQ4M	5.26W	4.5W	0.5W	0.13W	0.13W

*Includes leakage current at T_J=125^{0}C of 1.2W for EQ4M and 2W for EQ4H.

**Utilizing EyeQ4H/M full capabilities; includes the EyeQ4 I/Os 3.3V/1.8V/1.1V/1V at worst case condition of T_J=125^{0}C.

Table 6 represents the full utilization of EyeQ capabilities. In other use cases, where not all of EyeQ's capabilities and functionalities are required, the power envelope may be different.

Specific use case power dissipation for EyeQ4H using a single DDR and a single 1.7MP image sensor—total TDP is 5.5W (rather than 10W).

Specific use case power dissipation for EyeQ4M using a single 1.7MP image sensor—total TDP is 4.5W (rather than 5.26W).

For thermal simulations, FloMCAD Bridge thermal models for EyeQ4H and EyeQ4M are available on SharePoint.

3.3 System Thermal Resistance

When calculating the system thermal resistance it is important to include all elements in the heat path. Common examples are thermal pads, heat sinks, metal housing, and plastic covers.

3.4 EyeQ4 Mission Profile

To ensure the longevity of the product, you should take into consideration the EyeQ4 mission profile as early as possible in the design stage. See the table below.

Table 9: EyeQ4 Mission Profile

Lifetime (yrs)	15
Power on time (hrs)	8000
Total km during life (km)	150000

Tj (°C)	Distribution	Operative hrs
-32	6%	480
45	20%	1600
70	65%	5200
120	8%	640
125	1%	80
Total (hrs)		8000

3.5 Utilizing EyeQ4H Full Capabilities

To utilize the full capabilities of EyeQ4H, the system should be designed as a two box solution: one box (including the sensors) to be mounted on the windshield; and a second box (including the EyeQ4H SoC) to be placed in a cool vehicle area. The EyeQ4H should not be placed on the windshield due to its TDP.

3.6 Difference Between Max Current Spec and Max Thermal Spec

The EyeQ4 max current spec detailed in Table 4 and Table 5 represents the maximum instantaneous current draw from the power supply. To prevent the rail voltage from collapsing at high current draws, the power supply selected for the EyeQ4 should be rated to at least the maximum instantaneous current draw of the specific rail.

The EyeQ4 max thermal spec detailed in Table 7 represents the average EyeQ4 power dissipation over a period of a few seconds.

4. Pre-PCB Simulations

At the end of the layout process, and before PCB sign-off, it is recommended to run thermal and power integrity simulations.

4.1 Thermal Simulation

The thermal simulations should include all internal and external heat sources and all elements in the thermal resistance path.

4.2 Power Integrity Simulation

The power integrity simulation should include the digital core power supply DC accuracy, components tolerance, load transient response, and IR drop under all temperature conditions.

5. Board Bring-up

For EyeQ4 Bring-up customer board basic verification (section 4.6 in "EyeQ4_BringUp_WORKFLOW)", special software is provided to validate:

- Thermal performance of the product under stress conditions
- That the digital core power rail is within specifications

The special test software generates the maximum digital core power rail current transient (continuously switching from a low current level to a high current level and back), while dissipating 8.5W for EyeQ4H and 4.5W for EyeQ4M. See Appendix AAppendix A for a more detailed description of the test.

5.1 Validating Digital Core Power Rail Performance

5.1.1 Measurement Setup

To accurately measure the digital core power rail voltage, it is recommended to use a dedicated power rail probe connected to the EyeQ4 VDD and GND ball with as low as possible loop inductance.

Before commencing the test it is recommended to verify the calibration and noise floor of the measurement setup.

5.1.2 Measurement Method

Set the scope to log the minimum and maximum voltage values and run the test code for a few minutes. While running the test software, any voltage spike above 1.03V or below 0.97V should be considered as a failure to meet the digital core power rail specifications.

To verify that the digital core power rail is within the specifications, the test must be repeated under different temperature conditions.

5.2 Validating Product Thermal Performance

The thermal performance validation consist of two stages:

1. Testing the EyeQ4 PCB in its housing (thermal pad, metal housing, and plastic cover) in an oven chamber.
2. Testing the entire system, including all elements in the thermal resistance in a wind tunnel.

The EyeQ4 mission profile should be taken into consideration when deciding the oven and the wind tunnel tests parameters.

5.2.1 Measurement Setup

To accurately measure the thermal performance of the product, it is important to include all internal and external heat sources and to configure each heat source’s power dissipation to be equal to its specified TDP.

5.2.2 Measurement Method

Set a data logger to log the EyeQ4 junction temperature and run the test code until the EyeQ4 temperature output stabilizes. Any temperature spike above 124^{0}C should be considered as a failure to meet the EyeQ4 specifications.

Note: To guarantee full functionality EyeQ4 T_J should not exceed the -40^{0}C to 125^{0}C temperature range. To ensure the longevity of the product refer to the maximum T_J in EyeQ4 mission profile.

Appendix A Digital Core Power Rail Test Software

The digital power rail test software tries to load every EyeQ4 core (CPU + accelerators) with the worst-case data from the heaviest operations processing. For example, a multiplier multiplying zeros draws very little current, but a multiplier multiplying random data draws much more current because the transistors making up its logic repeatedly switch from 0 to 1 and back and every switch draws current.

For the CPU, the test use a double-precision arithmetic (multiply-accumulate) and memory load operations hitting the cache.

For the MPC, the test use a single-precision arithmetic (multiply accumulate) and memory load operations hitting the cache (with an extra multiply executing per load, a special MPC feature).

For PMA, the test activates MAC4 operations in all of its DPUs [data processing units] while feeding random inputs from all the memory banks to maximize memory bandwidth as well as compute load.

For VMP, the test issues the heaviest operation in each of its asymmetric compute units [a matrix multiplication operation, a histogram update operation, and a cumulative sum.]

Note: It is infeasible to mathematically prove that a hand-written test reaches the worst case current consumption; all chip designs rely on human judgement for these tests. We are fairly confident that these tests are very close to the theoretical worst case and are quite far from any realistic scenario. For example, in a realistic scenario, not all local memory bandwidth is simultaneously used, data is far from random, not all compute units are executing the most heavy operation at every cycle, compute fabric waits for main memory data and stays idle, entire accelerators are idle waiting for input from the rest of the chip, control code is executing within an accelerator leaving most of the compute resources unused, etc.