R.V. COLLEGE OF ENGINEERING, BENGALURU - 560059
(Autonomous Institution Affiliated to VTU, Belgaum)

Design and Development of Flyback Converter

MAJOR PROJECT REPORT

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Submitted by

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in partial fulfillment for the award of degree

of

Bachelor of Engineering

in

Electrical & Electronics Engineering

R.V. COLLEGE OF ENGINEERING, BENGALURU - 560059

(Autonomous Institution Affiliated to VTU, Belgaum)

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

CERTIFICATE

Certified that the major project titled **'Design and development of Flyback converter Topology'** is carried out by **T.Vignesh Nayak (1RV14EE055)** who is bona-fide student of **R.V College of Engineering, Bangalore**, in partial fulfillment for the award of degree of **Bachelor of Engineering** in **Electrical and Electronics Engineering** of RVCE, Bangalore. It is certified that all corrections/suggestions indicated for the internal Assessment have been incorporated in the report deposited in the departmental library. The project report has been approved as it satisfies the academic requirements in respect of project work prescribed by the institution for the said degree.

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DECLARATION

I, **T.Vignesh Nayak** student of 8th semester B.E., **Electrical and Electronics Engineering**, hereby declare that the project titled **"Design and development of Flyback Converter"** has been carried out by me and submitted in partial fulfillment of the program requirements for the award of degree in Bachelor of Engineering in Electrical and Electronics Engineering of the **Visvesvaraya Technological University, Belgaum** during the year **2017-2018**.

Further I declare that the content of the dissertation has not been submitted previously by anybody for the award of any degree or diploma to any other University.

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Date: **Name** **Signature**

1.T Vignesh Nayak

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T.Vignesh Nayak

SECURE

This is to certify that

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at Secure Meters, Udaipur

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ABSTRACT

The Meter which is connected to the electric network needs power controlling and power conversion for its operation. Normally if the equipment is DC and input is AC, rectifier is needed which sometimes will give a lot of ripple. Switched mode power supply (SMPS) is used for effective conversion from AC to DC. SMPS has two topology Isolated and Non-isolated. This thesis addresses Fly back converter which belongs to isolated topology. This work addresses challenges faced in developing 20 W and two output fly back converter. Normally fly back transformer has only 75% efficiency. In order to increase the efficiency it is necessary to decide the mode in which converter should run among continuous mode, discontinuous mode and critical conduction mode. Every mode has its own advantages and disadvantages. This work addresses advantages of critical conduction mode and controller is chosen accordingly.

Reducing the switching losses MOSFET efficiency can be increased hence in this work quasi resonant mode is adopted which is done by UCC28600 controller which drives MOSFET. Transformer core must operate in near saturation region. Also transformer must have less leakage inductance so that most of the energy transfers to the secondary. Transformer parasitic parameters are calculated using the Bode 100. Simulation of transformer was also carried out using Pexprt. Feedback design must be proper in order to regulate the output voltage properly. Type 2 compensator is used to give additional gain and phase margin. Snubber and clamp circuit were designed properly to reduce transient and to limit the voltage across winding. PCB design was carried out using Altium software. Circuit is tested for its stability using Bode 100 and varied line and load condition to check for proper working. Simulation is done using TINA-TI.

Test results shows more than 80% efficiency in full load condition for input voltage from 85V AC to 265V AC. It also shows ripple voltage of 0.1mV and output maintains 30V and 50V under variable load condition. Project work exhibits good performance at low cost of less than 100Rs. This work justified the development of a fly back transformer with high efficiency with multiple outputs.

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List of Symbols

α - Percentage regulation

η - Efficiency

A_E - Cross section area of transformer

A_L - Inductance factor

A_P - Area product

A_W - Window area of the transformer

B -Magnetic field

C - Capacitor

C_1 - Compensating capacitor

C_2 - Compensating capacitor

C_{Out} - Output capacitor

C_{sn} - Snubber capacitor

C_{ss} - Soft charging capacitor

C_{VDD} - IC supply capacitor

D - Duty cycle

E - Energy

F_f - Fringing factor

F_P - Pole frequency

F_r - Ringing frequency

F_{sw} - Switching frequency

F_Z - Zero frequency

I_{avg} - Average current

I_{Out} - Output current

$I_{Pripeak}$ - Primary peak current

I_{Prirms} - Primary RMS current

I_{Secrms} - Secondary RMS current

$I_{Secpeak}$ - Secondary peak current

J - Current density

K_e - Electrical constant

K_g - Core geometry

K_u - Window utilization factor

$L_{leakage}$ - Leakage inductance

L_{Primax} - Primary maximum magnetizing inductance

N_P - Number of primary turns

N_{Pb} - Primary to bias turns ratio

N_{PS} - Primary to secondary turns ratio

N_S - Number of secondary turns

$P_{FETSwitching}$ - FET Switching losses

P_{in} - Input power

P_{OUT} - Output power

P_{Sn} - Snubber losses

R_2 - Compensating resistor

R_{Cs} - Current sensing resistor

R_L - Load resistor

R_{LED} - Series LED resistor

R_P - Primary winding resistance

R_S - Secondary winding resistance

R_{OVP} - Over voltage protection resistor

R_{Sn} - Sunbber resistor

R_{Su} - IC power supply resistor

S_d - Skin depth

T - Transfer function

t_{on} - on time of MOSFET

t_{demag} - Time for demagnitization

t_{res} - Resonance time

t_{ss} - Soft charging time

V_{CESat} - Collector emitter saturation voltage of optocoupler

$V_{CS(OS)}$ - Current sense offset voltage

V_{dd} - Supply voltage of IC

V_{dcmin} - Minimum DC voltage

V_{dcpeak} - Peak DC voltage

V_{drain} - Voltage on Drain

V_{ds} - Drain to source voltage

V_f - Forward voltage drop

$V_{leakage}$ - Voltage due to leakage inductance

V_{OUT} - Output voltage

X_L - Inductive reactance

X_C - Capacitor reactance

List of Abbreviations

AC	-	Alternating Current
BoM	-	Bill of Material
CCM	-	Continuous Conduction Mode
CS	-	Current Sense
CTR	-	Current transfer ratio
DC	-	Direct Current
DCM	-	Discontinuous Conduction Mode
EMC	-	Electro Magnetic Compatibility
EMI	-	Electro Magnetic Interference
ESR	-	Equivalent Series Resistance
FB	-	Feedback
GND	-	Ground
SOIC	-	Small outline Integrated circuit
LED	-	Light emitting Diode
MLT	-	Mean length Turn
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
MOV	-	Metal Oxide Varistor
MPL	-	Mean path length
NTC	-	Negative Temperature Coefficient
OVP	-	Over Voltage Protection
PC	-	Personal Computer

PCB	-	Printed Circuit Board
PExprt	-	Power Electronic Expert
PIV	-	Peak inverse voltage
PWM	-	Pulse Width Modulation
RMS	-	Root Mean Square
SMPS	-	Switched Mode Power Supply
SS	-	Soft Start
TINA-TI	-	Toolkit for Interactive Network Analysis – Texas Instruments
UVLO	-	Under voltage Lock Out
WUF	-	Window Utilization Factor

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CHAPTER 1

INTRODUCTION

This Chapter includes brief introduction related to AC-DC conversion, discussion about isolated and non-isolated topology. Extensive literature survey on SMPS based on Flyback topology and its modes of conduction, transformer design, and controller design. It also includes research motivation, problem statement, methodology and objectives that have been considered.

1.1 Switched Mode Power Supply

AC-DC conversion can be done by simple bridge rectifier but it adds more ripple to the system and also it doesn't regulate the output voltage. In order to regulate the output voltage linear regulator is the best choice. But as the wattage increases the efficiency decrease. So in order to increase the efficiency switching element is used which switches between on and off but dissipates less energy. This is the fundamental idea of Switched Mode Power Supply (SMPS). Regulation of output voltage by varying the duty ratio of switching element. Normally SMPS consists of 4 stages. First stage is the rectifier stage in which there is full bridge rectifier and bulk capacitor for reducing ripple. Next stage is power factor correction stage. It is optional normally it is based on application. In this project power factor correction is not considered. Next stage is switching stage where the topology is decided. At the end there is filter to reduce ripple.[1]

SMPS has few disadvantages compared to linear regulator. SMPS is noise sensitive and design is complex. Apart from these two disadvantage in most of the cases industry prefer SMPS over linear regulator. Mainly two types of SMPS are there, namely Isolated and Non-Isolated. Non isolated topology is simple and consist of generally one inductor but it is not used in consumer product because of non-isolation. Buck, Boost, Cuk are the best example of non-isolated topology. These topologies does not provide isolation. Isolated topology normally consists of transformer or optocoupler for isolation. Flyback, Push pull, forward are the examples of non-isolated topology. Because of isolation it is preferred in charger and portable devices. Normally in electric meter, isolation and multiple output are the main concern, flyback topology is the best choice [2].

1.2 Evolution of SMPS

Jean Picard et al[3] discussed about how flyback topology works in the real world. It also discusses about parasitic element effect on Flyback Topology. This work shows effect of leakage inductance and how to reduce it and different winding techniques, selection of wires to increase the transformer efficiency. This work explains in depth about cross regulation and how to mitigate it. This work explains effect of EMI, effect of parasitic on current limiting feature and benefit of adding feed forward technique. It also explains different snubber circuits and their effect on efficiency.

T-Y Ho M-S chen et al[4] discussed about different type of topologies and analysis each of topology. It also discusses about flyback topology and how it works. The work includes a design of Flyback converter. This work shows design consideration to take in order to build efficient flyback transformer. This work also explains number of ways to improve efficiency. It also discusses about active clamp, quasi resonant mode and parasitic element which affects SMPS efficiency.

Lisa Dinwoodie et al[5]discussed quasi resonant mode. This work explores advantages and disadvantages in quasi resonant mode and it explains practical difficulties in quasi resonant mode. It explains how to select controller for quasi resonant mode and explains about frequency fold back mode. Finally it gives design example to create efficient Flyback converter.

Colonel Wm. T. McLyman et al[6] discussed about flyback transformer and it types. It discusses about material property different core types and their advantage and disadvantage. This work shows how to design transformer with high efficiency and how to make trade off based on design consideration. This work shows different techniques to reduce leakage inductance, interwinding capacitance and other parasitic element. It also shows how to model transformer. It explains about selection of wire, window utilization factor, effect of high frequency, effect of parasitic on transformer. It shows different design example and design consideration to design a transformer.

Ray Ridley et al[7] discussed about snubber design. This work explains how design RC and RCD snubber based on the system requirements. This work explains effect of parasitic element on snubber. This work shows how the efficiency of power supply can be affected by inappropriate snubber choice.

Laszlo Balogh et al[9] discussed about MOSFET characteristics and their effect on power supply. It explains MOSFET characteristics, parasitic capacitances, switching losses. It shows how miller effect can change threshold voltage of MOSFET. It explains different driver circuit direct drive circuit. This work shows how to vary turn on and turn off speed of MOSFET and reduce switching losses.

Dan Mitchell et al[10] discussed control strategy for power supply. This work first explains about control strategy for buck converter for continuous conduction mode, discontinuous conduction mode. It shows different control algorithm and what is its effect on power supply. This work shows how to design a stable system and compensator for a given system.

1.3 Motivation

At end of 20^{th} century household electronics grew rapidly. It contains non-linear load. Nonlinear load injected harmonics into the grid and caused poor efficiency and power factor. So the converting and controlling of electric power became major issue. At the beginning of 21^{st} century because of energy crisis efficiency of the electronic equipment became important.

Most of the electronic gadgets needs SMPS which transfers AC to DC effectively. Portable charger, adapter, hair dryer, trimmer, LED lighting Electric meter contains SMPS. Especially in metering industry SMPS plays a major role. In India most houses has electric meter. If the SMPS does not have good efficiency losses is high. So in energy saving point of view SMPS plays a major role. So in order to save the energy we need to reduce the losses. There are so many ways to reduce the losses. One by reducing the standby power. Nowadays industries are moving towards low standby power normally in meter low standby power is needed. SMPS goes to full load when sending the data. Apart from this situation most of the time SMPS is on no load. By choosing the right controller we can reduce this loss.

Transformer design must be proper so that it can have less leakage inductance. Selection of wires based on calculation of current density, the way of winding. Selection of core play an important role. Finally the switching losses. MOSFET must have less switching losses this can be achieved by soft switching. These problems need to be addressed so that is the reason this project has been taken up. By

implementing all these we can implement high efficiency low cost flyback converter with multiple output which can meet industrial standards.

1.4 Problem Statement

To design a SMPS based on a flyback converter topology for universal input ($85V_{AC}$ to $265V_{AC}$) which has two output namely 50V & 0.1A (5W) and 30V & 0.5A (15W) to give more than 85% efficiency with regulated output voltage and less ripple content.

1.5 Main Objective:

To design and develop Flyback which has two output with high efficiency and less ripple.

- SMPS must be efficiently convert input voltage variation from $85V_{AC}$ to $265V_{AC}$ to the desired output voltage of 50V and 30V respectively with less ripple.
- Output voltage must be constant irrespective of load.
- Simulation of circuit using TINA-TI software
- Development of highly efficient and cost effective SMPS.
- Development of hardware, testing and validation of integrated system.

1.6 Methodology

Based on literature review, flyback converter can be build which can be reliable, cost effective, and efficient. The project is undertaken in order to increase the efficiency, reduce ripple, maintain regulation irrespective of load regulation and mitigate cross regulation.

Every design need input specification. In this project input range chosen as universal input and output is specified as 30V and 0.5A (15Watt) and 50V and 0.1A (5Watt). Quasi resonant mode is selected in order to reduce switching losses and UCC28600 IC drives MOSFET. Reflected voltage considered based on stress on primary and secondary side. Based on reflected voltage and minimum duty cycle transformer turns is decided. Core selection done based on wattage and window area. After this transformer constructed with interleaved winding to reduce leakage inductance. After this leakage inductance measured and snubber design must be completed accordingly. According to input and output specification input capacitor, output capacitor diodes are selected. MOSFET selection is made based on voltage stress.

Based on UCC28600 requirements current sense resistor, power limit resistor, line and load overvoltage resistor selected according to electrical characteristics specified in the datasheet. Finally closed loop design must be done. Type 2 compensator is selected to give appropriate phase margin, gain margin and good dynamic response.

PCB design must done accordingly. PCB fabrication and components should be mounted properly. Tests are conducted for universal input and different load condition and results must validate against theoretical and simulation.

1.7 Organization of the report:

The report has been organized into various chapters and each chapter has been explained briefly as follows:

Chapter 1: This chapter includes introduction to SMPS, Literature survey, objective and methodology.

Chapter 2: This chapter deals with basics of Flyback converter, Different types of conduction mode and its comparison especially about quasi resonant mode and explanation about UCC28600IC and way it operates.

Chapter 3: This chapter focuses on Component selection such as diode, MOSFET, capacitor, snubber calculation of the parameters for circuit design and UCC28600 design based on its electrical characteristics. It explains transformer design completely, the parameters necessary for a design, the way it is constructed and transformer modelling using Bode 100 and simulation of Transformer using Pexprt.

Chapter 4: This chapter explains requirements for a closed loop to be stable and detailed design analysis closed loop system for SMPS using TL431 and optocoupler.

Chapter 5: This chapter gives how the PCB made using Altium, hardware development and detailed analysis of the results obtained.

Chapter 6: This chapter gives the future scope of the project and summaries the objectives achieved as conclusion.

CHAPTER 2

FLYBACK TOPOLOGY

This chapter includes fundamental theory of flyback topology, how it works and comparison of discontinuous conduction mode, continuous conduction mode and detailed explanation of quasi resonant mode. It also gives explanation about UCC28600IC, pin details of UCC28600 and its operation based on line and load condition.

2.1 Theory of Flyback

Flyback topology is known for low efficiency, poor cross regulation, multiple outputs, better isolation and low number of components. It is suitable for low wattage application less than 200Watt. Normally notebook adopter, chargers, set up boxes, electric meter uses this topology. Normally when it comes to isolated power supply flyback has many advantages. First of all transformers gives isolation, separates primary from secondary and avoids electric shocks which is really helpful in consumer product. Transformer also helps in suppressing the ripple no need of extra filter circuit, simple capacitor is enough. Even though it is called as transformer, in reality it is a coupled inductor which is discussed later in Chapter 4. Flyback converter can accommodate multiple output which can be used for many application. Based on turns ratio output voltage can be step up or step down. Only limitation for number of outputs is number of transformer pins. It has relatively less number of components compared to other topologies. In mass production flyback has upper hand because of less number of components and less bill of material. Even though there are problems related to flyback such as efficiency, poor cross regulation which can be improved but elimination is difficult. But proper design consideration can make flyback topology highly efficient. Normally flyback topology consists of a transformer, MOSFET, diodes and output filter. MOSFET is used for switching purpose which is driven by PWM generator. Clamp circuit used for to clamp the overshoot voltage generated by leakage inductance. Transformer is used for isolation, Energy storage and energy transfer. At the output end capacitor are used to reduce the ripple. Output voltage depends on the turns ratio of the transformer[1]. Based on the voltage and current

rating component must be selected and other design consideration is discussed in Chapter 4. Fig. 2.1 shows basic circuit diagram of Flyback topology [2].

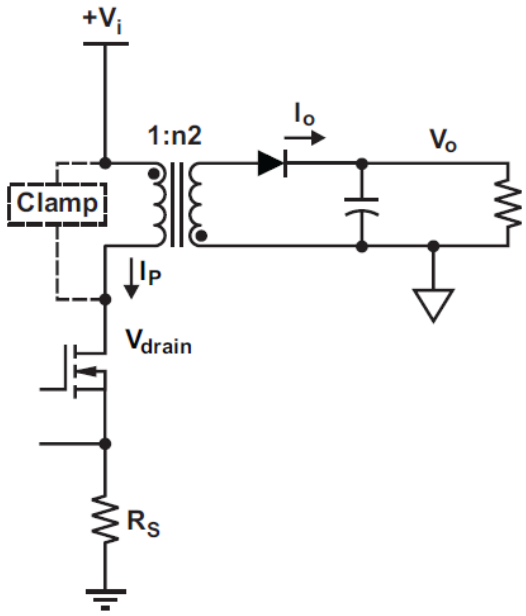

Fig. 2.1 Basic circuit of Flyback Converter

2.1.1 Working Principle of Flyback converter:

Fig. 2.2 shows working of simple flyback topology. There are three stages in Flyback converter operation. In the first stage MOSFET is switched on and the primary current starts rising it raises to maximum value and energy is stored in this period between air-gap of Ferrite core transformer. In this stage energy supplied on output is only by output capacitor. Once the current reaches its peak value MOSFET switched off. In the second stage energy transfer occurs. Once the MOSFET switched off, dotted end become more negative compared to un dotted end. So on the secondary side diode be forward biased and leakage inductance oppose this change, voltage overshoot occur at the drain side of the MOSFET and it cause the ringing with MOSFET parasitic capacitance. When all the energy transfers to the secondary side, in the primary side parasitic component of MOSFET and magnetizing inductance forms a LC circuit and start to resonate. So the next switching can be any time. It depends upon the mode of the energy transfer[3].

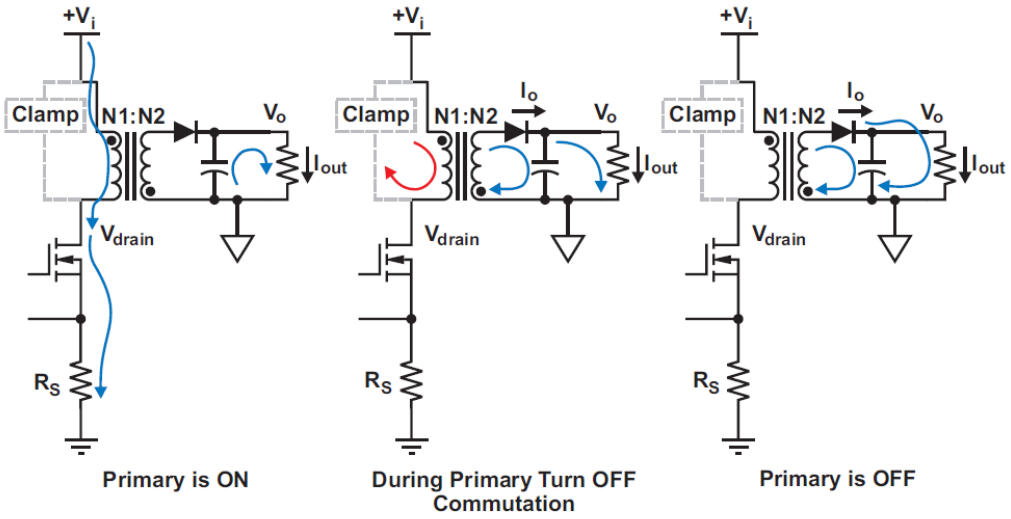

Fig. 2.2 Operational stages of flyback converter

2.2 DCM and CCM

Energy transfer can be happen in two ways. First one is Discontinuous conduction mode (DCM) where all the energy transfers to the secondary side. Second one is Continuous Conduction Mode (CCM) where part of the energy still remains in the air gap when MOSFET again switched on[2]. These two have their own advantage and disadvantage; it is tabulated in Table 2.1.

TABLE2.1 COMPARISON BETWEEN DCM AND CCM

Mode Of Operation	Advantage	Disadvantage
DCM	• No diode reverse recovery loss • Constant switching frequency • First Order system	• Large ripple and peak current • Higher MOSFET conduction loss and voltage stress • High core loss
CCM	• Small ripple and peak current • Low core loss • Better cross regulation	• High diode reverse recovery loss • Low light load efficiency

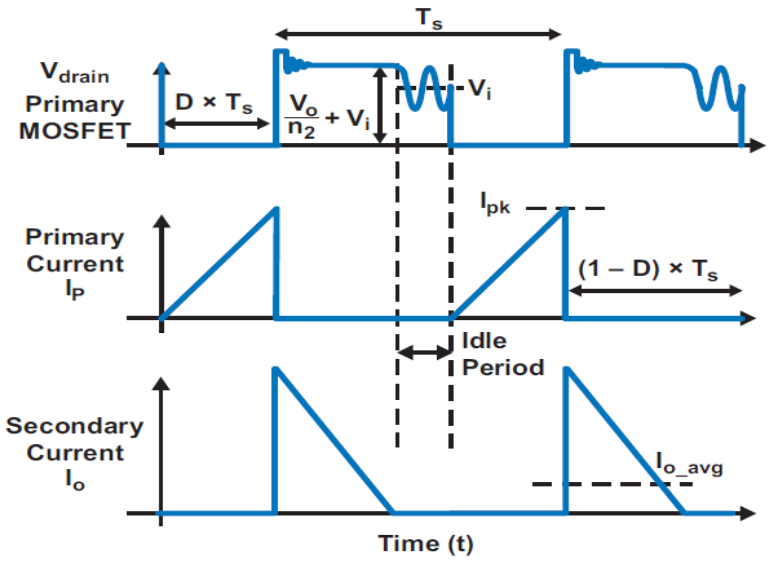

Fig. 2.3 Waveform of DCM

Fig. 2.3 shows primary goes to zero then secondary current starts rising. So complete energy transferred to the secondary.

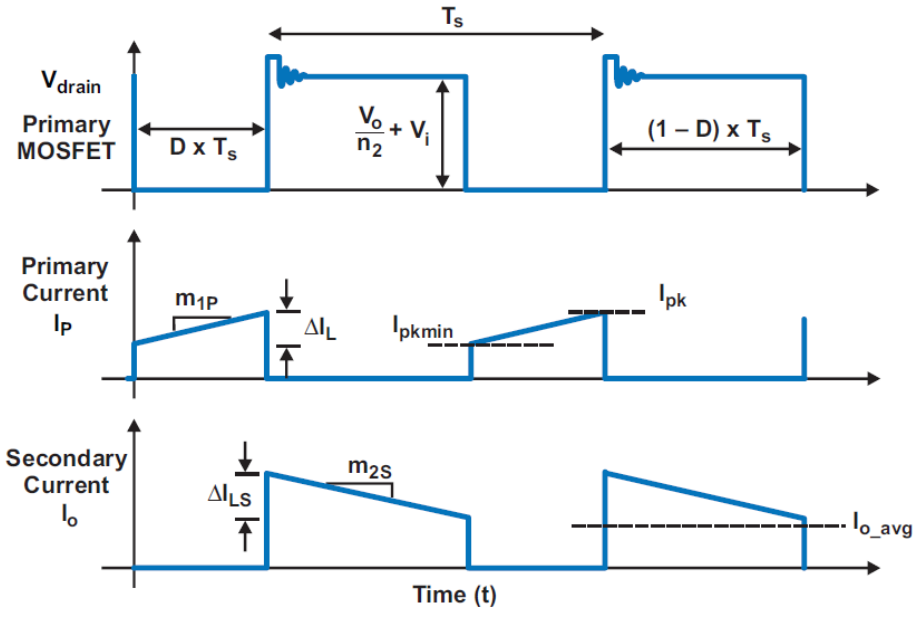

Fig. 2.4 Waveform of CCM

Fig. 2.4 shows secondary starts rising when primary current is not zero. Energy is still left in the transformer.

2.3 Quasi resonant Mode

In order to overcome disadvantages of Discontinuous Conduction Mode, controller must to do soft switching. There are many ways to do soft switching. In olden days there is a dedicated resonant converter to detect when current goes to zero to initiate next switching. This type of circuit increases bill of material. Quasi means something similar so quasi resonant mode uses circuit parasitic ringing to initiate next switching. Once the core is demagnetized completely MOSFET output capacitance and magnetizing inductance forms a resonant circuit and starts ringing. In DCM next switching can start at any valley and it causes a lot of switching losses. But in quasi resonant Mode switching happens at first valley and MOSFET losses are square of the voltage across drain to source, hence it reduces all the MOSFET switching losses. Fig. 2.5 shows waveform of quasi resonant mode. In the first valley MOSFET switches on and reduction in MOSEFET switching loss. Quasi resonant mode has other advantages too like less electromagnetic interference, better transient response. So the difference is in the switching. Quasi resonant mode is soft switching, the frequency of the oscillator is modulated and DCM is hard switching, oscillator frequency is held constant[5].

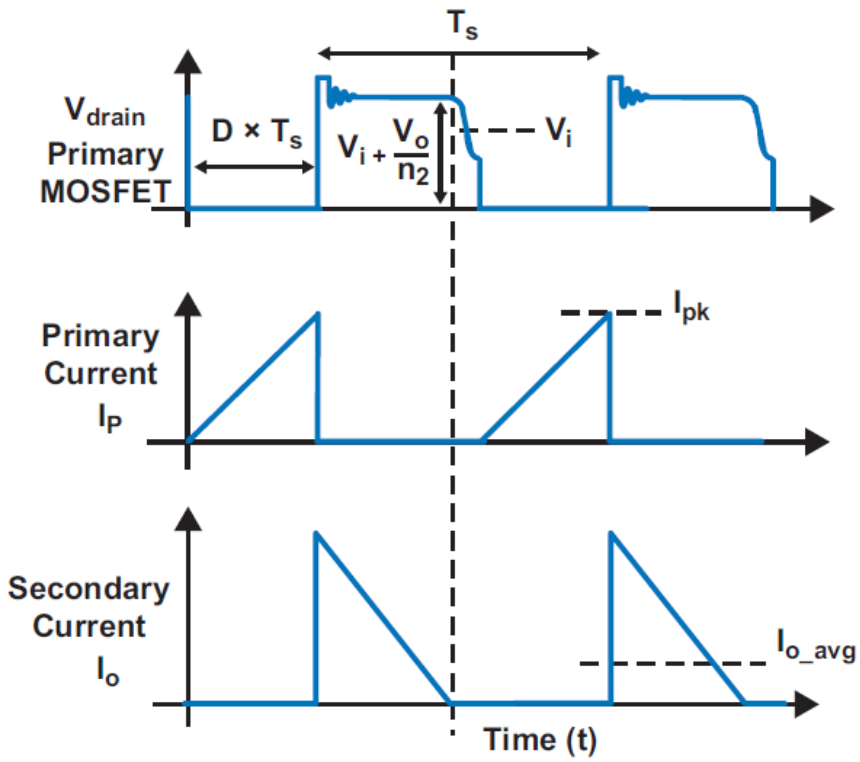

Fig. 2.5 Waveform of Quasi Resonant Mode

2.4 UCC28600

In order to do quasi resonant switching controller must detect valley, UCC28600 is the IC which detects the valley and suitable for quasi resonant mode. Fig. 2.6 shows the UCC28600 top view. UCC28600 works in green mode, frequency foldback mode based on load condition. It also has overvoltage protection, over temperature detection, under voltage lockout and power limit feature. It has low start up current which is 25μA. It is a PWM controller whose pulse width depends on feedback voltage[14].

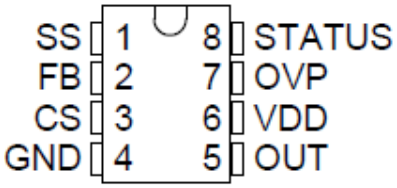

Fig. 2.6 D Package 8 Pin SOIC Top View

TABLE 2.2 PIN FUNCTIONS OF UCC28600

Name	Number	I/O	Description
SS	1	I	Soft start pin. It helps starting the IC. The rate depends on capacitor value. When fault detected it discharges through internal MOSFET.
FB	2	I	Feedback pin. It takes feedback from optocoupler.
CS	3	I	Current sense pin. It is used for over current protection for MOSFET and also for power limit.
GND	4	-	Ground pin.
OUT	5	O	Output pin drives the power MOSFET.
VDD	6	I	This pin provides power to the device. It is connected to auxiliary winding of the transformer.
OVP	7	I	Overvoltage protection pin. It senses line and load overvoltage.
STATUS	8	O	Status pin can be used to disable PFC circuit.

2.4.1 Operation of UCC28600

UCC28600 controller has different operating modes based on line and load condition. It modulates both frequency and peak primary current. Fig. 2.7 shows operation of UCC28600. At heavy loads from 100% to 30% controller have less switching frequency so that there is more time for demagnetizing and it also reduces switching loss. As the load decreases the switching frequency increase because less energy to deliver. But it causes problem at light load because frequency is very high. So in order to avoid this controller clamps frequency at 130KHz. When load is between 30% to 10% controller run frequency fold back mode. In which it modulate the frequency by keeping the current constant. At very light loads controller clamps the frequency to 40KHz and run in Green mode or Burst mode to save the energy. In burst mode packets or burst of 40KHz runs the MOSFET[14].

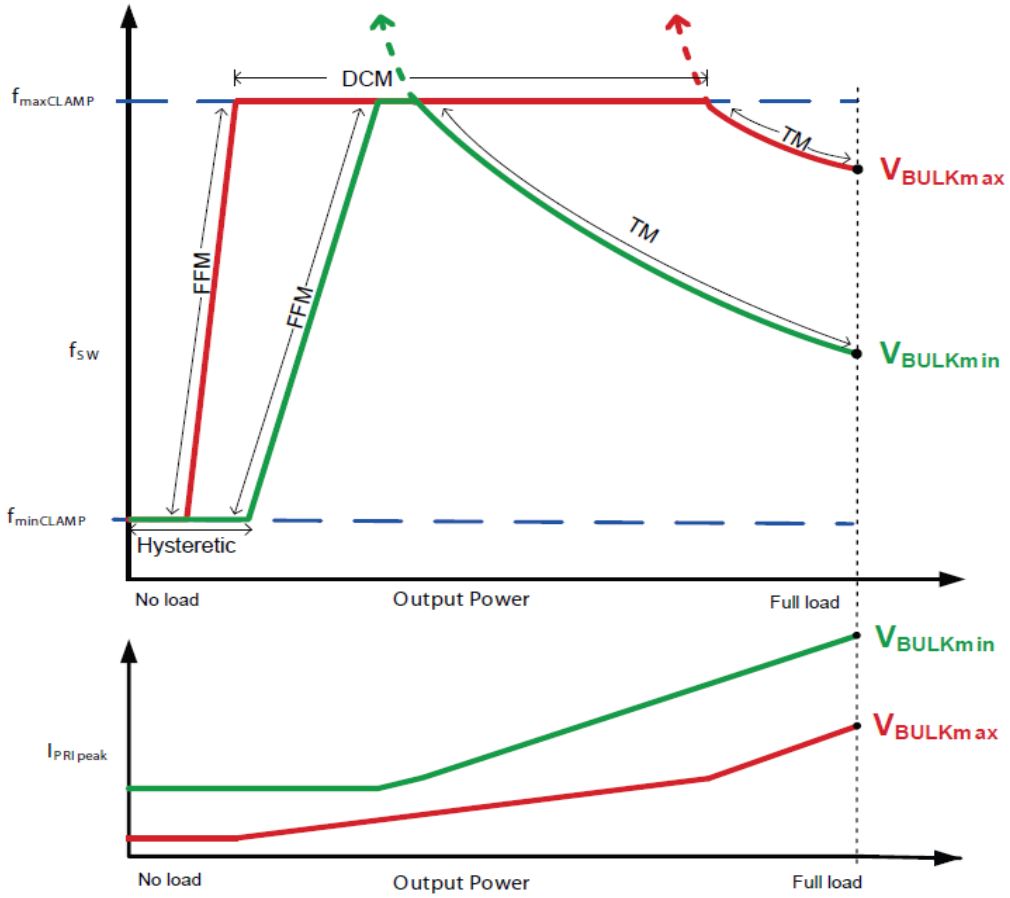

Fig. 2.7 Mode of UCC28600 under different line and load condition

These line and load condition are determined by voltage at feedback pin. This feedback obtained from optocoupler. It provides isolation to the circuit. Fig. 2.8 shows different operating mode based on voltage on the feedback.

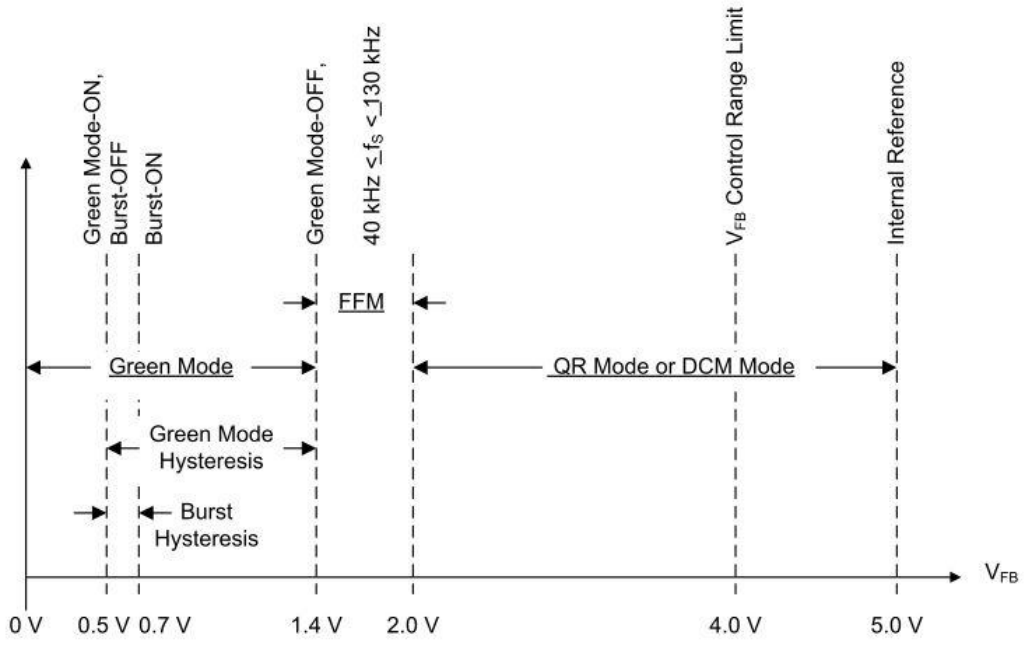

Fig. 2.8 Operating mode of UCC28600 based on voltage at feedback pin

CHAPTER 3

SYSTEM DESIGNING

This chapter deals with system designing and component selection for the circuit given. It also includes capacitor value calculation, diode and MOSFET rating calculation, snubber calculation and required component values for UCC28600. It explains transformer design completely, the parameters necessary for a design, the way it is constructed and transformer modelling using Bode 100 and simulation of Transformer using Pexprt.

3.1 Methodology

Based on the literature review Flyback Topology is developed.

- To operate in universal input and give high efficiency and reliable
- To give less ripple and load independent

To develop the proposed system following methodology is implemented:

1. Mentioning input specification and output specification
2. Calculation of input capacitor value, diode, MOSFET rating, designing of transformer based on specification and calculation of snubber, UCC28600 parameters, output capacitor and feedback design.
3. Simulation of the circuit using TINA- TI.
4. Development of prototype, testing and validation

3.2 Block Diagram

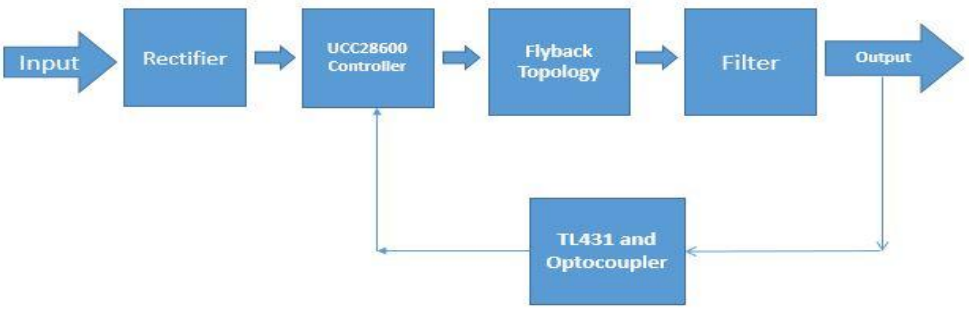

Fig. 3.1 Block diagram of entire system

Fig. 3.1 shows block diagram of Switched mode power supply using Flyback converter. It has fullbridge rectifier, transformer, UCC28600, closed loop and output filters. Fig. 3.2 shows actual circuit diagram of SMPS.

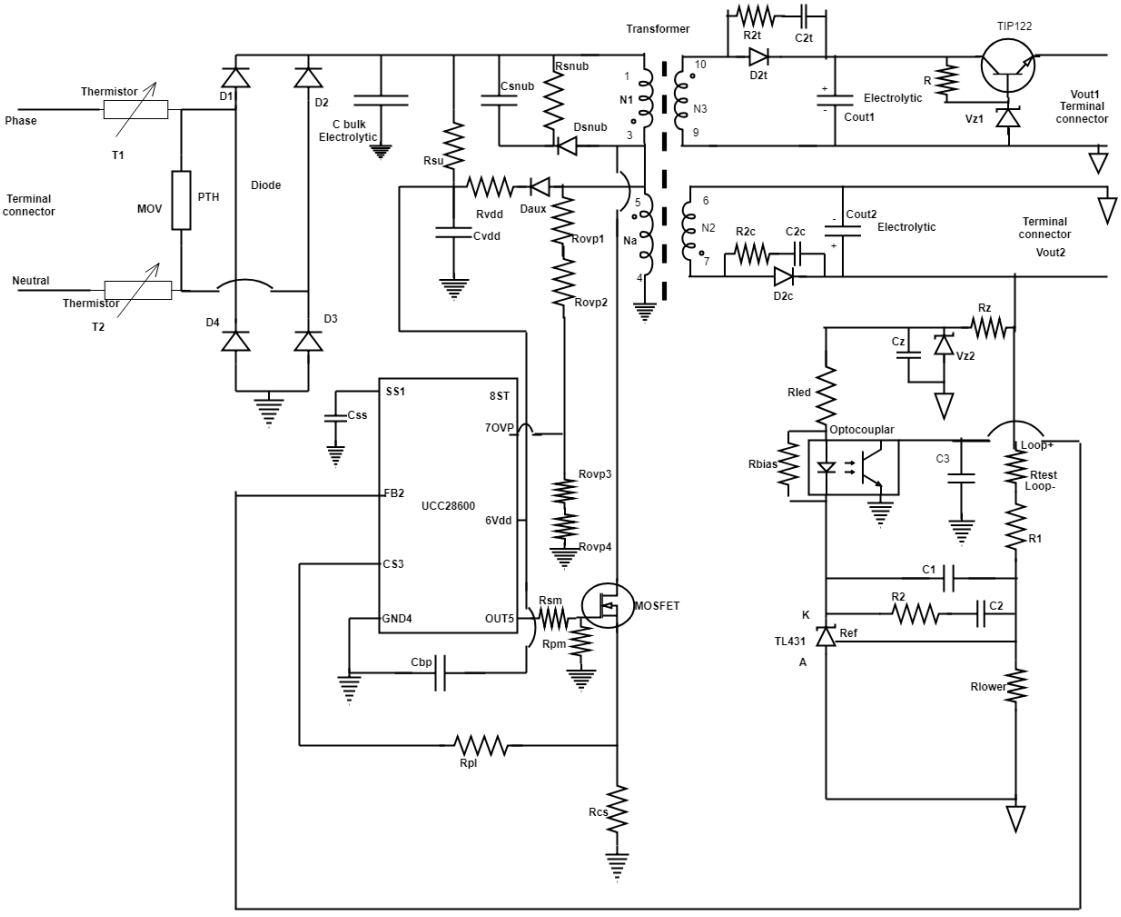

Fig. 3.2 Complete circuit diagram with connection

3.3 Specifications

In order to design a flyback converter specification of input and output are necessary. Table 3.1 gives input and output specification. Any system can't be 100% efficient but based on literature survey flyback give 70% to 80% efficiency. In this project aim is to achieve 85% efficiency. At the output ripple free is difficult to achieve. A reasonable ripple needs to be there. Input and output is based on the application. Input frequency is based on region of operation. In India grid frequency is 50Hz. In this project input is selected as universal input design is based on minimum voltage which is considered as worst case.

Table 3.1 Input and output specification

INPUT SPECIFICATION		OUTPUT SPECIFICATION	
AC rms V min	85	DC voltage	30V
AC rms V max	265	DC current	.5A
Frequency	47.5 to 52.5	DC voltage	50
Efiiciency	>.85	DC current	0.1A
Power	23.529W	Output ripple(ΔVout)	.3V
		Power	20W

3.4 Calculation of Parameters on Primary side

In order to design 20 Watt SMPS input current must be known. This can be calculated by calculating the input power. If output power is 20W then input power is given by equation 3.1

$$P_{in} = \frac{P_{out}}{\eta} \tag{3.1}$$

Input power is 23.529W. Then input current is given by equation 3.2

$$I_{avg} = \frac{P_{in}}{V_{dc\,min}} \tag{3.2}$$

$I_{avg} = 0.260A$

Based on the duty cycle peak current is decided. So in order find D_{max} reflected voltage is needed. Reflected voltage is the voltage reflected on the primary when secondary is conducting. Reflected voltage also called as Flyback voltage. Reflected voltage value also decides stress on MOSFET and secondary side. For example choosing the higher value of there is higher stress on MOSFET. Choosing the lower value there is more stress on secondary. Normally in order to reduce secondary side stress high value is chosen. It depends on the output rating. Flyback voltage or reflected is assumed as 95V.

$V_{reflected} = 95V$

$V_{min} = 90V$

$$D_{Max} = \frac{V_{reflected}}{(V_{reflected} + (V_{min} - V_{ds}))} \quad (3.3)$$

$D_{max} = 0.507$

$$I_{peak} = (2 \times \frac{I_{avg}}{D}) \quad (3.4)$$

$I_{peak} = 1.02564A$

$$I_{prirms} = I_{pripeak} \times \sqrt{\frac{D}{3}}$$

(3.5)

$I_{prirms} = 0.421A$

Full bridge rectifier diode must withstand 0.421A. So peak inverse voltage for fullbridge rectifier is equal to maximum input voltage which is 265V. For input capacitor calculation ripple voltage value is needed. 20% to 30% ripple is allowed. Normally input capacitor is electrolytic. Capacitor selection is difficult for less ripple. Fig. 3.3 shows output waveform of fullbridge rectifier[4].

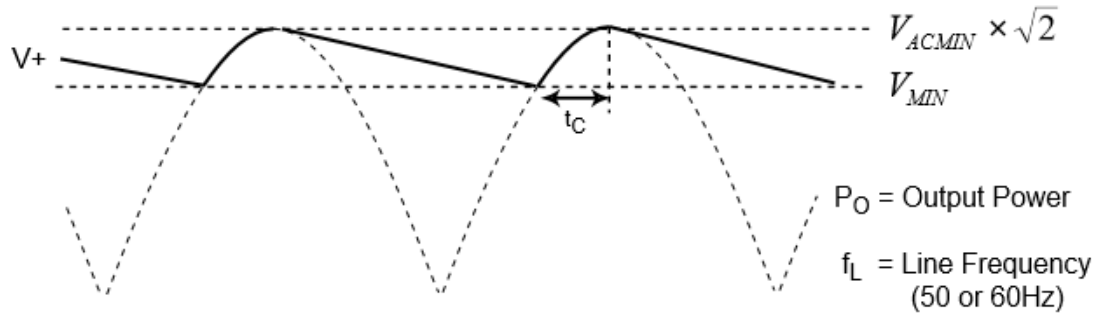

Fig. 3.3 Fullbridge output voltage waveform

Time instant when voltage across capacitor is V_{min}

$$T_{min} = \frac{1}{(2 \times \pi \times f)} \times \sin^{-1}(\frac{V_{dc\,min}}{V_{dcpeak}}) \quad (3.6)$$

Time instant when voltage across capacitor is $V_{ACMIN*\sqrt{2}}$

$$\frac{1}{(2 \times \pi \times f)} \times \sin^{-1}(\frac{V_{dcpeak}}{V_{dcpeak}}) \quad (3.7)$$

$$T_c = \left(\frac{1}{(2\times\pi\times f)}\times\sin^{-1}\left(\frac{V_{dcpeak}}{V_{dcpeak}}\right)\right) - \left(\frac{1}{(2\times\pi\times f)}\times\sin^{-1}\left(\frac{V_{dc\,min}}{V_{dcpeak}}\right)\right) \quad (3.8)$$

Discharge time of capacitor is given by the equation 3.9

$$T_c + T_d = 10mS \quad (3.9)$$

Capacitor value can be found out by using the equation 3.10

$$C = \frac{(2\times P_{in}\times T_d)}{(V^2_{dcpeak} - V^2_{dc\,min})} \quad (3.10)$$

By substituting desired value of ripple, capacitance value can be obtained. Table 3.2 shows different capacitor value for different ripple.

TABLE 3.2 CAPACITOR VALUES FOR DESIRED RIPPLE VOLTAGE

$V_{ACMIN}*\sqrt{2}$	Ripple	V_{min}	T_C	T_D	Value of Capacitance
120.208V	30	90.208	2.298mS	7.701mS	57.40μF
120.208V	25	95.208	2.250mS	7.746mS	69.06μF
120.208V	20	100.208	1.862mS	8.137mS	88.59μF

So the capacitor voltage must be withstanding maximum voltage $265\times\sqrt{2}$ which 375V. Hence capacitor needed is 88.59μF and voltage rating of 375V.

MOSFET must withstand primary rms current and it must have low gate threshold voltage. When MOSFET is in switched off condition the voltage it must withstand is given below. Fig. 3.4 shows voltage across MOSFET in off condition[9].

$V_{drain} = V_{max} + V_{reflected} + V_{leakage} + V_{spike}$ = 375 + 95+ 230 that is 700V.

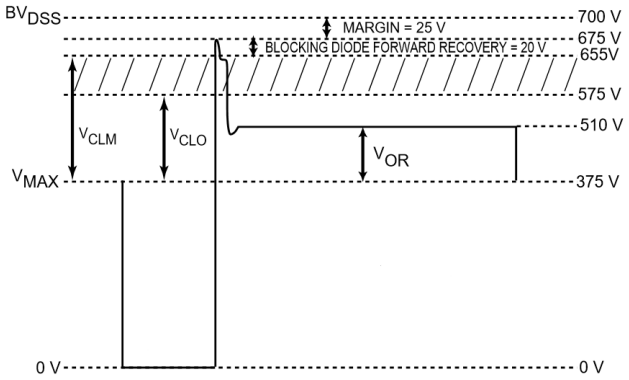

Fig. 3.4 Voltage across MOSFET when it is off

Losses in MOSFET are calculated below.

$$P_{Conductionloss} = I_{prirms}{}^{2} R_{dson} \quad (3.11)$$

R_{dson} = 5Ω.

Loss =1.2Watt

Switching loss is calculated below.

$$P_{FETSwtching} = F_{max} \times [(\frac{C_{oss} \times V^{2}_{DS}}{2}) + (\frac{(V_{Bulk\,min} + V_{Flyback}) \times I_{Pripeak} \times t_{f}}{2})] \quad (3.12)$$

$P_{FETSwitching}$ =1.3015mW.

So total loss in MOSFET is switching loss + conduction loss.

Total loss = 1.2013015W

When MOSFET switch off, complete energy can't be transferred to secondary because of leakage inductance. Energy stored in leakage inductance needs a path. If snubber circuit is not there, MOSFET output capacitance gets charged and destroys the MOSFET. So the proper snubber design very important. Fig. 3.5 shows waveform of snubber circuit. In order to design snubber leakage inductance value which is taken from next chapter. Value of leakage inductance obtained is 4μH. Power in leakage inductance must be completely dissipated in snubber circuit[7].

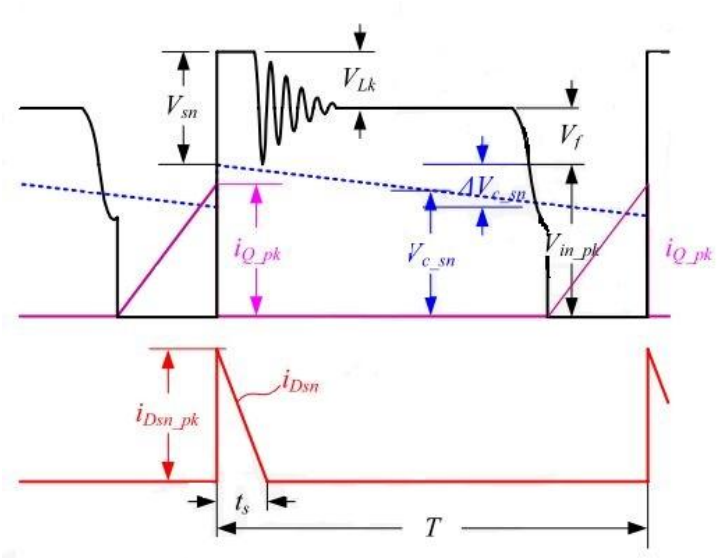

Fig. 3.5 Waveform of snubber circuit

So the value of resistor is given by equation 3.13.

$$R_{sn} = \frac{V_{sn}^{\ 2}}{((\frac{1}{2}\times L\times I^2)\times(F_{sw})\times(\frac{V_{sn}}{V_{sn}-(nV_{out})}))} \tag{3.13}$$

Selection of V_{sn} is critical. Lower the value more slow commutation process. Higher the value faster the commutation but it may degrade cross regulation. Generally two to three times the reflected voltage value is acceptable. Hence V_{sn} = 250V.

R_{sn} = 119KΩ

To calculate value of snubber capacitor ripple voltage must be assumed. Value of ripple voltage is 50V. Value of capacitance obtained by equation 3.14.

$$C_{sn} = \frac{V_{sn}}{(\Delta V_{sn}\times F_{sw}\times R)} \tag{3.14}$$

C_{sn} = 4.7nF

Power dissipation in snubber circuit is given by equation 3.15.

$$P_{sn} = \frac{V^2_{sn}}{R_{sn}} \tag{3.15}$$

P_{sn} = 0.33W

In order to know the value of primary inductance we must decide turns ratio and switching frequency. Turn ratio requires little foresight on secondary side. In order to reduce conduction loss in secondary diode must be chosen carefully. Turns ratio given by equation 3.16

$$\frac{N_P}{N_S} = \frac{(V_{IN}-V_{DS})\times D}{(V_O+V_{fw})\times(1-D)} \tag{3.16}$$

$\frac{N_P}{N_S}$ for 30V output is 3.15

$\frac{N_P}{N_S}$ for 50V output is 1.89

UCC28600 has ability to switch MOSFET between 40KHz to 130KHz. Inductance value depends on duty cycle. So switching frequency is selected as 80KHz. Even though quasi resonant mode has little dead time which is difficult to calculate. Hence resonant time must be assumed to be 100nS in order to calculate duty cycle. And according to conservation of energy, energy stored in on time must be equal to energy transferred in off time. Using equation 3.17 and 3.18 T_{ON} can be obtained[14].

$$T_{sw} = t_{on} + t_{demag} + t_{res} \tag{3.17}$$

$$V_{bulk\,min} \times t_{on} = N_{ps} \times (V_{out} + V_F) \times t_{demag} \tag{3.18}$$

T_{ON} = 6.186μS.

Hence duty cycle is 0.507

Value of primary inductance given by equation 3.19.

$$L_{pri\,max} = \frac{V_{dc\,min} \times D_{max}}{I_{Pri} \times F_{sw}}$$

(3.19)

L_{primax} = 570μH.

3.5 Calculation of parameters of UCC28600

UCC28600 has overvoltage protection, power limit, current sense, soft start features. Fig. 3.6 shows component for UCC28600. Every input pin has its own electrical specification based on that resistance value must be calculated. UCC28600 has under voltage lockout, below 8V it won't start. It checks all the line and load condition once everything is perfect and at V_{DD} pin 13V available, it charges the soft charging capacitor and it checks the voltage at feedback pin based on that mode of the controller is decided.

In the beginning current flowing from R_{su} charge the C_{VDD} in the next cycle transformer auxiliary winding supply power to the V_{DD} pin. Auxillary diode must have less reverse recovery time in order to cope up with the switching. UCC28600 gets the signal for thermal shutdown in high temperature. UCC28600 is sensitive to Rovp, R_{Pl}

and R_{cs} values[14]. In order to calculate the resistances values we need to know the primary to bias turns ratio which is given by equation 3.20.

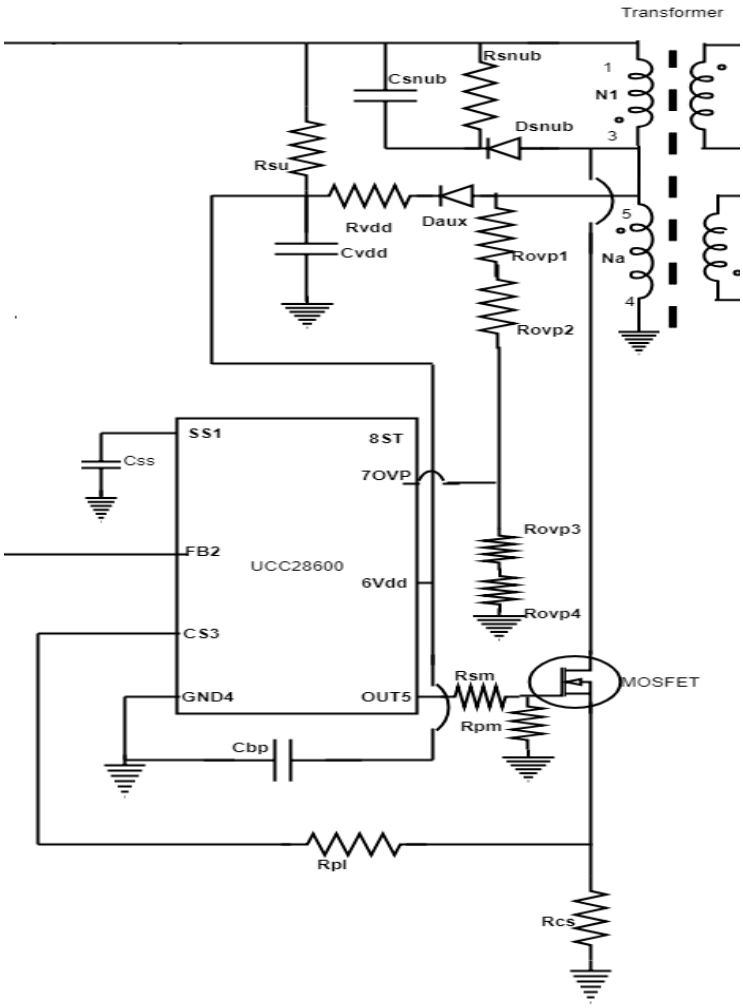

Fig. 3.6 Components for UCC28600

$$N_{pb} = N_{ps} \times (\frac{V_{out}}{V_{bias}}) \tag{3.20}$$

$N_{pb} = 6.25$

$$R_{ovp1} = \frac{V_{Bulk}}{(N_{pb} \times I_{ovpline})} \tag{3.21}$$

$I_{ovpline} = 450\ \mu A$

$R_{ovp1} = 133.33K\Omega$

$$R_{ovp2} = R_{ovp1} \times \frac{V_{ovp}}{((\frac{N_{ps}}{N_{pb}} \times (V_{outshut} + V_f)) - V_{ovpload})} \quad (3.22)$$

$V_{ovpload}$ = 3.75 V

R_{ovp2} = 36.39KΩ

Current sense and power limit resistor are calculated as below.

Ipeak for low line = 1.02564A = I_{P1}

Ipeak for max load = 0.2690A = I_{P2}

$$I_{cs(1)} = 0.5 \times (550mV \times (\frac{1}{R_{ovp1}} + \frac{1}{R_{ovp2}}) + \frac{V_{bulk\,min}}{N_{pb} \times R_{ovp1}})$$

(3.23)

$I_{cs(1)}$ = 64.8195uA

$$I_{cs(2)} = 0.5 \times (550mV \times (\frac{1}{R_{ovp1}} + \frac{1}{R_{ovp2}}) + \frac{V_{bulk\,max}}{N_{pb} \times R_{ovp1}}) \quad (3.24)$$

$I_{cs(2)}$ = 414.01uA

$$R_{cs} = \frac{(V_{pl} - V_{cs(os)}) \times (I_{cs(2)} - I_{cs(1)})}{(I_{cs(2)} \times I_{p(1)}) - (I_{cs(1)} \times I_{p(2)})}$$

(3.25)

V_{pl} = 1.20V

$V_{cs(os)}$ = 0.40V

R_{cs} = 0.875Ω

$$R_{pl} = \frac{(V_{pl} - V_{cs(os)}) \times (I_{p(2)} - I_{p(1)})}{(I_{cs(1)} \times I_{p(2)}) - (I_{cs(2)} \times I_{p(1)})} \quad (3.26)$$

R_{pl} = 2.25KΩ

Soft charging capacitance value can be found out once the soft charging time is found out.

$$t_{ss\,min} = \frac{(C_{out} \times V^2_{out})}{(2 \times P_{lim})}$$

(3.27)

$t_{ssmin} = 3.419\mu S$

$$t_{ss\,min} = [-R_{load} \times \frac{C_{out}}{2}] \times [\ln \frac{(Vout - \Delta V)}{(R_{load} \times P_{out\,lim})}]$$

(3.28)

$t_{ssmin} = 47.230nS$

t_{ssmin} must greater of above two. So $t_{ssmin} = 3.419\mu S$

So the capacitance value given by the equation 3.29

$$C_{ss} \rangle I_{ss} \times [\frac{t_{ss\,min}}{A_{cs(FB)} \times (V_{pl} - V_{cs(os)})}] \quad (3.29)$$

$I_{ss} = 6\mu A$ and $A_{cs(FB)} = 2.5$

$C_{ss} > 10.25nF$

Equation 3.30 gives R_{su} value.

$$R_{su} = \frac{V_{bulk(min)}}{I_{startup}} \quad (3.30)$$

$I_{startup} = 25\mu A$

$R_{su} = 4.7M\Omega$

Calculation of C_{VDD} and R_{VDD} are done below.

$$R_{vdd} = (\frac{\pi \times N_b}{4 \times N_p}) \times (\frac{V_{ds1(os)} \times f_{QR(max)} \times \sqrt{L_l \times (C_D + C_{snub})}}{I_{DD} + (C_{ISS} \times V_{out(hi)} \times f_{QR(max)}}) \quad (3.31)$$

I_{DD} is the operating current of the UCC28600 which is 20mA.

C_{ISS} is the input capacitance of MOSFET which is 350pF.

$V_{OUT(Hi)}$ is $V_{(OH)}$ of the OUT pin, either 13 V (typ) V_{OUT} clamp or less as measured.

V_{ds1}(os) is the amount of drain-source overshoot voltage.

R_{VDD}=48.32Ω

$$C_{vdd} = (I_{DD} + (C_{ISS} \times V_{out(hi)} \times f_{QR(max)}) \times \frac{T_{Burst}}{\Delta V_{DD(burst)}} \quad (3.32)$$

T_{BURST} is the measured burst mode period.

ΔV_{DD}(burst) is the allowed VDD ripple during burst mode.

ΔV_{DD}(uvlo) is the UVLO hysteresis.

C_{VDD} = 1.432μF.

$$C_{vdd} = (I_{DD} + (C_{ISS} \times V_{out(hi)} \times f_{QR(max)}) \times \frac{T_{ss}}{\Delta V_{DD(UVLO)}} \quad (3.33)$$

C_{VDD} = 7.58μF.

C_{VDD} must be greater of above two. Hence C_{VDD} is 7.58μF.

3.6 Calculation of Parameters on Secondary side

First set of calculation are for 30V and 0.5A. It includes calculation secondary current, diode rating calculation and capacitor rating calculation.

$$I_{secpeak} = \frac{N_p}{N_s} \times I_{pripeak} \quad (3.34)$$

$I_{secpeak}$ = 3.214A

Diode must withstand Peak inverse voltage of 151V which is given by equation 3.35.

$$PIV = Output + V_{dcmax} \times \frac{N_s}{N_p} \quad (3.35)$$

$$I_{secrms} = \sqrt{\frac{2 \times I_{out} \times I_{peak}}{3}} \quad (3.36)$$

I_{OUT} = 0.5A.

I_{secrms} = 1.039A.

Output capacitor calculation requires three things.

- Value of capacitance
- Voltage rating of capacitor
- Equivalent series resistance (ESR)

$$I_{out} = C\frac{dv}{dt} \tag{3.37}$$

dV is ripple which is 0.3V

C_{out} = 60.77μF.

$$I_{ripple} = \sqrt{I_{secrms}{}^2 - I_{dcsec}{}^2} \tag{3.38}$$

I_{ripple} = 0.910A

ESR must be less than $\frac{dV}{I_{ripple}}$ which is 329mΩ.

At the secondary side, presence of leakage inductance cause voltage spike. Proper design must be done in order to reduce voltage spike. Calculation of snubber resistor and capacitor are shown below. Secondaary side leakage inductance given by the equation 3.39.

$$L_{l2} = \frac{L_{l1}}{N_{Ps}{}^2} \tag{3.40}$$

L_{l2} = 0.41μH

$$Fr = \frac{1}{\sqrt{2 \times \pi \times L_l \times Cp}} \tag{3.41}$$

Parasitic capacitance value is 100pF which is obtained by transformer modelling which is explained in next chapter.

F_r = 63.078MHz

By equating characteristic impedance to resistance oscillation can damped.

$$R = Z = \sqrt{X_L{}^2 + X_C{}^2} \tag{3.42}$$

$R = 60\Omega$

$$C = \frac{1}{(2 \times \pi \times F_r \times R)} \tag{3.43}$$

$C = 88.41nF$

Power loss in secondary snubber is calculated below.

$$\text{Power loss} = \frac{L_{l2} \times I^2_{secrms}}{2} \tag{3.45}$$

$= 0.22Watt$

It also contains closed loop. Closed loop design is discussed in chapter 4.

So the same calculation goes for 50V and 0.1A.

$I_{secpeak} = 1.944A$

$I_{OUT} = 0.1A.$

$I_{secrms} = 0.360A.$

Diode peak inverse voltage is 256V.

$C_{out} = 21.85\mu F.$

$I_{ripple} = 0.34A$

ESR must be less than 1.445Ω.

Snubber calculation:

$L_{l2} = 1.08\mu H$

$C_p = 100pF$

$F_r = 38.29MHz$

$R = 84\Omega$

C = 180nF

$$\text{Power loss} = \frac{L_{12} \times I^2_{secrms}}{2} \tag{3.46}$$

= 0.070308Watt

It also has emitter follower circuit in the secondary side. Zener clamps the voltage at 50V and wattage rating of the zener is 3Watt. And emitter follower circuit regulates the output voltage 50V. Calculations are shown below.

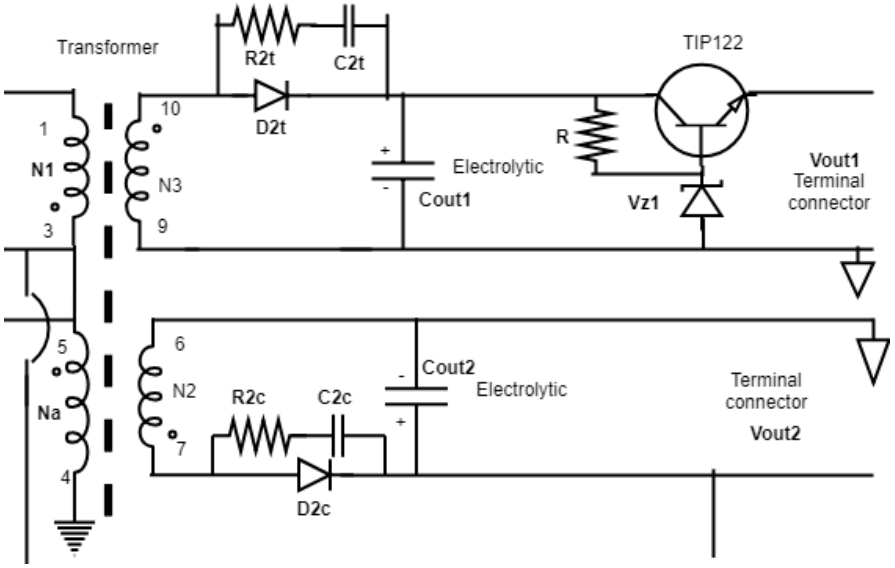

Fig. 3.7 Circuit diagram of Secondary side

$$I_{zener} = \frac{W_{zener}}{V_{zener}} \tag{3.47}$$

I_{zener} = 0.066A

$$R = \frac{V_{out} - V_{zener}}{I_z} \tag{3.48}$$

R = 282Ω.

3.7 Transformer design

This section includes selection of core and core material, calculation of wire gauge of primary, secondary and bias based on current density, skin effect and proximity effect. Calculation of core loss and copper loss. Measurement of the parasitic element of the transformer by bode 100 and precision LCR meter, simulation of transformer using Pexprt and comparison of theoretical, practical and simulated values.

3.7.1 Theory of Flyback transformer

Most important part in flyback topology is transformer. It decides efficiency, EMI, regulation. Even though it is called as transformer it is a coupled inductor. Generally in transformer when primary is conducting, secondary also has current flowing in it. But in flyback transformer when primary is conducting secondary side won't conduct. It stores energy in air-gap. Once the primary stops conducting polarity of primary changes, this changes polarity in secondary ad diode becomes forward biased. Then energy transfer occur. This property distinguishes from other transformer. Flyback transformer act like filter, gives isolation, energy storage and transfers energy to the secondary side. Dot in the transformer shows where the winding started. Winding strategy decides parasitic element.

3.8 Core selection

Ferrite core are generally used for SMPS design. Ferrite are black, brittle, hard and chemical inert. There are two types of ferrite soft ferrite and hard ferrite. Soft ferrites(which have low coercivity) are used in SMPS. General composition of ferrite is $(\underline{M}O)_m$-$(Fe2O3)_n$ where $\underline{M}$ represents transition metals. Most popular composition are MnZn and NiZn. NiZn has high resistivity suitable for application over 1MHz. MnZn has higher permeability and suitable for application below 1MHz. In this project N87(manufacturer EPCOS) which has MnZn as base material is selected. Core shape also play a important role. Core and bobbin should be chose based on system requirement such as physical height, weight, number of outputs and cost. Table 3.3 gives idea about how to choose core shape. In this project E core has taken because of its low cost and tight coupling requirement[25].

TABLE 3.3 FEATURES OF DIFFERENT CORES

Core Type	Features
EE, EI	Low cost, tight coupling
EFD, EFC	Low profile
EER	Large winding area, suitable for multiple output
PQ	Large cross sectional area and expensive
ETD	Suitable for high power

Selecting core size is not easy talk because there are many variables. Some magnetic manufactures give guidelines how to select core size based on the system requirement. In this project area product formula used which is given by equation 3.49.

$$A_p = A_w \times A_e = \left(\frac{P_{out}}{0.014 \times \Delta B \times F_{sw}}\right)^{\frac{4}{3}} cm^4 \quad (3.49)$$

$A_p = 0.05856 cm^4$

Or by core geometry approach selection of core size can be done.

First calculation of electrical condition, K_e.

$$K_e = 0.145 \times P_{out} \times B_m{}^2 \times 10^{-4} \quad (3.50)$$

$K_e = 0.261 \times 10^{-4}$

Then core geometry can be found out by equation 3.51.

$$K_g = \frac{Energy^2}{(K_e \times \alpha)} \quad (3.51)$$

Where α is regulation.

$K_g = 0.06850\ cm^5$.

Even though these are rough estimate. But it gives better picture how to select the core size. Based on above calculation E25/13/7 (Manufacturer EPCOS) is selected. Magnetics characteristics of E25/13/7 are listed below. Gapped core selected for energy storage.

A_e = cross-sectional area of the core = 52.5mm^2

A_w = Window area = 174mm^2

A_p = Actual area product = 0.09135cm^4

Mean path length = 57.5mm

Weight = 16g

Airgap = 0.25 ±0.02mm

A_L = Inductance factor = $\frac{L}{N^2}$

(3.52)

= 250nH

3.9 Transformer parameter calculation

Once the core is selected selection of wire plays an important role. Skin effect and proximity effect plays a major role. Skin effect can be reduced by selecting the proper wire size and proximity can mitigated if place the wire uniformly over the bobbin. Wire selection must also consider the current it carries. Calculations are shown below.

$$J = \frac{2 \times E \times 10^4}{(B_m \times A_p \times K_u)} \tag{3.53}$$

$J = 700 \frac{A}{cm^2}$

Once the current density is known we can calculate the area of the wire. Current flowing in primary already known from the previous calculation.

$$J = \frac{I}{A} \tag{3.54}$$

$A = 6.0428 \times 10^{-4} cm^2$

$$A = \frac{\pi \times D^2}{4} \tag{3.55}$$

D = 0.0277cm

Skin depth of the wire at 80KHz

$$S_d = \frac{6.62}{\sqrt{f}} \text{cm} \tag{3.56}$$

S_d = 0.0234cm

Inductance factor is already known. So number of turns on primary side is gven by equation 3.57.

$$A_L = \frac{L}{N^2} \tag{3.57}$$

N_{pri} = 48to get the proper turns ratio N_{pri} become 50.

Current density on the secondary must be same. Turns ratio is already known. By using these constraints we calculate the secondary number of turns and radius of the secondary wire.

For 30V and 0.1A

A = $1.484 \times 10^{-3} \text{cm}^2$

D = 0.0277cm = 0.277mm

N_{sec} = 16

For 50V and 0.5A

A = $5.14 \times 10^{-4} \text{cm}^2$

D = 0.0255cm = 0.255mm

N_{sec} = 26

For auxillary winding

A = $2.14 \times 10^{-5} \text{cm}^2$

D = 0.00529cm = 0.0529mm

N_{sec} = 8

Based on the Standard wire gauge Table 3.4 selection of proper wire gauge is made. It plays as important role in determining the losses[6].

TABLE 3.4 STANDARD WIRE GAUGE

SWG	inches	mm	SWG	inches	mm	SWG	inches	mm
7/0	0.500	12.700	13	0.092	2.337	32	0.0108	0.274
6/0	0.464	11.786	14	0.080	2.032	33	0.0100	0.254
5/0	0.432	10.973	15	0.072	1.829	34	0.0092	0.234
4/0	0.400	10.160	16	0.064	1.626	35	0.0084	0.213
3/0	0.372	9.449	17	0.056	1.422	36	0.0076	0.193
2/0	0.348	8.839	18	0.048	1.219	37	0.0068	0.173
1/0	0.324	8.236	19	0.040	1.016	38	0.006	0.152
1	0.300	7.620	20	0.036	0.914	39	0.0052	0.132
2	0.276	7.010	21	0.032	0.813	40	0.0048	0.122
3	0.252	6.401	22	0.028	0.711	41	0.0044	0.112
4	0.232	5.893	23	0.024	0.610	42	0.004	0.102
5	0.212	5.385	24	0.022	0.559	43	0.0036	0.091
6	0.192	4.877	25	0.020	0.508	44	0.0032	0.081
7	0.176	4.470	26	0.018	0.457	45	0.0028	0.071
8	0.160	4.064	27	0.0164	0.417	46	0.0024	0.061
9	0.144	3.658	28	0.0148	0.376	47	0.002	0.051
10	0.128	3.251	29	0.0136	0.345	48	0.0016	0.041
11	0.116	2.946	30	0.0124	0.315	49	0.0012	0.030
12	0.104	2.642	31	0.0116	0.295	50	0.001	0.025

So above calculation are summarized in Table 3.5.

TABLE 3.5 TRANSFORMER DETAILS

Type	Primary	$Seconadary_{30V}$	$Secondary_{50V}$	Bias
Turns	50	16	26	8
Diameter	0.277mm	0.438mm	0.255mm	0.05219mm
SWG	31	26	33	47

Now we need to cross check whether theses turns can be accommodate in window area of core. We need to calculate window utilization factor so that how much window area copper wire is actually utilizing. Window utilization factor (WUF) is multiplication of four factor.

$$K_u = S_1 \times S_2 \times S_3 \times S_4 \quad (3.58)$$

Where $S1 = \frac{\text{conductor area}}{\text{wire area}} = 0.8$

$S2 = \frac{\text{wound area}}{\text{usable window area}} = 0.78$

$S3 = \frac{\text{usable window area}}{\text{window area}} = 0.52$

$S4 = \frac{\text{usable window area}}{\text{window area + inssulation}} = 1$

$K_u = 0.33$

$$\text{Area} = ((\frac{N_{pri} \times \text{Wire}_{area}}{WUF}) + (\frac{N_{sec30V} \times \text{Wire}_{area}}{WUF}) + (\frac{N_{sec50V} \times \text{Wire}_{area}}{WUF}) + (\frac{N_{bias} \times \text{Wire}_{area}}{WUF})) \times 2 \quad (3.59)$$

Area = $50mm^2$

Actual window area = $174mm^2$

So we can accommodate all the winding in the given window area.

3.10 Losses in Transformer

Every transformer has losses which is divided into two part one is copper loss another is core loss. Copper loss again divided into two type one is DC losses and AC losses. Calculation limited only for core loss and DC losses. AC losses are difficult to find. Even though AC losses are much more than DC losses[6].

Wire gauge is already known. By using equation 3.60 we can calculate the resistance of the wire.

$$R_p = MLT \times N_p \times (\frac{\mu\Omega}{cm}) \times 10^{-6} cm \quad (3.60)$$

Where MLT is mean length turn which is obtained from bobbin geometry which is equal to 3cm.

$R_P = 0.415\Omega$

$$R_S = MLT \times N_S \times (\frac{\mu\Omega}{cm}) \times 10^{-6} cm \quad (3.61)$$

For 30V output R_S = 0.1932Ω

For 50V output R_S = 0.291Ω

Bias winding resistance = 5.68Ω

$$Loss = I^2 \times R \quad (3.62)$$

Copper loss in primary winding = 0.375W

Copper loss in bias winding = 0.002272W

Total primary copper loss = 0.377W

Copper loss in secondary winding with output 30V = 0.2085W

Copper loss in secondary winding with output 50V = 0.1509W

Total secondary copper loss = 0.3594W

Total copper loss = 0.7364W

Field in the airgap is not be uniform. It bends at the edges. It is called fringing effect. Fig. 3.8 depicts fringing effect very well.

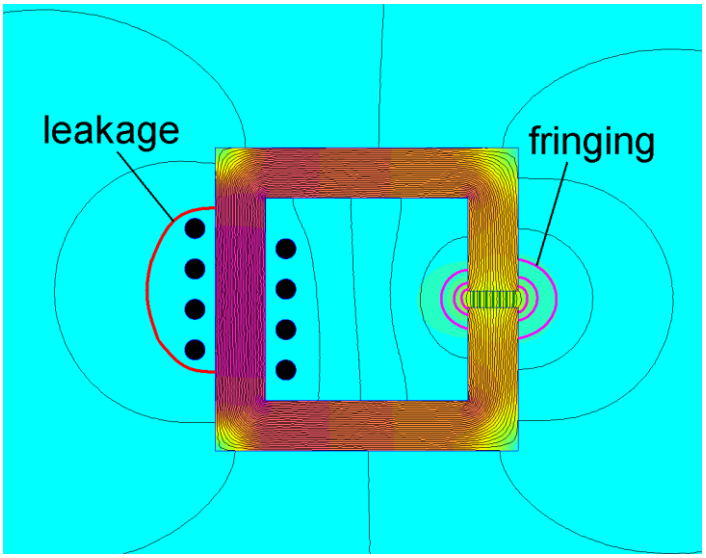

Fig. 3.8 Diagrammatic representation of fringing effect

Fringing factor need to be find in order to calculate magnetic field, B.

$$F_f = 1 + ((\frac{l_{gap}}{\sqrt{A_e}}) \times (\ln(\frac{2 \times W}{l_{gap}})) \quad (3.63)$$

Where W is length of the core window.

$F_f = 1.158$

$$B = \frac{(0.4 \times N_p \times F_f \times (\frac{I_{Peakpri}}{2}) \times 10^{-4}}{(l_{gap} + (\frac{MPL}{\mu}))} \quad (3.64)$$

MPL= .0575m and $\mu = 218$ are obtained from datasheet.

B = 2.37T

$$\frac{Watt}{Kg} = 4.855 \times 10^{-5} \times f^{1.62} \times B^{2.62} \quad (3.65)$$

$$\frac{Milliwatt}{Gram} = 40.835$$

$$Coreloss = (\frac{mW}{Gram}) \times Weight_{core} \times 10^{-3} \quad (3.66)$$

Core loss = 0.635W

$$Watt_{Density} = \frac{Powerloss}{Surfacearea} \quad (3.67)$$

$$Watt_{Density} = 0.0110 \frac{Watt}{mm^2} \quad (3.68)$$

$$T_{rise} = 450 \times (Watt_{Density}^{0.826}) \quad (3.69)$$

$$T_{rise} = 10.8 \frac{C}{Watt} \quad (3.70)$$

Total loss = Copper loss + Core loss

Total loss = 1.3714W

3.11 Transformer construction

Transformer construction determines leakage inductance, parasitic capacitance. So in this project in order to reduce leakage inductance between two primary all the secondary windings and bias windings are inserted. Transformer is winded using transformer winding machine. Fig. 3.9 shows the picture of transformer winding machine. Fig. 3.11 the winding construction. And starting of the primary winding must be connected to the drain of the MOSFET in order to reduce $\frac{dv}{dt}$ noise. And wires are spread uniformly over the bobbin to reduce proximity effect. Fig. 3.12 shows pin details of transformer. Primary winding started from pin 3 and ended in pin1. Next secondary (output 30V) winding started from pin7 and pin 6. Secondary (output 50V) winding started from pin 10 to 9. Bias winding started from pin 5 ended at pin 4. All winding are done in clockwise direction. Fig. 3.12, Fig. 3.13, Fig. 3.14, and Fig. 3.15 shows winding of the primary and secondary. Fig. 3.16 shows wires used for the winding.

Fig. 3.9 Transformer winding machine

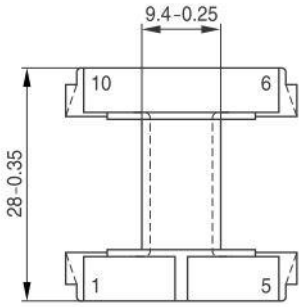

Fig. 3.10 Bobbin and transformer pin details

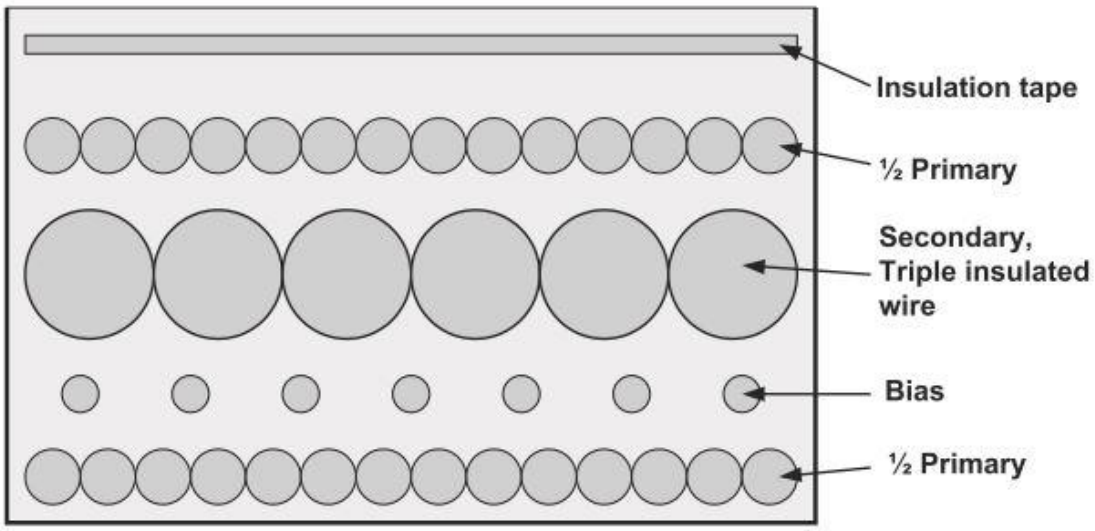

Fig. 3.11 Transformer winding method

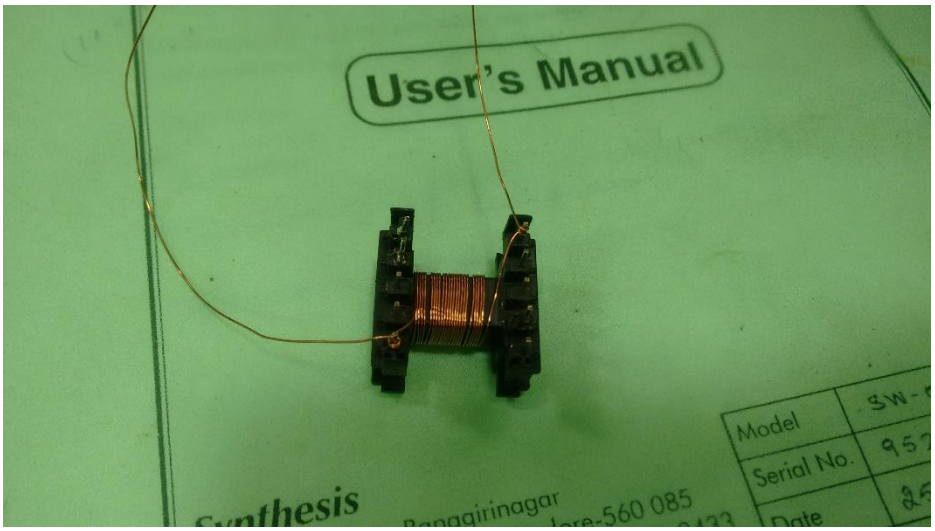

Fig. 3.12 Primary winding (25 Turns)

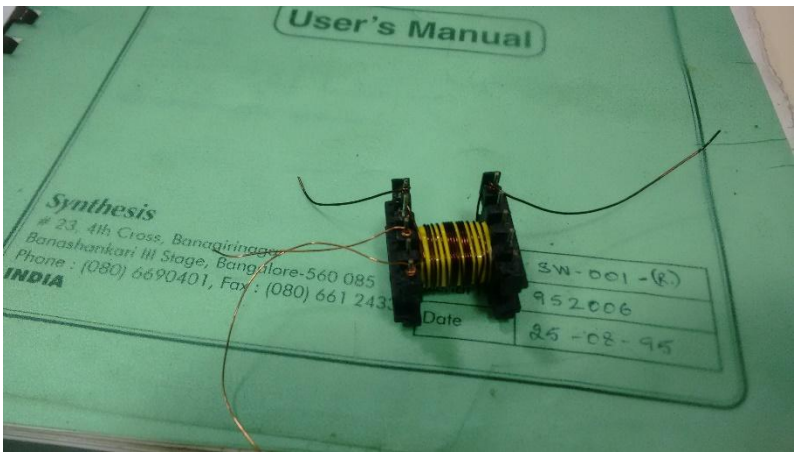

Fig. 3.13 Secondary winding with output 30V(16 turns)

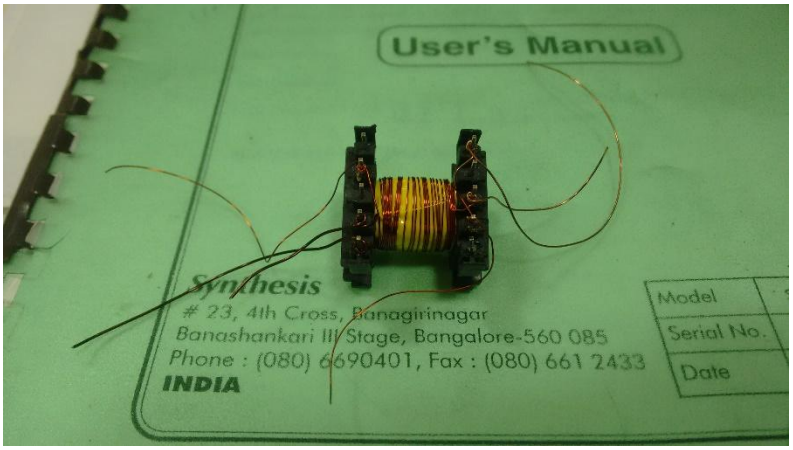

Fig. 3.14 Secondary winding with output 50V(26 Turns)

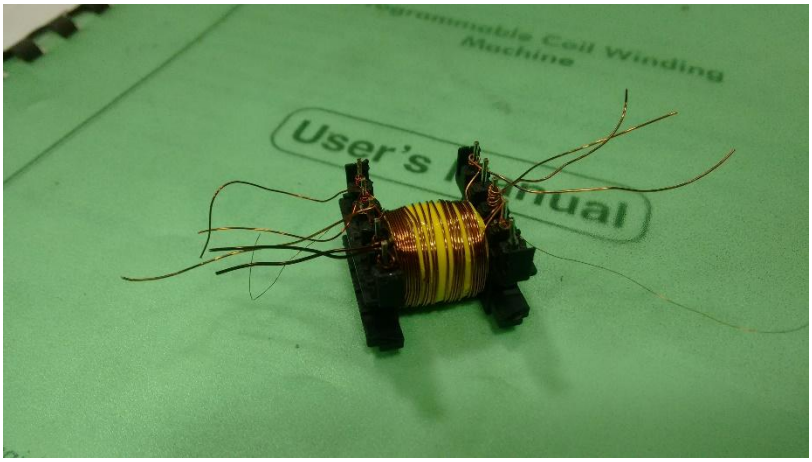

Fig. 3.15 Primary winding (25 Turns)

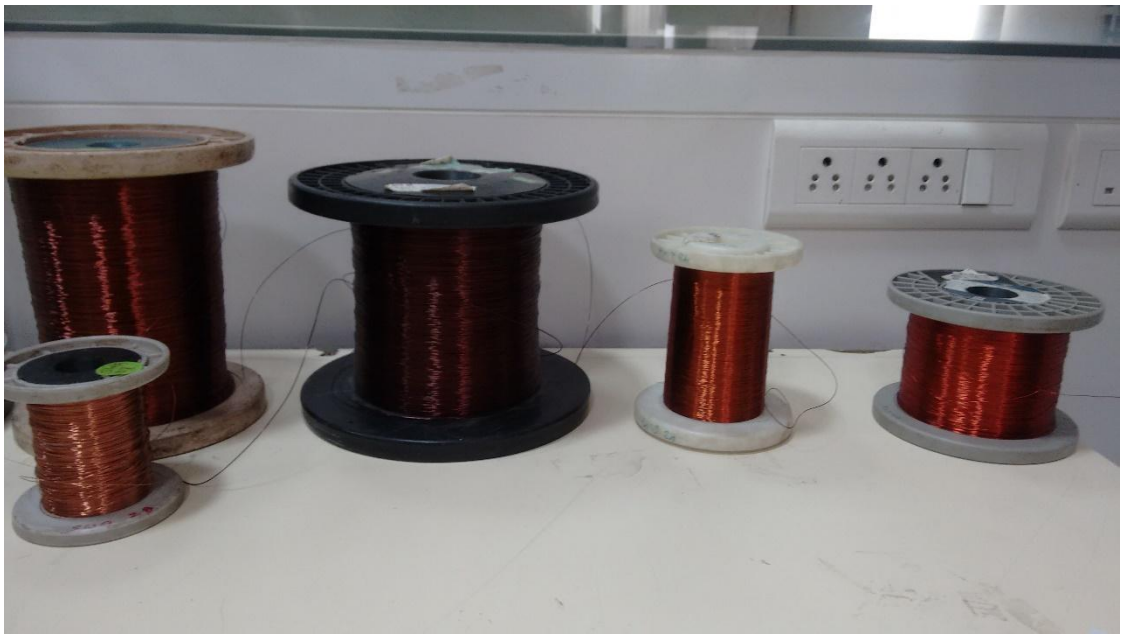

Fig. 3.16 Wires used to contruct transformer

3.12 Transformer Modelling

In order to calculate transformer parasitic element Bode 100 is used. Bode 100 is a USB controlled vector network analyzer. It produces frrequencies of different range from 1Hz to 50MHz with different gain values form -30dBm to 13dBm. It has one output and three input. Based on the requiremnt frequency must be set and gain by using the Bode 100 analyzer suite. Transformer frequency analysis is done by varying the frequencies from 10Hz to 1MHz by setting the proper gain value. Values are calculated at desired frequency. For example DC resistance measured at low frequency but leakage inductance and interwinding capacitance measured at 80KHz. Fig. 3.17 and 3.18 shows front and rear view of Bode 100.

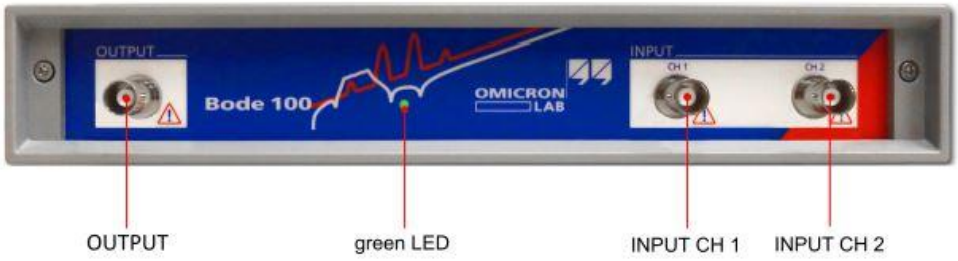

Fig. 3.17 Front view of Bode 100

Fig. 3.18 Rear view of Bode 100

Below are figures of measured resistance and inductance values. In the Fig.3.19, Fig. 3.20, Fig.3.21 resistance value started increse as the frequency increse because of skin effect and proximity effect. Fig. 3.22 and Fig.3.23 shows primary inductance and leakage inductance respectively. Fig. 3.24 and Fig.3.25 sows inter winding capacitance measured by precision LCR meter. And simulation of the transformer done using PExprt. Power Electronics Expert(PExprt) is an interactive, PC-based design tool that uses analytical expression to design magnetic components such as transformer and inductors.

Fig. 3.19 shows measurement of primary resitance whose value is 0.478Ω.

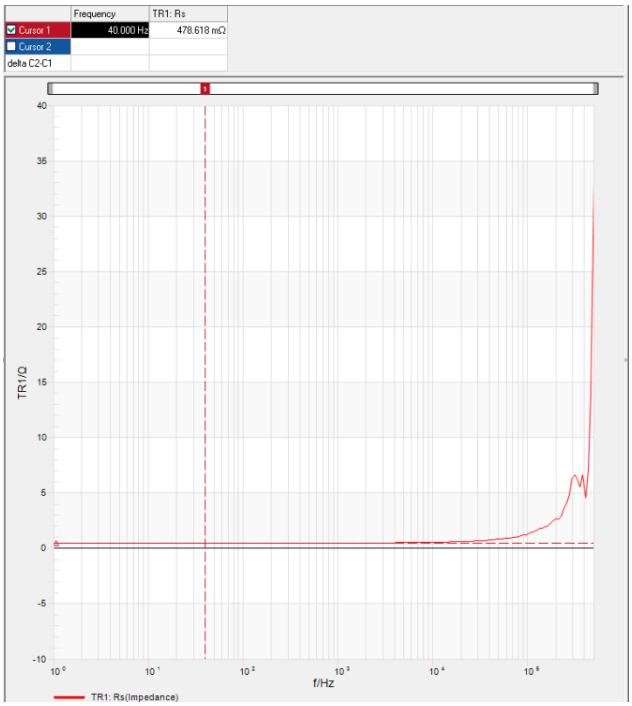

Fig. 3.19 Measurement of primary resitance

Fig. 3.20 shows measurement of secondary resintance with output 30V whose value is 0.199Ω.

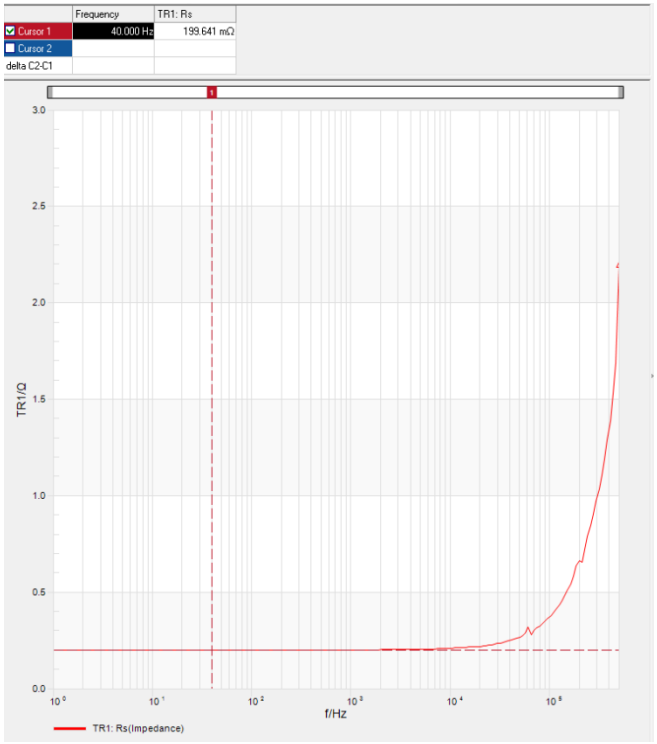

Fig. 3.20 Measurement of secondary resintance with output 30V

Fig. 3.21 shows measurement of secondary resintance with output 50V whose value is 0.509Ω.

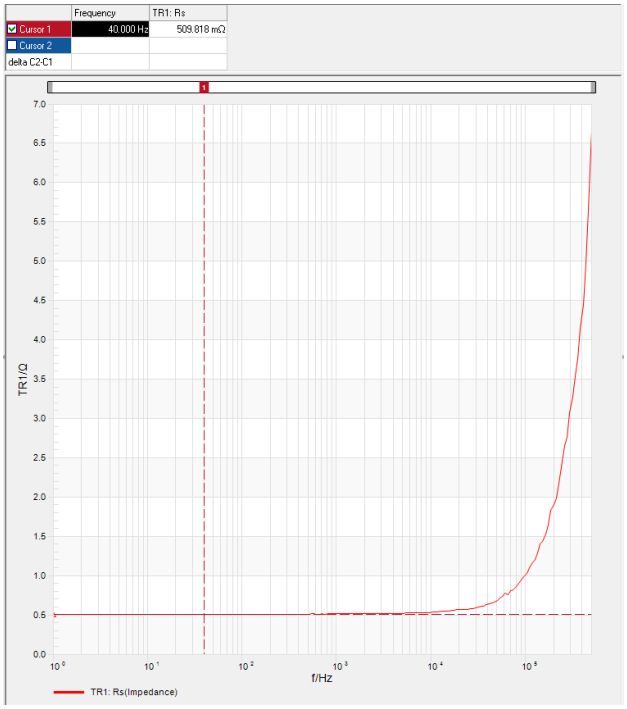

Fig. 3.21 Measurement of secondary resintance with output 50V

Fig. 3.22 shows measurement of primary inductance whose valueis 586μH.

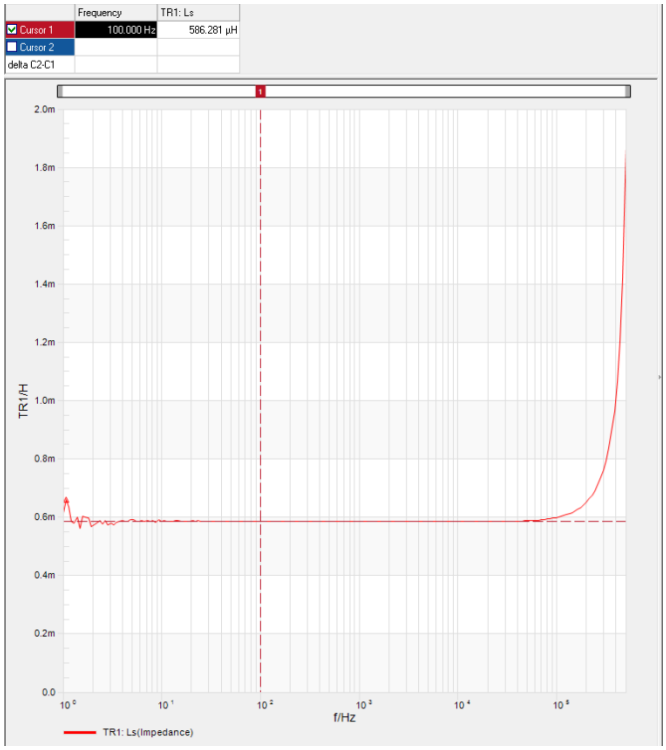

Fig. 3.22 Measurement of primary inductance

Fig. 3.23 shows measurement of leakge inductance whose value is 4µH.

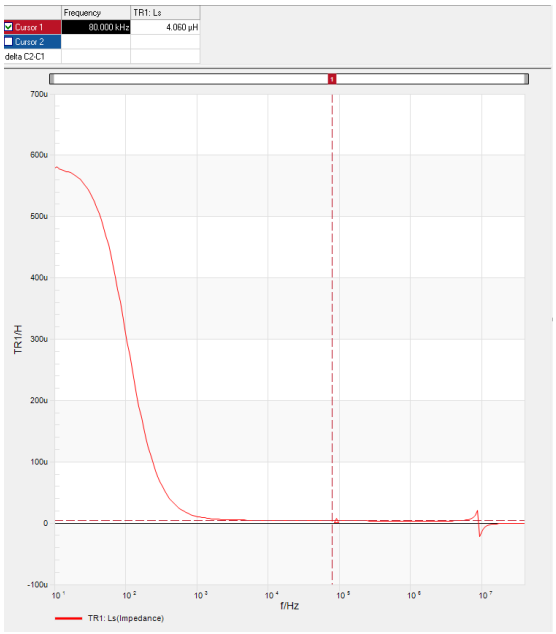

Fig. 3.23 Measurement of leakge inductance

Fig. 3.24 and Fig. 3.25 shows experimental setup for measurement of interwinding capacitance and value of interwinding capacitance is 49.43pF.

Fig. 3.24 Inter winding cpacitance measurement test setup.

Fig. 3.25 Measurement of interwinding capacitance

Fig. 3.26 shows simulation result of primary winding resistance whose value is 0.4Ω.

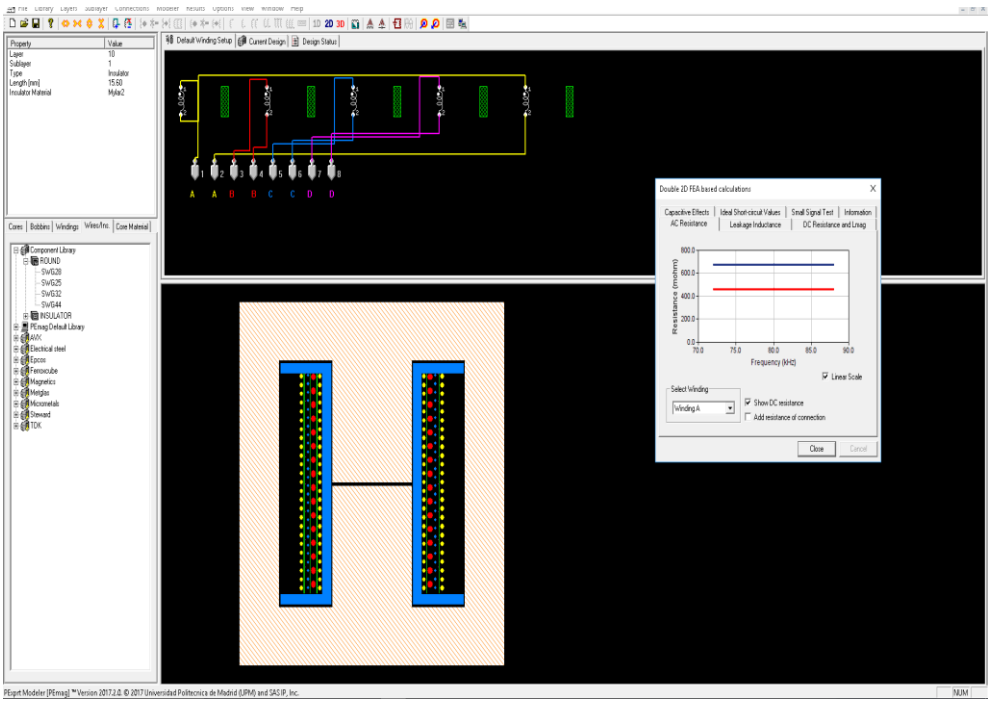

Fig. 3.26 Simulation result of primary winding resistance

Fig. 3.27 shows simulation result of leakage inductance whose value is 2.30µH.

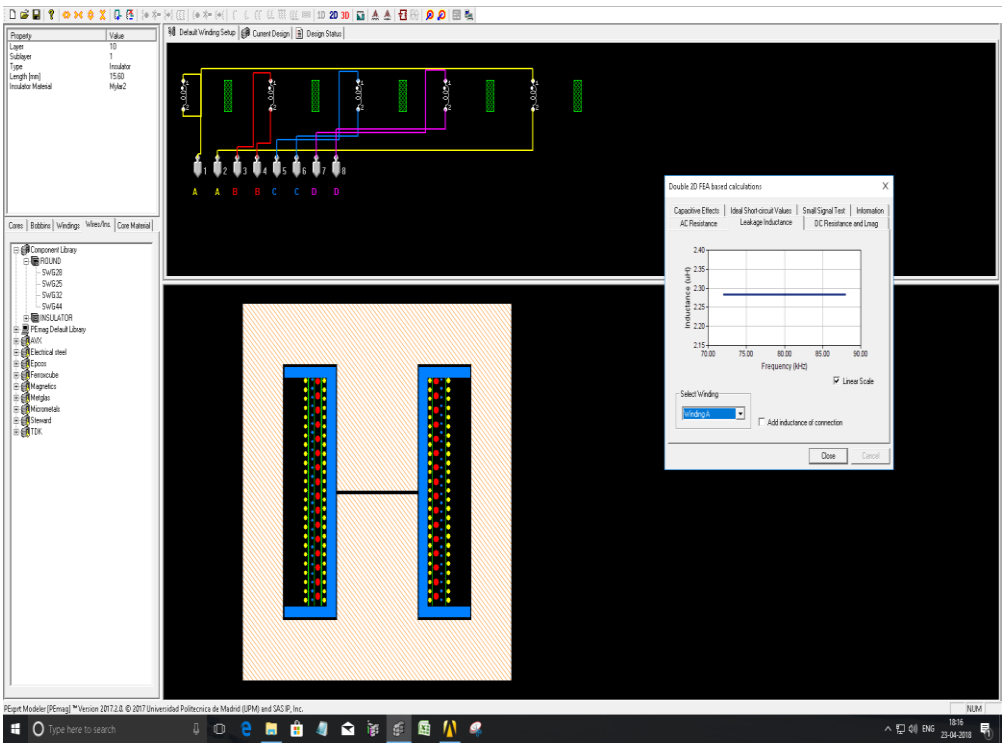

Fig. 3.27 Simulation result of leakge inductance

Fig. 3.28 shows simulation of interwinding capacitance and self capacitance whose values are 50pF and 3pF respectively.

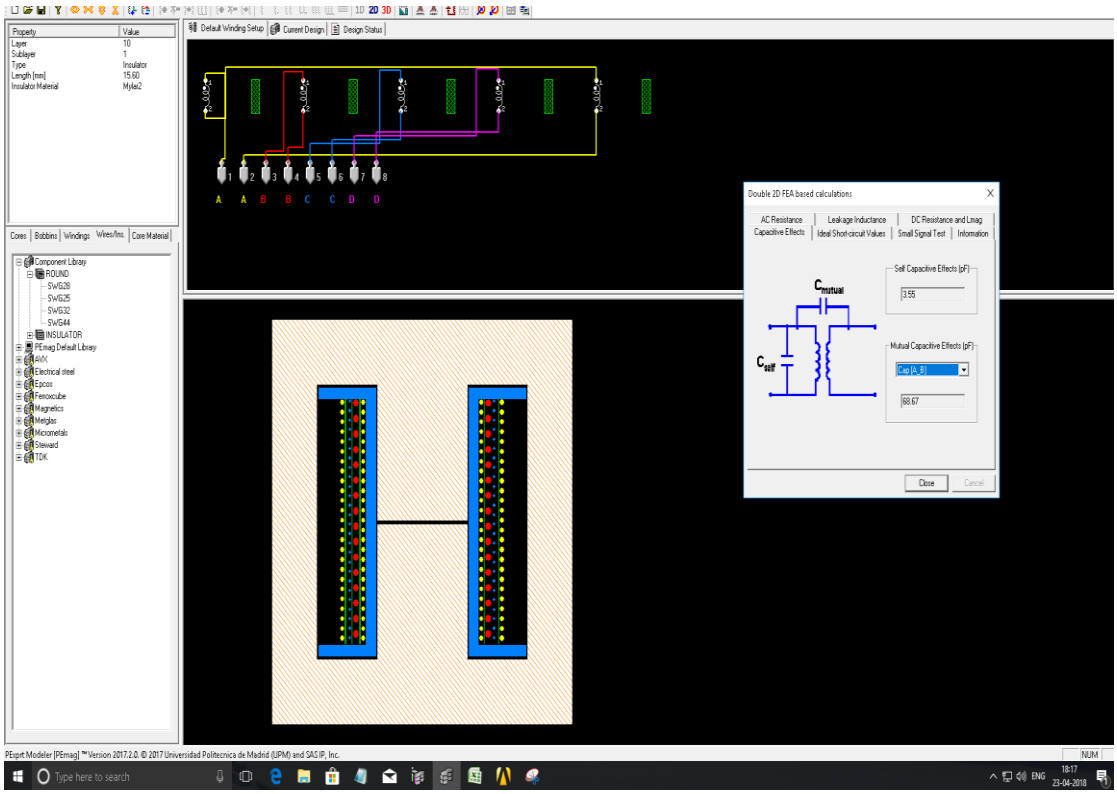

Fig. 3.28 Simulation result of interwinding capacitance and self capcitance

TABLE 3.6 COMAPRISION OF THEORITICL,PRACTICAL AND SIMULATION VALUES

Parameter	Theoritical	Practical	Simulation
Primary winding resistance	0.415Ω	0.478Ω	0.4Ω
Secondary winding (30V output) resistance	.199Ω	0.199Ω	0.1Ω
Secondary winding (30V output) resistance	0.291Ω	0.509Ω	0.2Ω
Primary inductance	570µH	586µH	570µH
Leakage inductance	-	4µH	2.30µH
Interwinding capacitance	-	49.43pF	50pF

CHAPTER 4

CONTROL LOOP DESIGN

This chapter explains closed loop stability of the power supply. It gives the detailed description about TL431, optocoupler, compensator design, how to get overall transfer function of the system. At the end it also bode plots of the transfer function.

4.1 TL431

TL431 three terminal adjustable shunt regulator which V_{REF} as 2.5V. It has good thermal stability. Output voltage can be set between 2.5V to 36V. In some application TL431 works beter than zener. Fig. 4.1 gives the pin detail. Fig. 4.2 shows how internal structure of TL431.In the diagram inverting pin connected to internal reference which is 2.5 V and non-inverting pin connected to output reference. Whenver reference voltage increases output voltage decreases because it is connected base of the transistor so its works like a opamp with negative feedback[24].

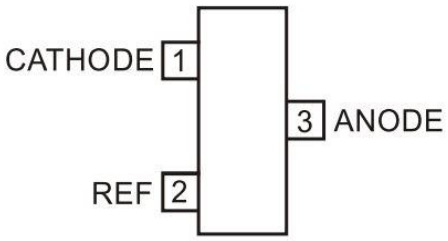

Fig. 4.1 TL431 top view SOT23 package

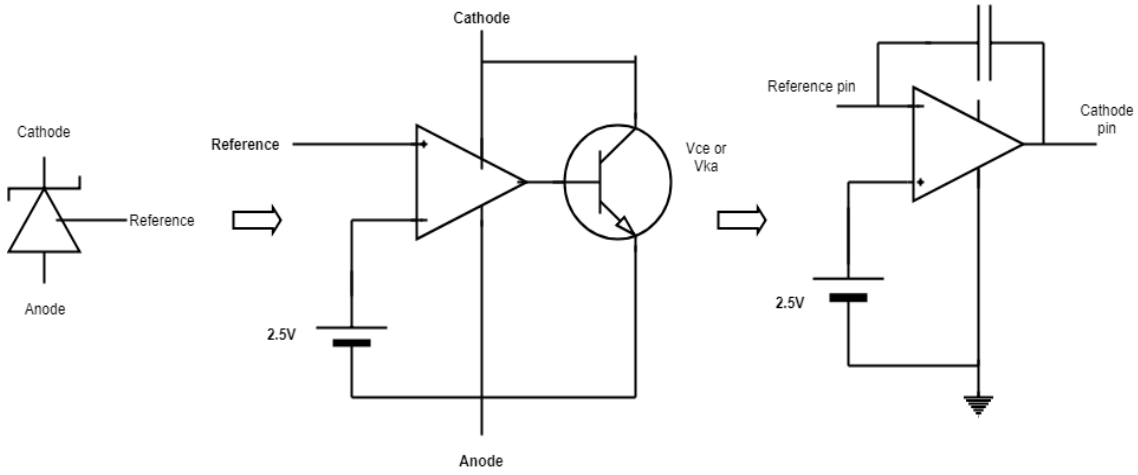

Fig. 4.2 TL431 internal structure

4.2 Type 2 Compensator

TL431 need compensation to give desired response. Type 2 give good transient response. V_{OUT} is compared with reference voltage and this goes to error amplifier. Error amplifier needed to give proper negative feedback. In this work optocouplar(VO615A) used to give proper feedback. Fig. 4.3 and Fig. 4.4 shows connection of type 2 compensator[10].

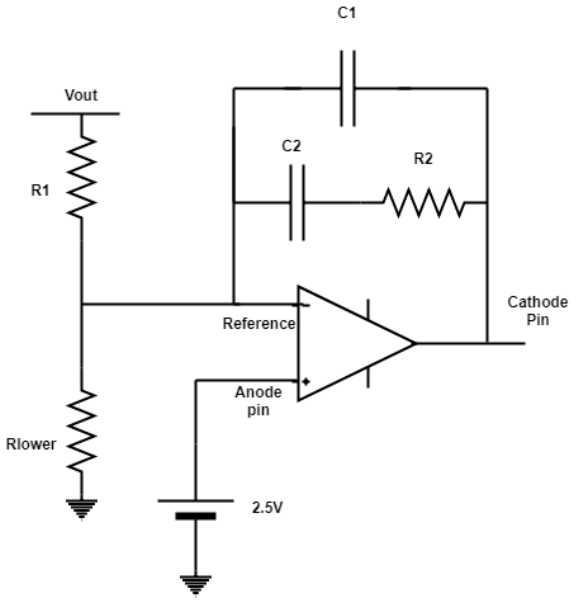

Fig. 4.3 Type2 compensator

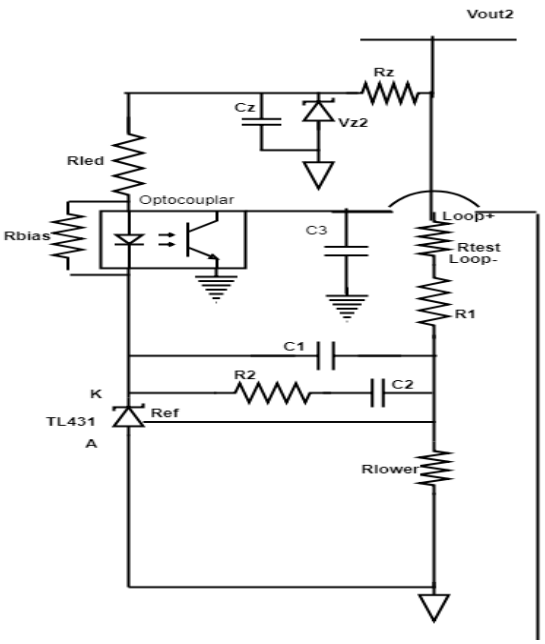

Fig. 4.4 Type2 compensator in actcual circuit

4.3 Calculation of transfer function

In this work UCC28600 IC is used and it operates in DCM mode. Small signal model is used in this work to obtain trasfe function of the whole system. It consists of three part.

- Duty production transfer function
- Filter circuit transfer function
- Compensation network transfer function

Duty production transfer function is given by equation 4.1

$$\frac{V_{comp}(s)}{I_s(s)} = \frac{5 \times R_{cs}}{\eta \times D} \tag{4.1}$$

Filter circuit tranfer function given by equation 4.2

$$\frac{V_o(s)}{i_s(s)} = \frac{(R_{01} + \frac{1}{sC_{out2}}) \times R_L}{R_L + (R_{01} + \frac{1}{sC_{out2}})} \tag{4.2}$$

Where R_L is load and R_{01} is equivalent series resistance of capacitor.

Open loop transfer function can be obtained by above two equations. Equation 4.3 gives open loop transfer function

$$\frac{V_o(s)}{V_{comp}(s)} = \frac{V_o(s)}{i_s(s)} \times \frac{i_s(s)}{V(s)} = \frac{(R_{01} + \frac{1}{sC_{out2}}) \times R_L}{R_L + (R_{01} + \frac{1}{sC_{out2}})} \times \frac{\eta \times D}{5 \times R_{cs}} \tag{4.3}$$

By substituting the values obtained from calculation we get below transfer function.

$$T = \frac{1.382 \times e^{-06} s^2 + 0.009545s}{1.168 \times e^{-05} s^2 + 0.00044s} \tag{4.4}$$

Compensator transfer function is given by equation

$$\frac{V_{comp}(s)}{V_o(s)} = -\left(\frac{sR_2C_2+1)}{sR_1C_2(sR_2C_1+1)}\right)\times\left(\frac{1}{1+sR_{pullup}(C_3+C_{opto})}\right)\times\frac{R_{pullup}\times CTR}{R_{LED}} \quad (4.5)$$

4.4 Calculation of compensator elements

$$T = \frac{1.382\times e^{-06}s^2 + 0.009545s}{1.168\times e^{-05}s^2 + 0.00044s} \quad (4.6)$$

Above transfer function has zero at 38Hz and compensator must cancel it.

In order to get values of C_2, C_1, R_2 calculation of R_{LED} is important. R_{LED} plays important role. If R_{LED} value is very high TL431 can't work properly and also reduces signal dynamic feature.

$$R_{Led} = \frac{(V_{out} - V_f - V_{TL431min})\times(CTR\times R_{pullup})}{(V_{dd} - V_{CEsat} + (I_{Bias}\times CTR_{min}\times R_{pullup}))} \quad (4.7)$$

$R \leq 14.85K\Omega$

Assume R_{LOWER} value to be $3K\Omega$

$$2.5 = \frac{30\times R_{lower}}{(R_1 + R_{lower})} \quad (4.8)$$

$R_1 = 33.3K\Omega$

R_{LED} taken as $2K\Omega$.

From bode plot, in order to have crossover frequency of 3KHz, we need 18dB gain.

$$R_2 = \frac{(G_{mid}\times R_1\times R_{LED})}{(R_{pullup}\times CTR)} \quad (4.9)$$

$R_2 = 87.37K\Omega$

$$C_1 = \frac{1}{(2\times\pi\times F_{p1}\times R_2)} \quad (4.10)$$

$$C_2 = \frac{1}{(2\times\pi\times F_z\times R_2)} \quad (4.11)$$

$$C_3 = \frac{1}{(2 \times \pi \times F_{p2} \times R_{pullup})} \tag{4.12}$$

Zero frequency is compensate the open loop. One pole frequency determines the crossover frequency. Other pole frequency for attenuate high frequency noise. Below are the chosen values of zero and pole.

F_z= 38Hz

F_{p1}= 2KHz

F_{p2}= 40KHz

C_1= 1nF

C_2= 47nF

C_3= 198pF

4.5 MATLAB RESULTS

Fig. 4.5 gives the bode plot of filter circuit whose zero must be cancelled by compensator transfer function.

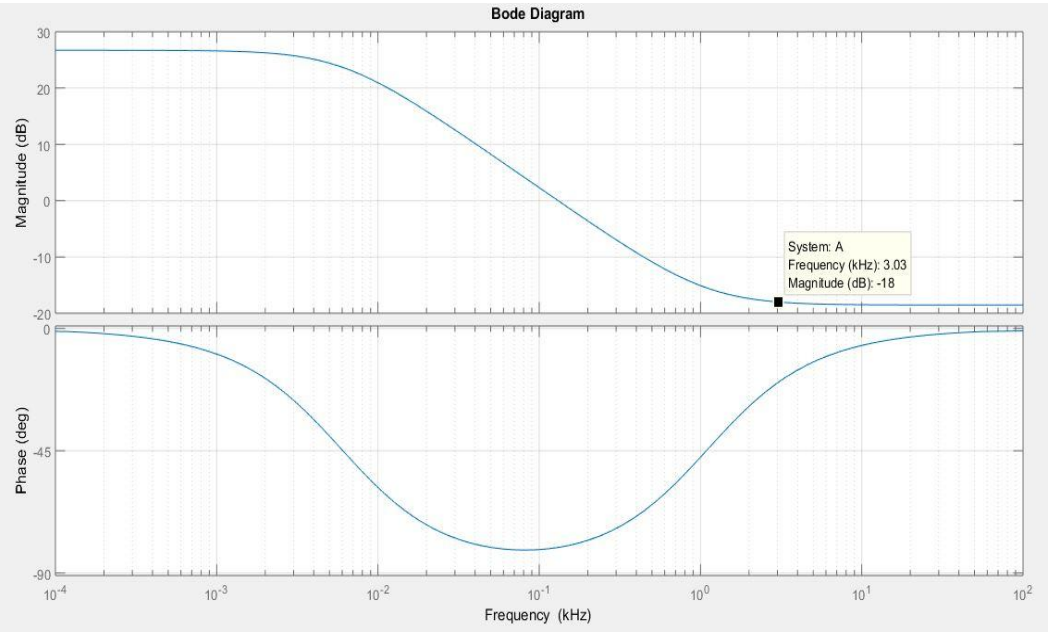

Fig. 4.5 Bode plot of filter circuit transfer function

Fig. 4.6 shows compensator transfer function which shows high cross over frequency which must be redued and phase margin must be increased.

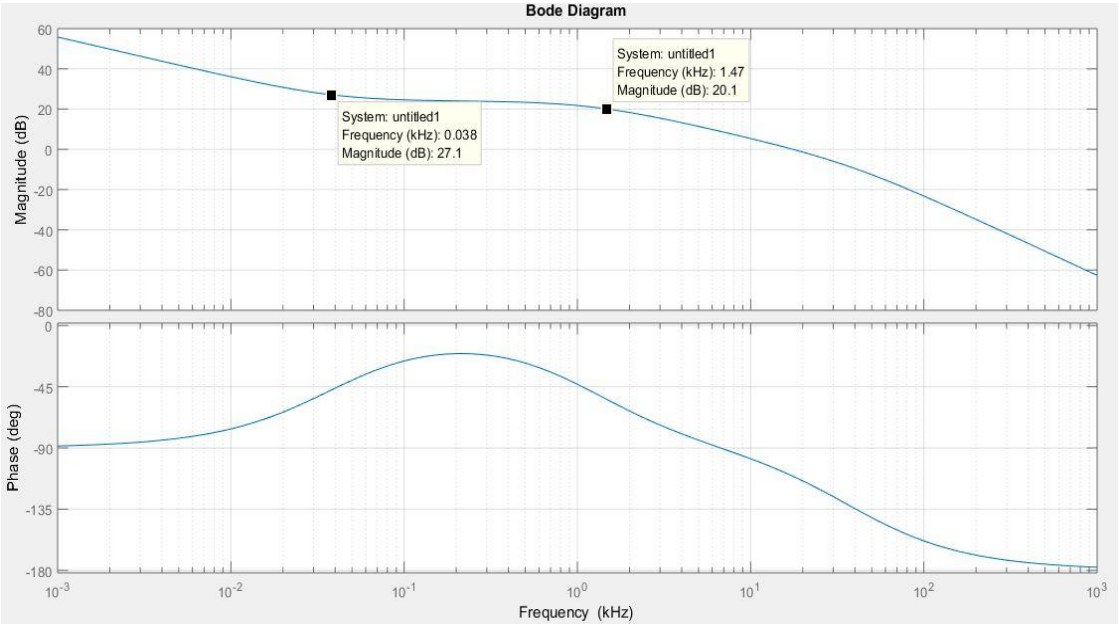

Fig. 4.6 Bode plot of comensator transfer function

Fig. 4.7 shows overall transfer function which has phase margin of 88.1 degree and cross over frequency of 2.23KHz. Gain margin is infinity so closed loop system is stable.

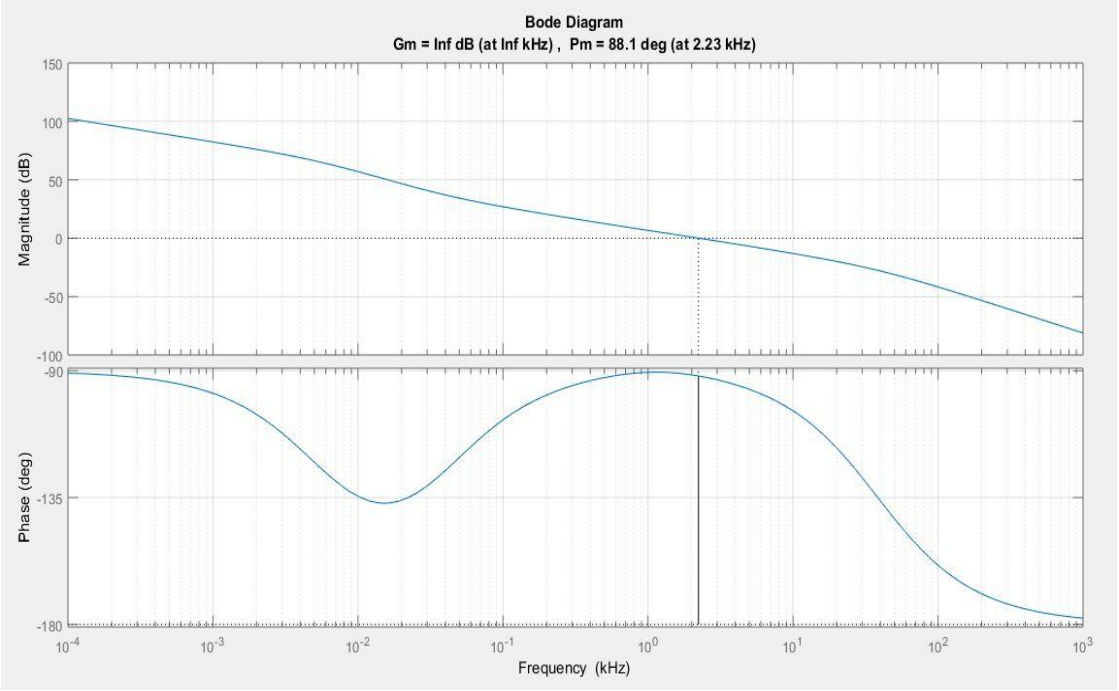

Fig. 4.7 Bode plot of system's transfer function

CHAPTER 5

HARDWARE IMPLEMENTATION

This chapter explains PCB designing, construction of the hardware, simulation results using TINA-TI. It also has waveform of snubber, rectifier output, reflected voltage, voltage across all pin of UCC28600 and output voltage. Thus, this chapter covers information about the performances of integrated system, cost and comparison between the proposed prototype and commercially available one.

5.1 PCB Design

PCB(Printed circuit board) design done using Altium software. Altium Designer is a PCB and electronic design automation software package for printed circuit boards. In this work double layer is constructed. Fig. 5.3 and 5.4 shows PCB top and bottom layer respectively. There are few consideration to be made before designing the PCB.

- Earth path must be smallest to eliminate noise.
- All components of near UCC28600 must have less trace.
- Snubber on both sides must be very near to the transformer.
- Drain pin must be close to the transformer.
- Feedback path must be very small.

And in order to separate primary and secondary side there must be small creepage distance. By considering all the above information PCB is designed. Before designing the PCB all the information of the components must be known. Using Altium software schematic of the circuit must be drawn. Once the schematic is done updating of the PCB done using the option. All the components must be placed on the board according to the creepage, clearance and based on system requirements. Creepage is the shortest distance along the surface of a insulating material between two conductive parts. Clearance is the shortest distance in air between two conducting parts. Once all the components are placed routing must be done. Once all the components are routed 3dimensional PCB can be seen by pressing 3. In order to fabricate PCB gerber file must be generated. Fig. 5.1 shows the schematic of the circuit. Fig. 5.2 shows PCB update from the schematic[11].

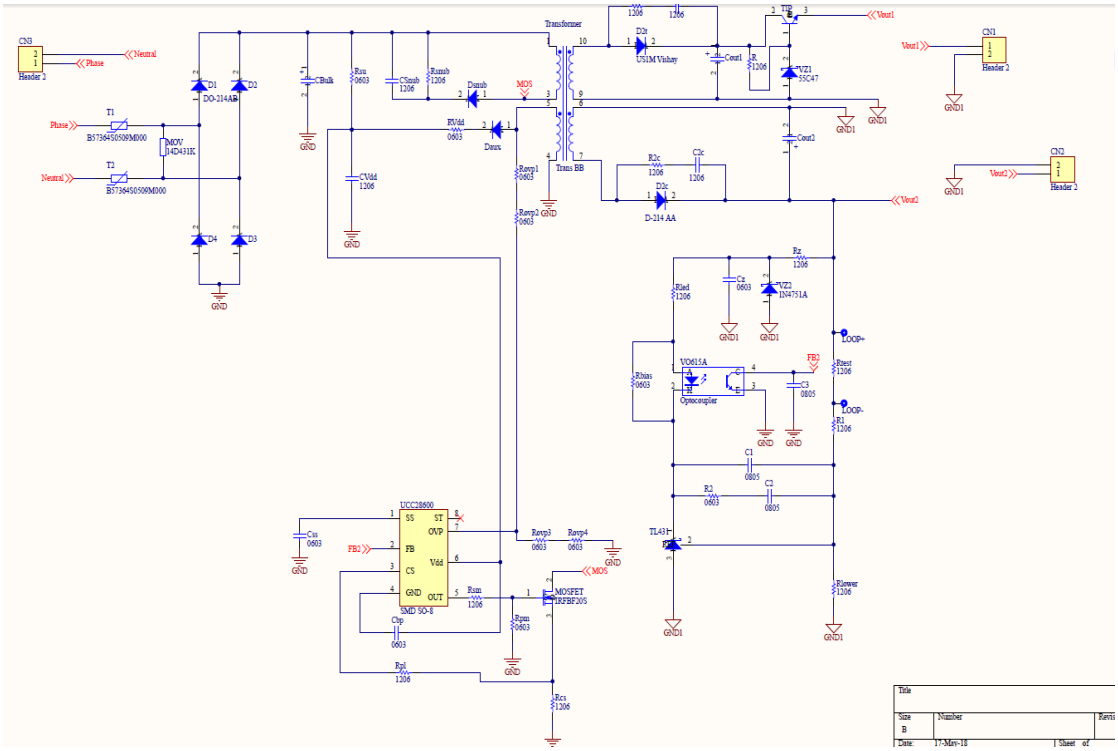

Fig. 5.1 Schematic of circuit diagram

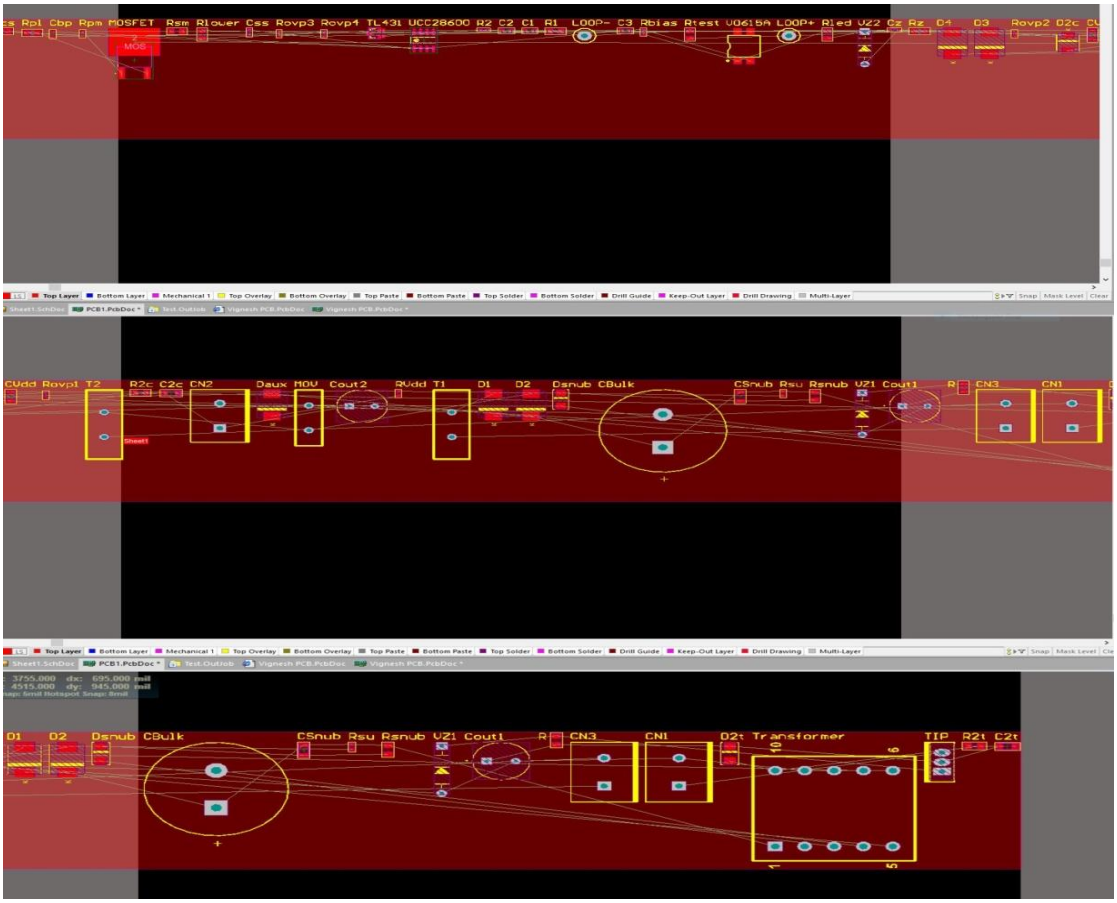

Fig. 5.2 PCB update

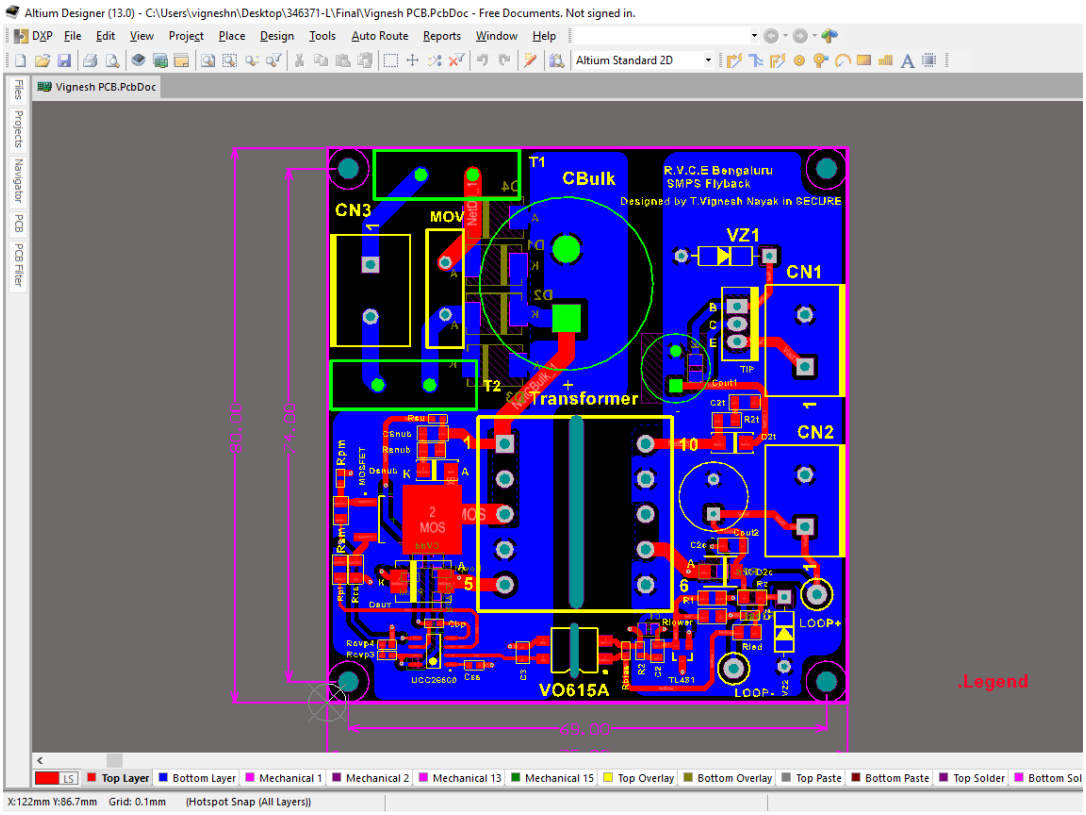

Fig. 5.3 PCB top layer

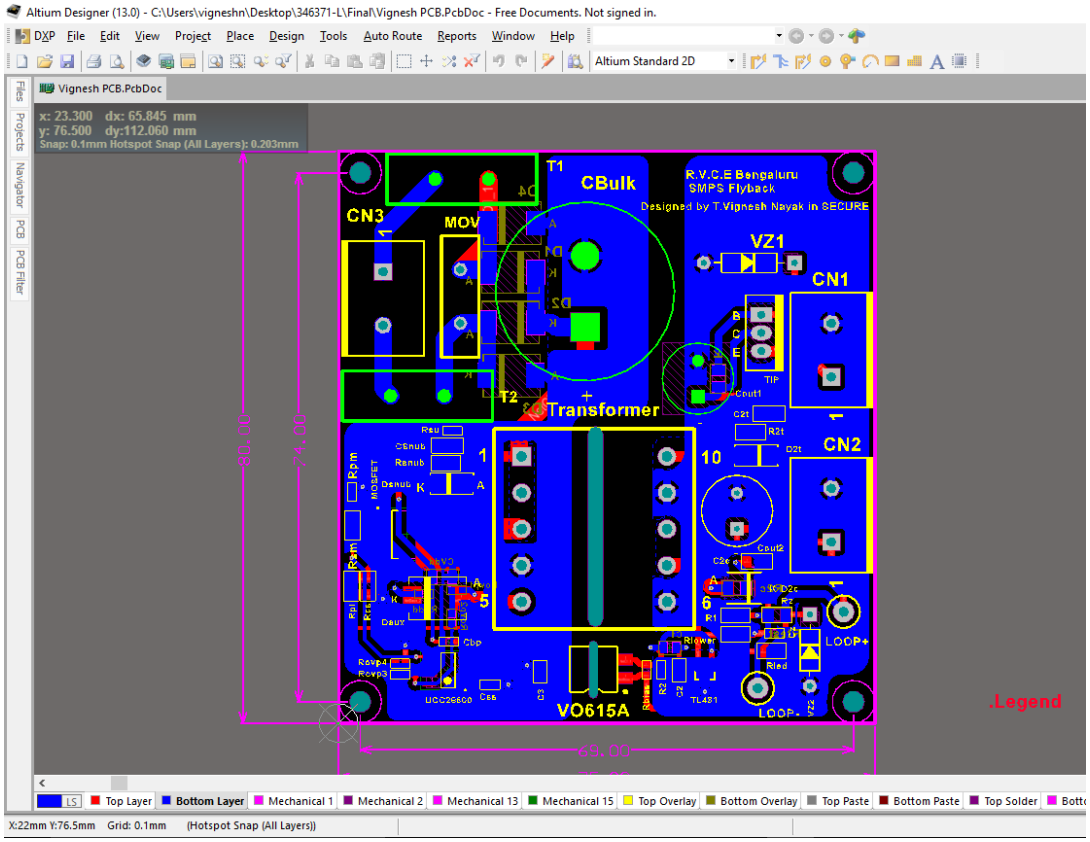

Fig. 5.4 PCB bottom layer

5.2 Simulation results using TINA- TI

TINA- TI is free software by Texas instrument to design and simulate analog circuits. Flyback converter is simulated using TINA-TI results are shown below. Fig. 5.5 shows circuit diagram of SMPS.

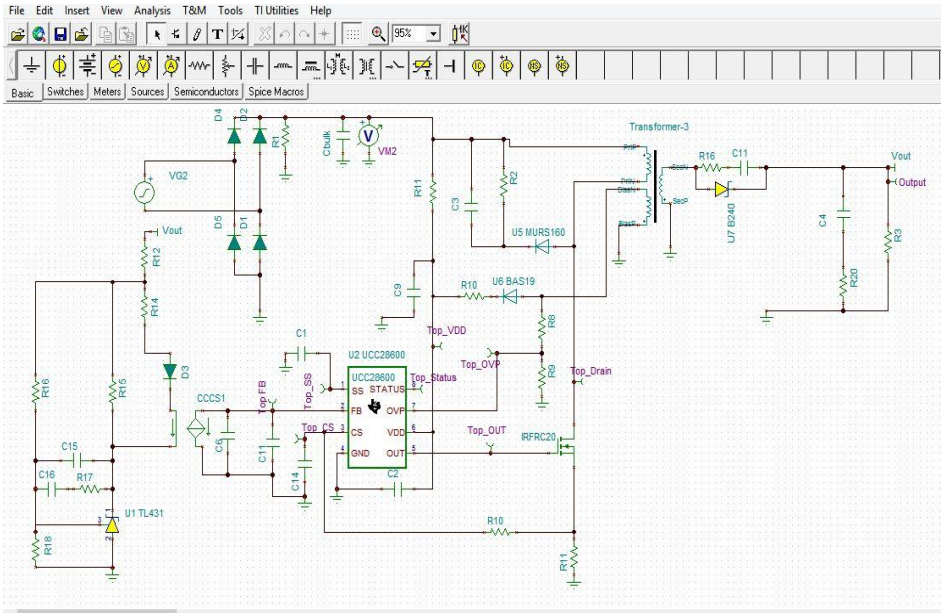

Fig. 5.5 Circuit diagram of SMPS Flyback converter

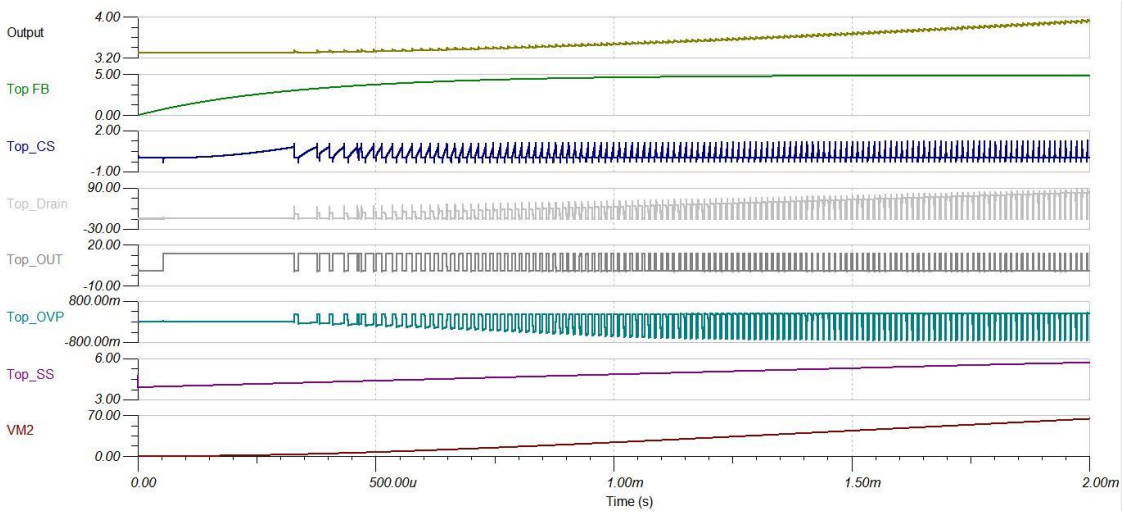

Fig. 5.6 Simulation results

Fig. 5.6 shows simulation results shows pulses at out pin, current sense pin, feedback pin and overvoltage protection pin for $85V_{AC}$ input. Soft start saturates at 6V. Output increases till desired output voltage. Drain pin have voltage of input and reflected voltage. VM_2 shows voltage at bulk capacitor.

5.3 Experimental setup

Experimental setup to implement flyback converter is shown in Fig.5.7 consists of

- Supply($85V_{AC}$ to $265V_{AC}$)
- Switched Mode Power Supply(SMPS)
- Digital storage oscilloscope
- Multimeter
- Multimeter probes
- Oscilloscope Probes
- Load

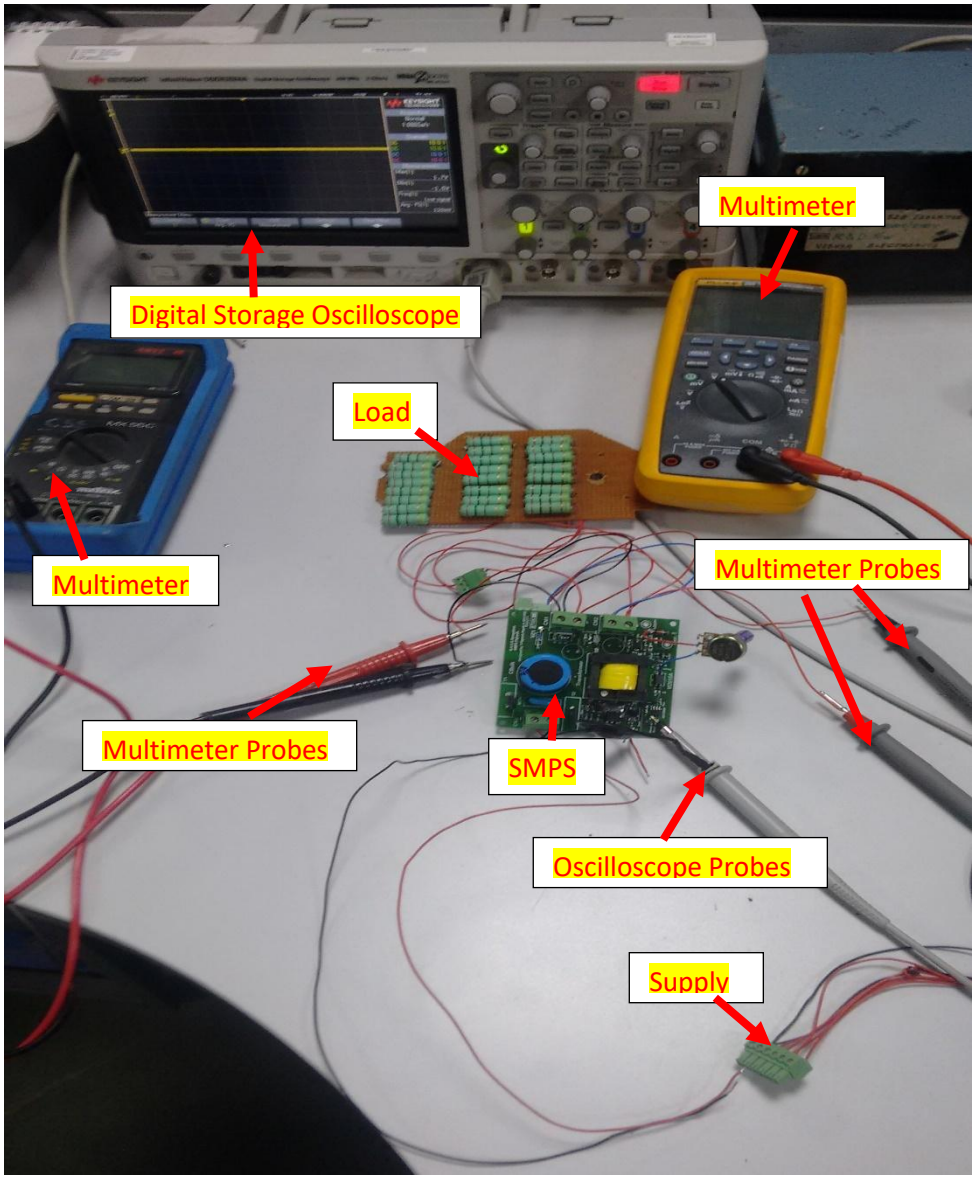

Fig. 5.7 Experimental setup for flyback converter

5.4 Results

Results include all the waveform, efficiency at every load and input condition.

5.4.1 Wave form of SMPS at 85V_{AC} input at lightly loaded condition

The waveform at drain and primary side snubber is shown in Fig. 5.8. At drain when MOSFET is in off condition voltage must be input plus reflected voltage.

Fig. 5.8 Waveform at Drain and snubber

Fig.5.9 shows 16V at IC's supply pin. Minimum supply needed for IC is 8V

Fig. 5.9 Waveform at supply pin of the IC

Fig.5.10 shows output waveform at transformer pin 7 which is 30V.

Fig. 5.10 Waveform at transformer pin 7

Fig. 5.11 shows output waveform at transformer pin 10 which is 50V.

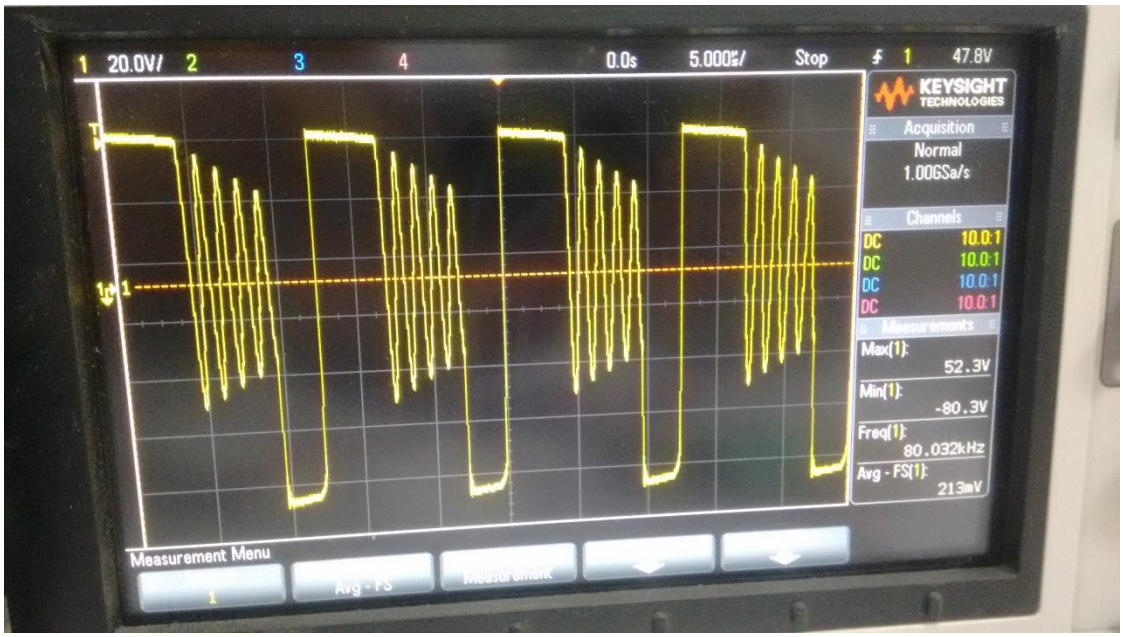

Fig. 5.11 Waveform at transformer pin 10

Table shows 5.1 shows efficiency at various loads, input voltages and ripple in each situation. Table 5.2 shows comparison between theoretical and practical value and table.

TABLE 5.1 EFFICIENCY OF SMPS AT VARIOUS LOAD AND INPUT CONDITION

Load Condition	Input $85V_{AC}$	Input $160V_{AC}$	Input $240V_{AC}$	Max Ripple at each condition
No Load	86% efficiency	87% efficiency	89% efficiency	3mV
Lightly Load	83% efficiency	86% efficiency	88% efficiency	1mV
Full load	80% efficiency	85% efficiency	87% efficiency	0.5mV

TABLE 5.2 COMPARISON BETWEEN THEORETICAL VALUE AND PRACTICAL VALUE

Parameter	Theoretical value	Measured value
IC supply	16V	16V
Tl431 reference	2.5V	2.5V
Transformer pin 7	30V	30V
Transformer pin 10	50V	50V

Fig. 5.12 shows how efficiency varies with various condition. Efficiency is difficult increase beyond 93% so based on the application tade off must be done.

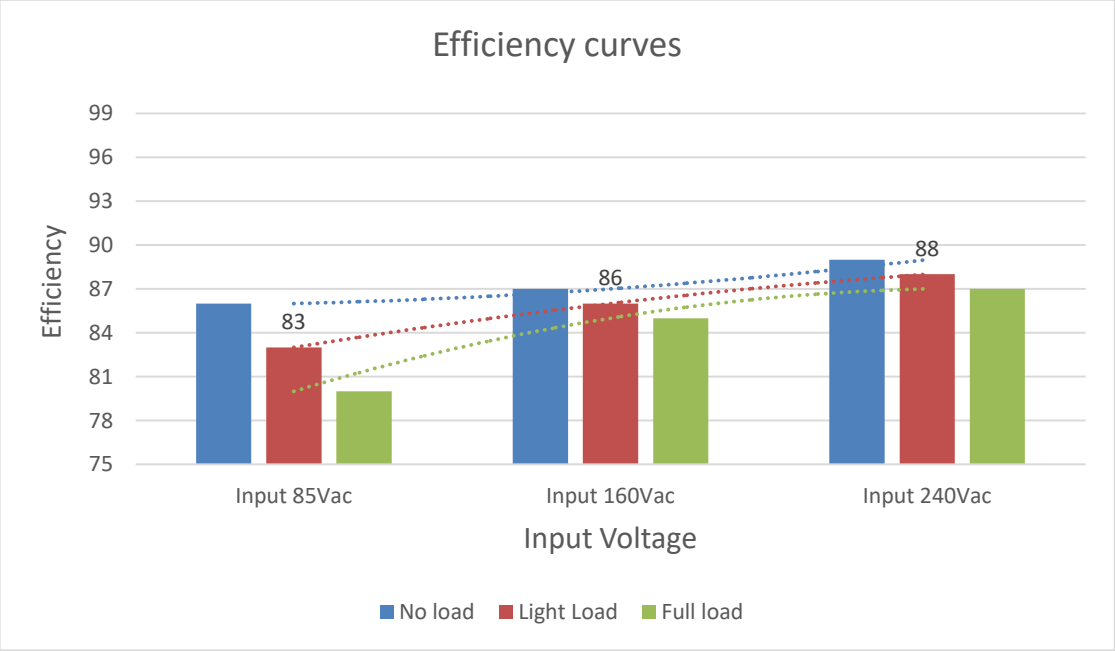

Fig. 5.12 Effciency curves of SMPS

Fig. 5.3 shows expenditure of the project to build 10 similar SMPS. So in mass production cost comes down to below 100Rs.

TABLE 5.3 COST ANALYSIS OF THE SMPS

Components and description	Quantity	Designation	Cost
Thermistor NTC, PTH molded disc, 5 ohm, 265 V, 4.2 A	2	T1 and T2	60
MOV,14D431K	1	MOV	20.39
iode general purpose, SMD SMC, If 5 A, PIV 2000 V,DO-214AB SM	5	D1,D2,D3,D4,Daux	115
Cbulk ,electrolytic,100uF 450V	1	Cbulk	50
Resistor SMD 0603, 4.7MΩ Ohm,	1	Rsu	4
SMD ULTA FAST RECTIFIER 1.0A 1000V	2	Dsnub and D2t	52
Capacitor ceramic, SMD 1206, 4.7 nF, +/-10%, 630 V dc	1	Csnub	10
Resistor SMD 1206, 120kΩ, +/-1%, 1/4W	1	Rsnub	4
Capacitor ceramic, SMD 1206, 1 uF, +/-10%, 50 V dc	1	Cvdd	10
Resistor SMD 1206, 48.32Ω, +/-1%, 1/4W	1	Rvdd	4
Capacitor ceramic, SMD 0603, 68 nF, +/-5%, 50 V dc	2	Cbp,Cz	20
UCC28600	1	UCC28600	40
IRFBF20S	1	MOSFET	80
Resistor SMD 1206, 1 Ohm, +/-1%, 1/4W	1	Rcs	4
Resistor SMD 1206, 10 Ohm, +/-5%, 1/4W	1	Rsm	4
TL431A SOT23 ADJUSTABLE PRECISION SHUNT REGULATOF	1	TL431	15
E 25/13/7 (EF 25) Ferrite core transformer	1	Transformer	100
Resistor SMD 0603, 10kOhm	1	Rpm	4
Resistor SMD 1206, 100 Ohm, +/-5%, 1/4W	2	R2c and R2t	8
DIODE SCHOTTKEY 2A D-214 AA ULTRA FAST	1	D2c	30
Cout capcitor,Electrolytic,470uF 50V	2	Cout1 and Cout2	25
Resistor SMD 0603, 120kΩ	1	Rovp1	4
Resistor SMD 0603, 33kΩ	1	Rovp3	4
Resistor SMD 0603, 3kΩ	1	Rovp4	4
Resistor SMD 0603, 12kΩ	1	Rovp2	4
Optocouplar VO165A,Vishay	1	Optocouplar	15
Capacitor ceramic, SMD 0805, 220 pF, +/-5%, 100 V dc	1	C3	10
Capacitor ceramic, SMD 0805, 100 pF, +/-5%, 50 V dc	1	C1	10
Capacitor ceramic, SMD 0805, 22 nF, +/-5%, 50 V dc	1	C2	10
Resistor SMD 1206, 2.7kΩ, +/-1%, 1/4W	3	Rpl,Rlower,Rled	12
Resistor SMD 0603, 1kΩ	1	Rbias	4
Resistor SMD 1206, 33kΩ, +/-1%, 1/4W	1	R1	4
TIP122,Transisitor	1	Tip	5
Resistor SMD 1206, 300Ω, +/-1%, 1/4W	1	R	4
55C47,Zener diode	1	Vz1	2
1N4751A ,zener	1	Vz2	2
Resistor SMD 0603, 55kΩ	1	R2	4
Resistor SMD 1206, 1000Ω, +/-1%, 1/4W	1	Rz	4
Capacitor ceramic, SMD 0603, 27 nF, +/-5%, 50 V dc	1	Css	10
Resistor SMD 1206, 10Ω, +/-1%, 1/4W	1	Rtest	4
Capacitor ceramic, SMD 0805, 100 nF, +/-5%, 100 V dc	2	C2t,C2c	16
	52	PCB	750
			1541.4

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

The proposed prototype is competitive in both performance and cost. However, there is still scope for improvisation. This chapter concludes this project and also discusses about areas which can be improvised further.

6.1 Conclusion

This project has three stages.

- Calculation of the component based on specification
- Transformer design
- PCB design and hardware implementation

Every power supply need to have high efficiency, long life and good performance. Switched mode power supply is the heart of any electric meter. In this project universal input is taken and it is shown that it can work satisfactorily in any condition. Every flyback converter has transformer which contributes more losses. In order to reduce losses sandwiched winding is done to reduce leakage inductance. Selection of proper wire gauges based on skin and proximity effect, in order to reduce the transformer losses. MOSFET switching losses reduced by using the quasi resonant mode operation. Selection of proper value of diode, resistor and capacitor in order to increase the efficiency. In this all the above mentioned points are implanted in order to increase the efficiency.

To get better dynamic response type 2 compensator is used. Ripple is reduced. PCB design is done based on the consideration of parasitic and to reduce unwanted noise. For all condition from light load to full load tight regulation is achieved by closed loop system and emitter follower configuration. In order to protect circuit from surges Metal Oxide Varistor(MOV) is connected parallel to the input. At the input side to limit inrush current two negative temperature coefficient(NTC) thermistor are applied. These above techniques increases the efficiency, achieve tight load regulation, less ripple and gives stable response.

6.2 Future Scope

The successful working of the proposed prototype has an efficiency of about 85%, is cost effective and competitive to its commercial counterparts and sustainable. But it still needs improvement.

The scopes of this project in the future are as follows.

1. Adding PFC circuit to the existing circuit in order to improve the power quality.
2. Reducing the standby power of SMPS to increase the efficiency at no load.
3. On the secondary side implementing synchronous rectifier efficiency can be increased further.
4. Four layer PCB design for reducing the emission and noise.
5. Implementing CCM, peak current reduces and efficiency can be increased.
6. Development of primary side sensing in order to reduce BoM.

6.3 Mapping of COs, POs, PSOs

Course Outcomes

- Successful understanding of literature review, work done in the field and problem definition.
- Successful implementation of a methodology using tools like PExprt, Altium and TINA- TI.
- Successful designing and developing the model and interpreting the desired results.
- Learnt preparing quality document of project work for publications, patenting and final thesis.

Design and Implementation of Flyback Converter														
POs and PSOs														
PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7	PO 8	PO 9	PO 10	PO 11	PO 12	PSO1	PSO2	PSO3
3	2	2	2	2	2	3	3	2	3	2	3	3	2	3

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APPENDIX

APPENDIX 1

MATLAB CODE

```
Rcs = 0.875;

D = 0.507;

n = 3.12;

RL = 60;

C = 440e-6;

Resr = 329e-3;

R2 = 87370;

C2 = 47e-9;

R1 = 33000;

C1 = 1500e-12;

Rpullup =20000;

C3 = 198e-12;

Copto = 10e-12;

Rled = 1000;

CTR =.3;

s = tf('s');
M =(n*D)/(5*Rcs);
A = (((M)*RL*(Resr+(1/(s*C))))/(RL+Resr+(1/(s*C))));
bode(A)
margin(A)
hold on
B=((s*R1*C2)*((s*R2*C1)+1))*(1+(s*Rpullup*(C3+Copto)))*Rled;
F = (((s*R2*C2)+1)*Rpullup*CTR);
bode(F/B)
margin(F/B)
hold on
H =(A*F)/B;
bode(H)
hold on
margin(H)
```

Flyback Converter

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