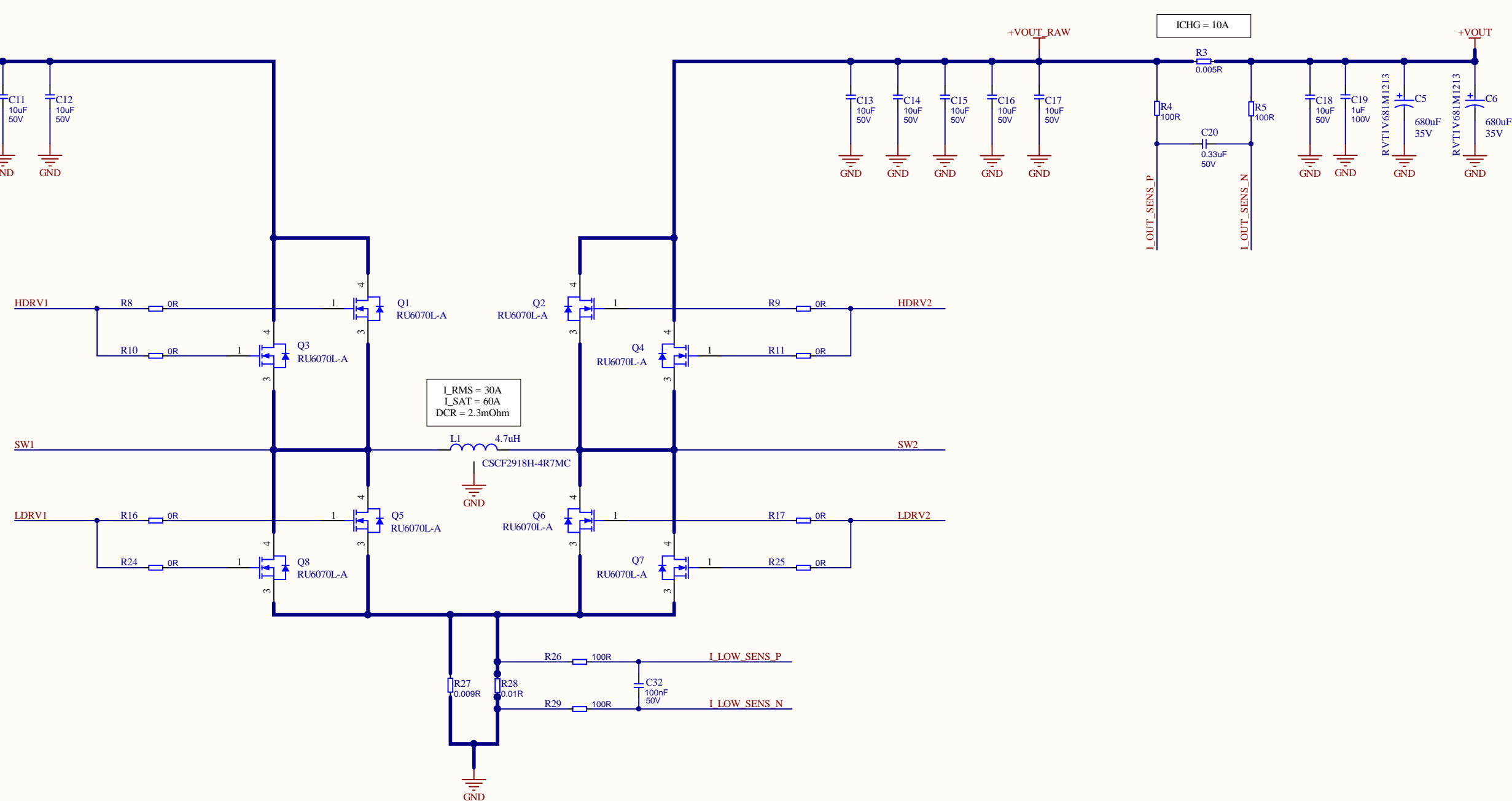
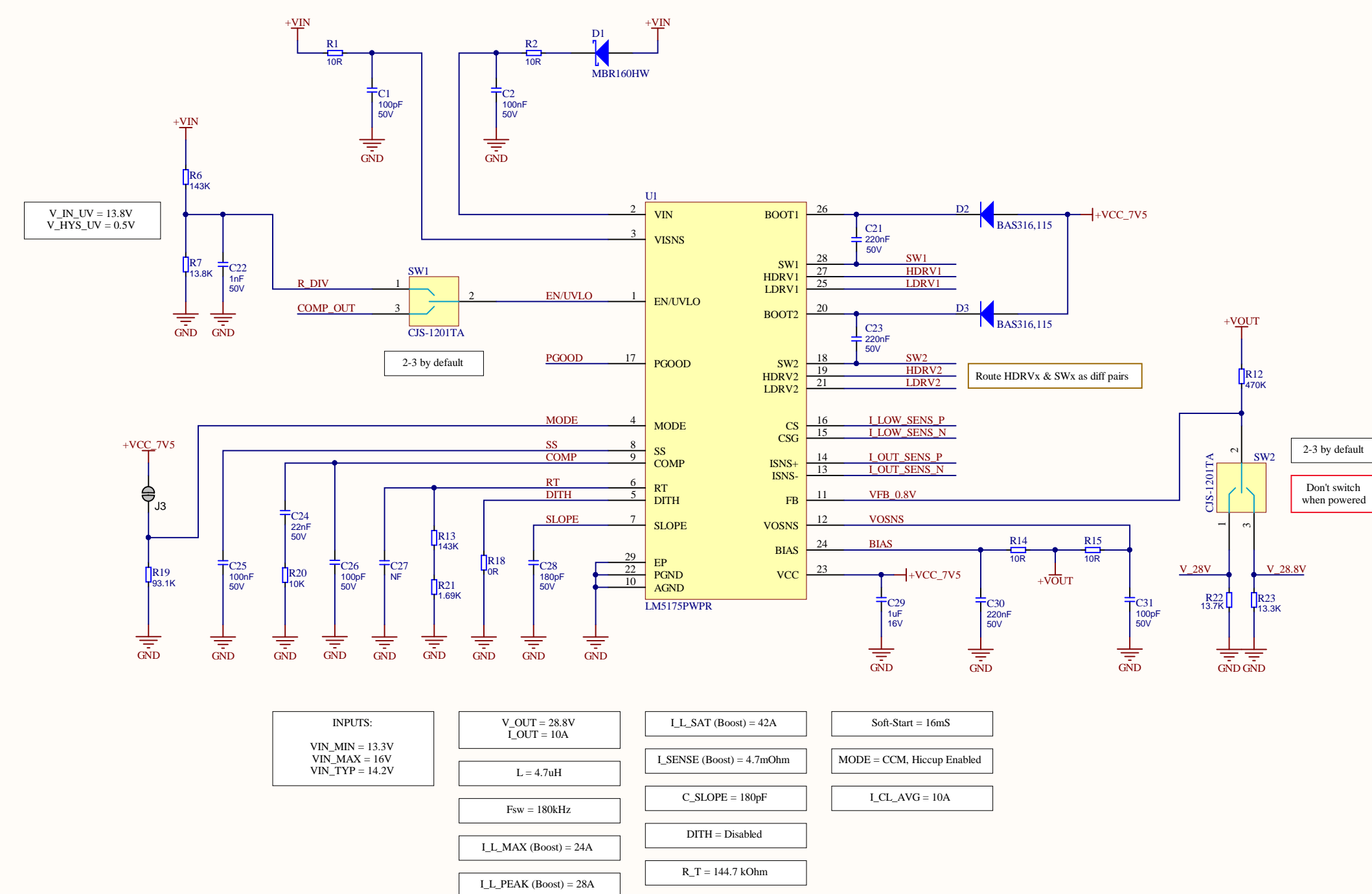


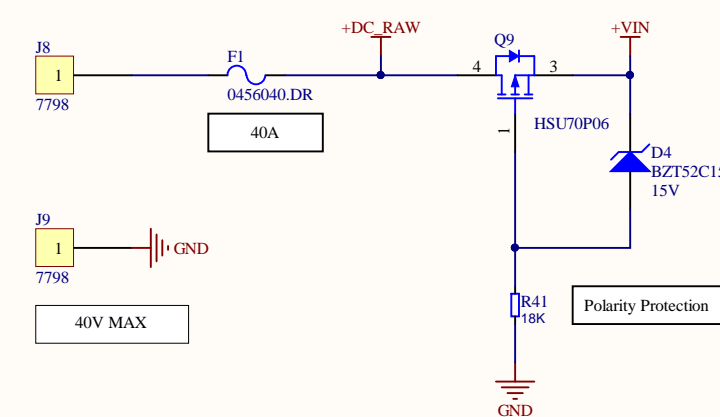
DC Charger REV1.1 - Schematic



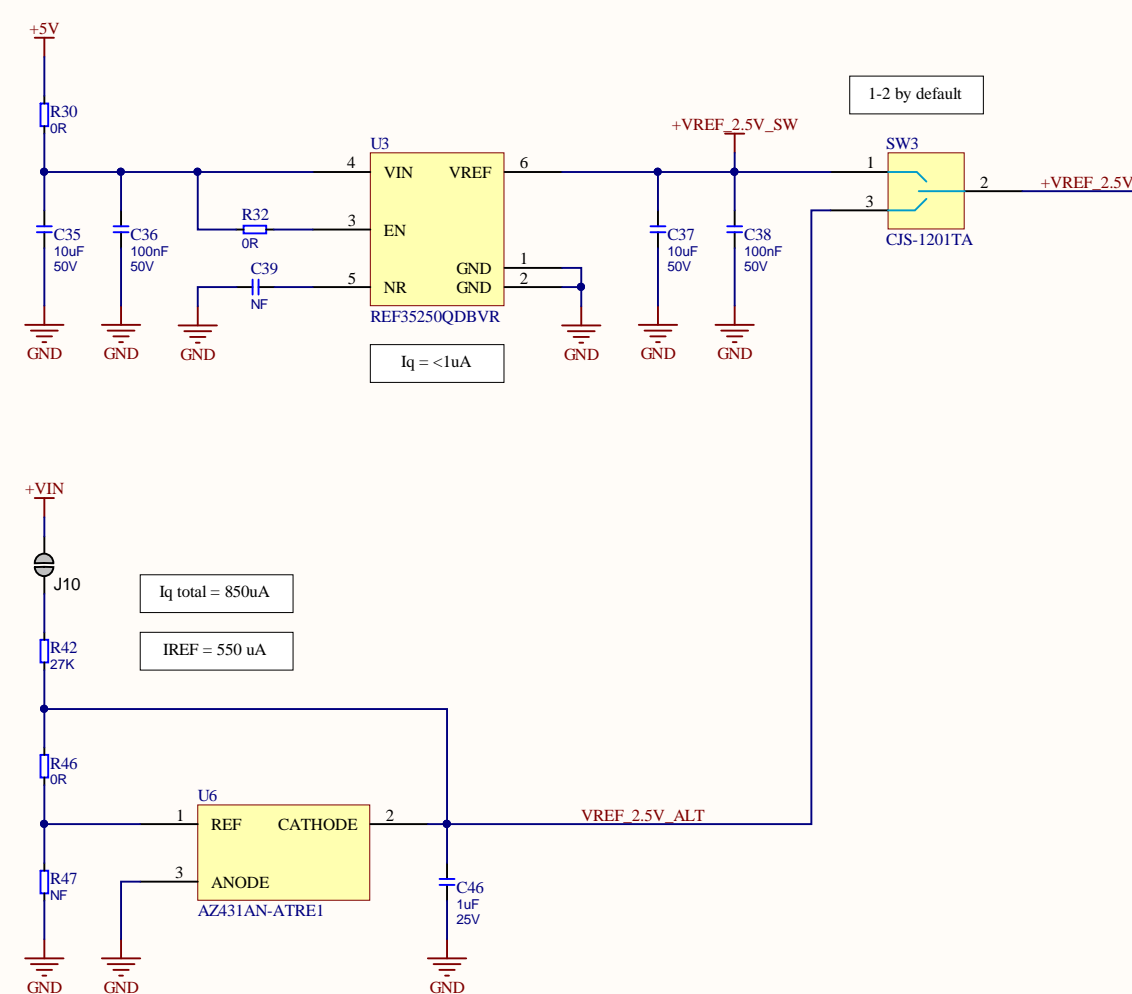
LDO (5V)



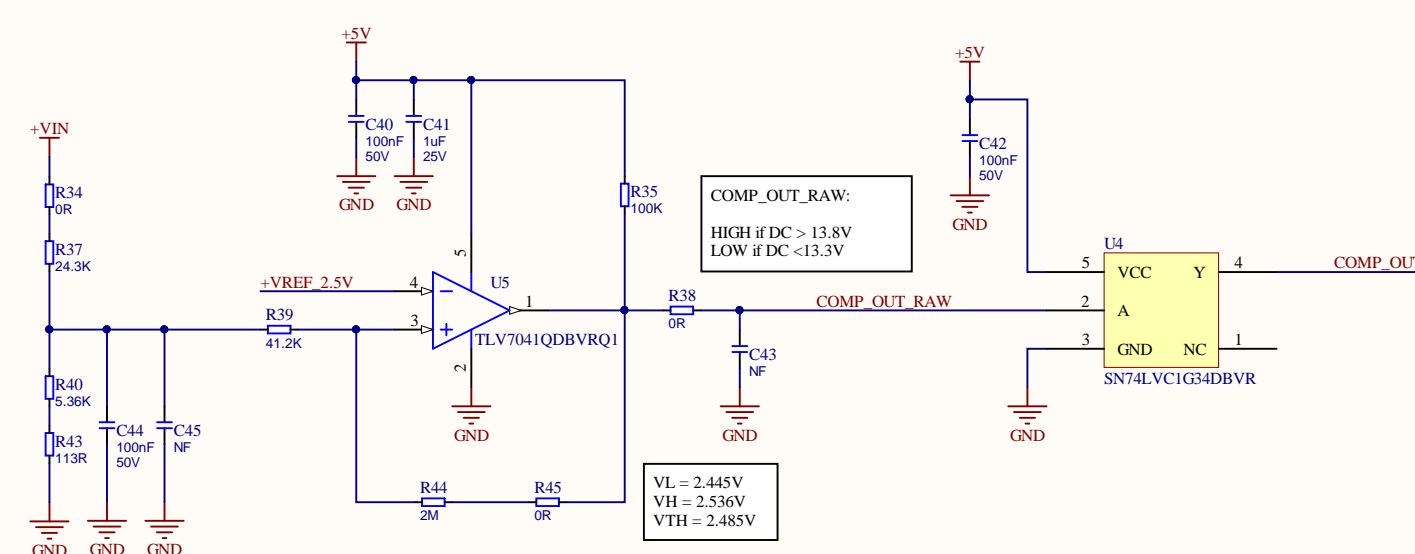
DC Input



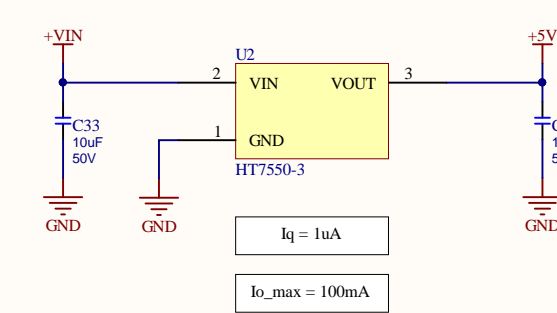
Ref. Voltage (2.5V)



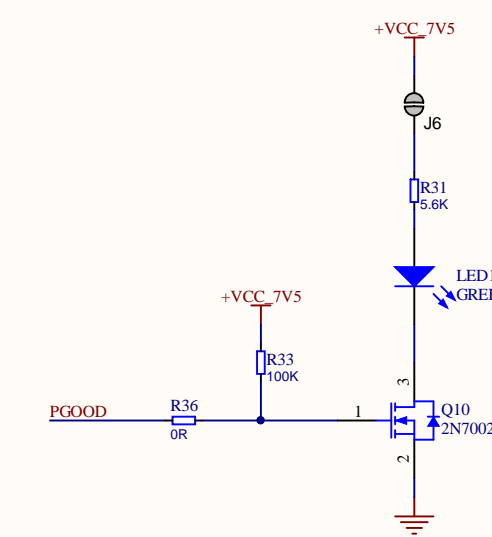
Comparator Sensing



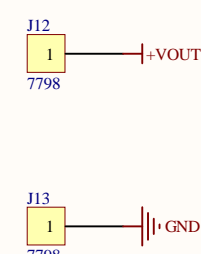
LDO (5V)



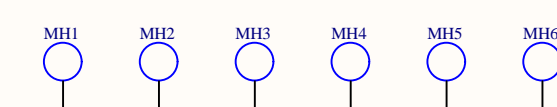
Debug



DC Output



Mounting Holes



-
- The diagram shows a vertical timeline with ten time points labeled TP1 through TP10. The signals and voltage levels are as follows:
- TP1:** SW1 (blue line)
 - TP2:** HDRV1 (blue line)
 - TP3:** LDRV1 (blue line)
 - TP4:** SW2 (blue line)
 - TP5:** HDRV2 (blue line)
 - TP6:** LDRV2 (blue line)
 - TP7:** +VCC_TV5 (blue line)
 - TP8:** +5V (blue line)
 - TP9:** +VREF_2.5V (blue line)
 - TP10:** EN_UVLO (blue line)