

8 Input Capacitor Selection

Similar to a boost converter, the SEPIC has an inductor at the input. Hence, the input current waveform is continuous and triangular. The inductor ensures that the input capacitor sees fairly low ripple currents. The RMS current in the input capacitor is given by:

$$I_{Cin\text{ (rms)}} = \frac{I_L}{\sqrt{12}} \quad (17)$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not so critical in a SEPIC application, a 10 μ F or higher value, good quality capacitor would prevent impedance interactions with the input supply.

9 SEPIC Converter Design Example $V_{in} = 8-30V$

Input voltage (V_{in}): 3.0 V-5.7 V LM3478 controller is used in this example. The schematic is shown in Figure 5.

Output voltage (V_{out}): 14.4V / 8A /

Output current (I_{out}): 2.5A /

Switching frequency f_{sw} : 330 kHz 200kHz /

LM3478 controller is used in this example. The schematic is shown in Figure 5.

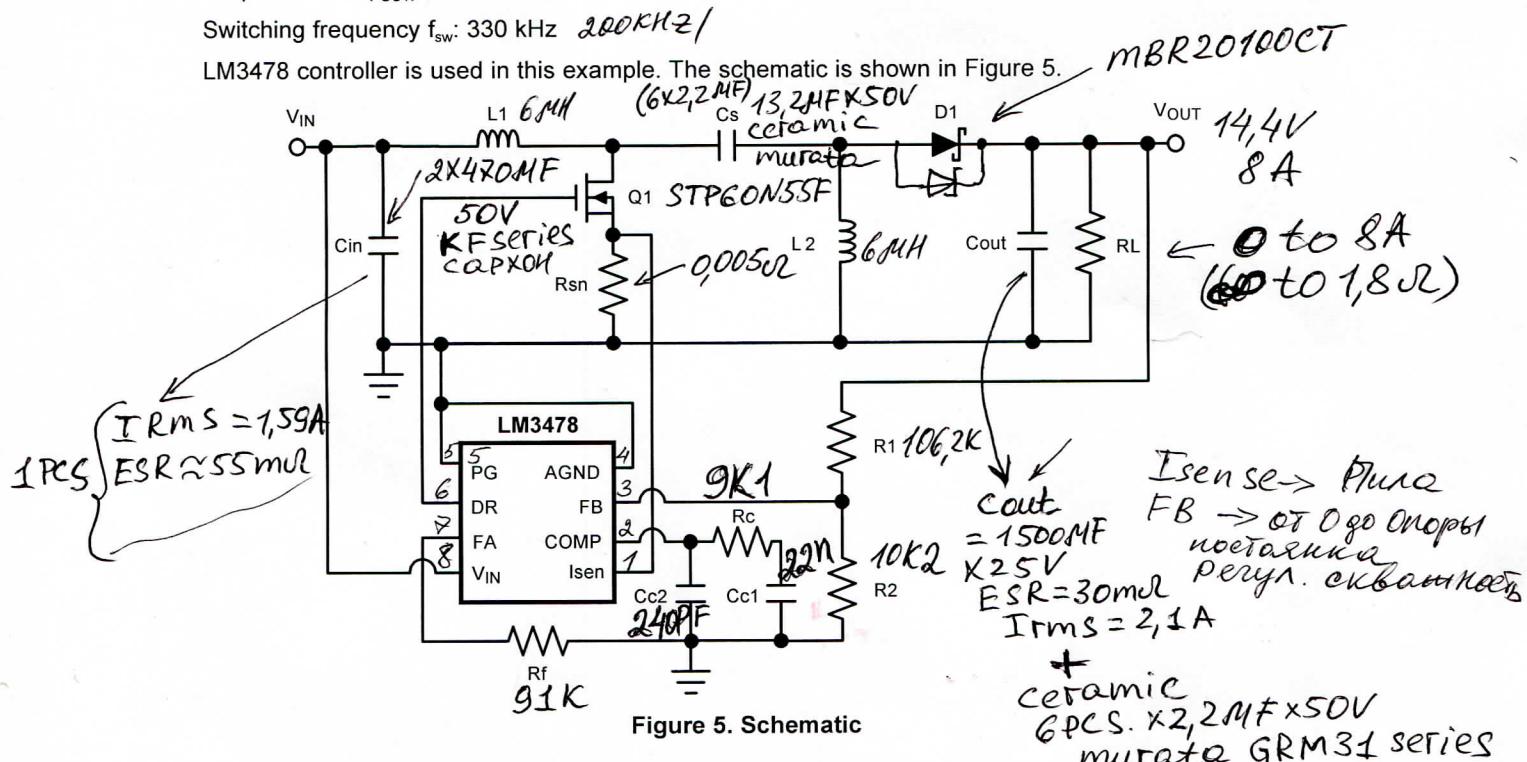


Figure 5. Schematic

Step 1: Duty cycle calculation

Assume that the V_D is 0.5 V,

$$\begin{aligned} D_{max} &= \frac{V_{out} + V_D}{V_{in\text{ (min)}} + V_{out} + V_D} = \frac{14.4 + 0.6}{8V + 14.4 + 0.6} = 0.652 \\ &= \frac{3.3 + 0.5}{3.0 + 3.3 + 0.5} = 0.56 \end{aligned} \quad (18)$$

$$D_{\min} = \frac{V_{\text{OUT}} + V_D}{V_{\text{IN}}(\text{max}) + V_{\text{OUT}} + V_D} = \frac{14,4 + 0,6}{30 + 14,4 + 0,6} = 0,333$$

$$= \frac{3,3 + 0,5}{5,7 + 3,3 + 0,5} = 0,40$$
(19)

Step 2: Inductor selection

The input inductor L1 ripple current is:

$$\Delta I_L = I_{\text{OUT}} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}(\text{min})} \times 40\% = 8A \times \frac{14,4}{8} \times 0,4 = 5,76A$$

$$= 2,5 \times \frac{3,3}{3,0} \times 0,4 = 1,1A$$
(20)

and the inductance for L1 and L2 is:

$$L_1 = L_2 = L = \frac{V_{\text{IN}}(\text{min})}{\Delta I_L \times f_{\text{sw}}} \times D_{\max} = \frac{8V}{5,76A \times 200k} \times 0,652 = 4,53 \mu H$$

$$= \frac{3,0}{1,1 \times 330k} \times 0,56 = 4,6 \mu H$$
(21)

The closest standard value of a off-the-shelf inductor is 4.7 μH . The peak input inductor current is:

$$I_{L1(\text{peak})} = I_{\text{OUT}} \times \frac{V_{\text{OUT}} + V_D}{V_{\text{IN}}(\text{min})} \times \frac{3}{2} + \frac{40\%}{2} = 8A \times \frac{14,4 + 0,6}{8V} \times 1,2 = 18A$$

$$= 2,5 \times \frac{3,3 + 0,5}{3,0} \times 1,2 = 3,8A$$
(22)

The peak current for L2 is:

$$I_{L2(\text{peak})} = I_{\text{OUT}} \times \frac{3}{2} + \frac{40\%}{2} = 2,5 \times 1,2 = 3A = 8A \times 1,2 = 9,6A$$
(23)

Step 3: Power MOSFET selection

The MOSFET peak current is:

$$I_{Q1(\text{peak})} = I_{L1(\text{peak})} + I_{L2(\text{peak})} = 18A + 9,6A = 27,6A$$

$$= 3,8 + 3 = 6,8A$$
(24)

and the RMS current is:

$$I_{Q1(\text{rms})} = I_{\text{OUT}} \sqrt{\frac{(V_{\text{OUT}} + V_{\text{IN}}(\text{min}) + V_D) \times (V_{\text{OUT}} + V_D)}{V_{\text{IN}}^2(\text{min})}} = 8A \cdot \sqrt{\frac{(14,4 + 8V + 0,6) \times (14,4 + 0,6)}{8V^2}} = 18,575A \approx 18,6A$$

$$= 2,5 \times \sqrt{\frac{(3,3 + 3,0 + 0,5) \times (3,3 + 0,5)}{3,0^2}} = 4,2A$$
(25)

The rated drain voltage for the MOSFET must be higher than $V_{\text{IN}} + V_{\text{OUT}}$. Si4442DY ($R_{\text{DS(ON)}} = 8 \text{ m}\Omega$ and $Q_{\text{GD}} = 10 \text{ nC}$) is selected in this design. The gate drive current I_G of the LM3478 is 0.3A. The estimated power loss is:

$$P_{Q1} = I_{Q1(\text{rms})}^2 \times R_{\text{DS(ON)}} \times D_{\max} + (V_{\text{IN}}(\text{min}) + V_{\text{OUT}}) \times I_{Q1(\text{peak})} \times \frac{Q_{\text{GD}} \times f_{\text{sw}}}{I_G} = 18,6A^2 \times 0,0115 \times 0,652 + (8V + 14,4V) \times 27,6A \times \frac{9,5nC \cdot 200k}{0,3A} = 6,51W$$

$$= 4,2^2 \times 8m \times 0,56 + (3 + 3,3) \times 6,8 \times \frac{10n \times 330k}{0,3} = 0,55W$$
(26)

Step 4: Output diode selection

The rated reverse voltage of the diode must be higher than $V_{\text{IN}} + V_{\text{OUT}}$ and the average diode current is equal to the output current at full load.

$$V_D > V_{\text{IN}} + V_{\text{OUT}} > 45V$$

Step 5: SEPIC coupling capacitor selection

The RMS current of the Cs is:

$$I_{Cs(\text{rms})} = I_{OUT} \times \sqrt{\frac{V_{OUT} + V_D}{V_{IN(\text{min})}}} = 8A \times \sqrt{\frac{14.4 + 0.6}{8}} = 10.955A \approx 11A$$

$$= 2.5 \times \sqrt{\frac{3.3 + 0.5}{3.0}} = 2.8A$$

chose cap murata(2,2MF x 50V x RR) x 6 PCS
C = 13.2 MF

(27)

and the ripple voltage is

$$V_{Cs} = \frac{I_{OUT} \times D_{\max}}{Cs \times f_{sw}} = \frac{2.5 \times 0.56}{10P \times 330k} = 0.42V$$

$$V_{Cs} = \frac{8A \times 0.652}{13.2MF \times 200k} = 1.976V$$
(28)

A 10 μ F ceramic cap is selected. $\rightarrow 13.2MF (2,2 \times 6 \text{ PCS})$ **Step 6: Output capacitor selection**

The RMS current of the output capacitor is:

$$I_{out(\text{rms})} = I_{Cs(\text{rms})} = 2.8A = 11A$$
(29)

Assuming the peak-to-peak ripple is 2% of the 3.3V output voltage, the ESR of the output capacitor is:

$$\text{ESR } d \frac{V_{\text{ripple}} \times 0.5}{I_{L1(\text{peak})} + I_{L2(\text{peak})}} = \frac{0.02 \times 3.3 \times 0.5}{3.8 + 3} = \frac{0.02 \times 0.5 \times 14.4V}{27.6A} \leq 5.2 \text{ m}\Omega,$$

$$= 4.8 \text{ m}\Omega$$
(30)

and the capacitance is:

$$C_{out} t \frac{I_{OUT} \times D_{\max}}{V_{\text{ripple}} \times 0.5 \times f_{sw}} = \frac{2.5 \times 0.56}{0.02 \times 3.3 \times 0.5 \times 300k} = \frac{8A \times 0.652}{902 \times 14.4 \times 0.5 \times 200k} \geq 181 \text{ MF}$$

$$= 141 \text{ PF}$$
(31)

Two pieces of 100 μ F (6m Ω ESR) ceramic caps are used. For cost-sensitive applications, an electrolytic capacitor and a ceramic capacitor can be used together. Noise sensitive applications can include a second stage filter.**Step 7: Input capacitor selection**

The RMS current of the input capacitor is:

$$I_{in(\text{rms})} = \frac{A_{IL}}{\sqrt{12}} = \frac{1.1}{\sqrt{12}} = 0.32A = \frac{5.76}{\sqrt{12}} \approx 1.67A$$
Capxon KF series Ø13X20
470MF x 50V
Irms = 1.59A; Z = 55m Ω
2x470MF
(32)

Step 8: Feedback resistors, current sensing resistor calculation and frequency set resistor

R1 is the top resistor and R2 is the bottom resistor of the voltage divider. The feedback reference voltage is 1.26V.

$$R_1 = 100k + 6.2k \text{ series}$$

If R1 = 20 k Ω , then:

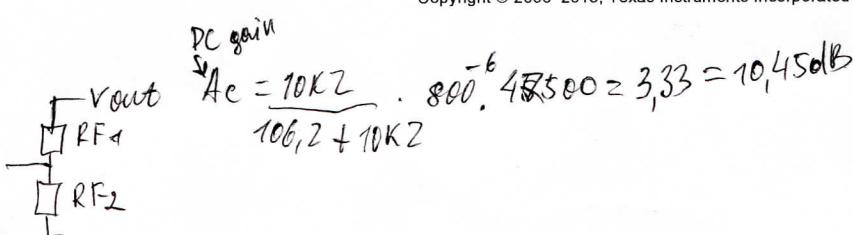
$$R_2 = \frac{V_{REF}}{V_{OUT} - V_{REF}} \times R_1 = \frac{1.26}{3.3 - 1.26} \times 20k = \frac{1.26}{14.4 - 1.26} \times 106.2k = 10.18k \approx 10.2k$$

$$5k1 + 5k1 \text{ series}$$

$$= 12.4 k$$
(33)

For the LM3478, the threshold voltage to trigger the current protection varies with duty cycle. The threshold is a ramp which is defined by Vsense at 0% duty cycle and Vsense - Vsl at 100% duty cycle. The values for Vsense and Vsl can be taken from the *Electrical Characteristics* section of the *LM3478, LM3478-Q1 High-Efficiency Low-Side N-Channel Controller for Switching Regulator Data Sheet (SNVS085)*. There is also a plot in the data sheet showing the typical current sense voltage vs duty cycle. In our example the duty cycle was calculated to be about 50% and so we use the current limit threshold of 130mV for the following calculation to keep things simple. Thus the sensing resistor value is:

$$R_{sn} = \frac{130 \text{ mV}}{I_{Q1(\text{peak})}} = \frac{130 \text{ m}}{6.8} = 19 \text{ m} \Omega = \frac{110 \text{ mV}}{27.6A} = 4 \text{ m}\Omega \approx 5 \text{ m}\Omega$$
(34)



R_{f1} is approximately 50 kΩ for 330 kHz operation. 91k for 200kHz operation

Step 9: Compensation Design

In the control to output transfer function of a peak current mode controlled SEPIC converter, the load pole can be estimated as $1/(2\pi RL \cdot C_{out})$; The ESR zero of the output capacitor is $1/(2\pi ESR \cdot C_{out})$, where RL is the load resistor, Cout is the output capacitor and ESR is the Equivalent Series Resistance of the output capacitor. There is also a right-half-plane zero (f_{RHPZ}), given by:

$$f_{RHPZ} = \frac{(1 - D_{max})^2 \times V_{OUT}}{2\pi \times D_{max} \times L_2 \times 0.5 \times I_{OUT}} = \frac{(1 - 0.652)^2 \times 14.4}{2\pi \times 0.652 \times 6.8 \text{mH} \times 0.5 \times 8A} = 12737 \text{Hz}$$

$$= \frac{(1 - 0.56)^2 \times 3.3}{2\pi \times 0.56 \times 4.7 \text{P} \times 0.5 \times 2.5} = 31 \text{kHz}$$
(35)

We can also see a "glitch" in the magnitude plot at the resonant frequency of the network formed by the SEPIC capacitor Cs and the inductor L2:

$$f_R = \frac{1}{2\pi \sqrt{L_2 \cdot C_s}} = \frac{1}{2\pi \sqrt{4.7 \text{PH} \times 10 \text{PF}}} = 12883 \text{Hz}$$

$$= 23 \text{kHz}$$
(36)

The crossover frequency is set at one sixth of the f_{RHPZ} or f_R , whichever is lower:

$$f_c = \frac{f_R}{6} = \frac{23 \text{kHz}}{6} = 3.8 \text{kHz} = \frac{17.9}{6} \approx 3 \text{kHz}$$
(37)

Parts Cc1, Cc2 and Rc form a compensation network, which has one zero at $1/(2\pi R_c \cdot C_{c1})$, one pole at the origin, and another pole at $1/(2\pi R_c \cdot C_{c2})$.

Where, V_{REF} is the reference voltage of 1.26 V, V_{OUT} is the output voltage, G_{cs} is the current sense gain (roughly $1/R_{sn}$) 100A/V, and G_{ma} is the error amplifier transconductance (800 μmho).

$$\frac{V_{out}}{V_{in}} = \frac{D}{(1-D)}$$

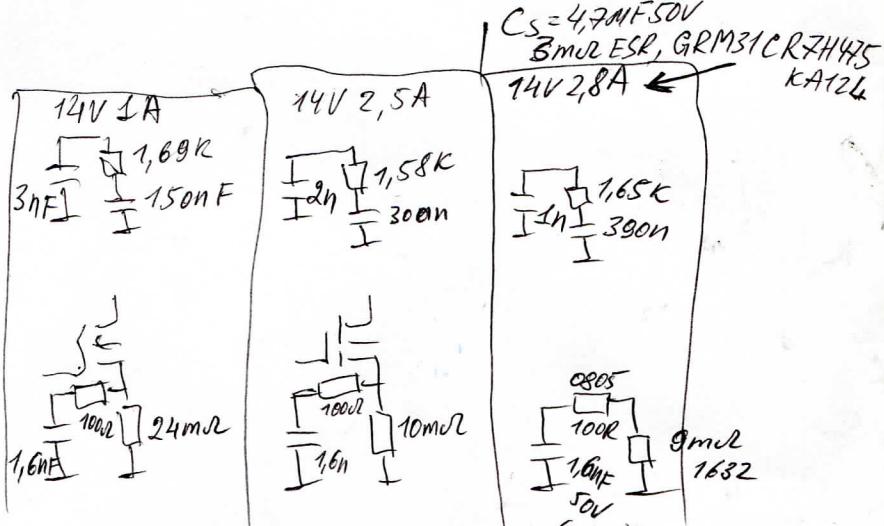
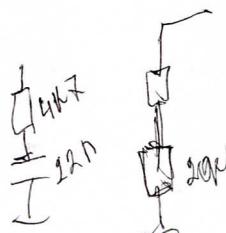
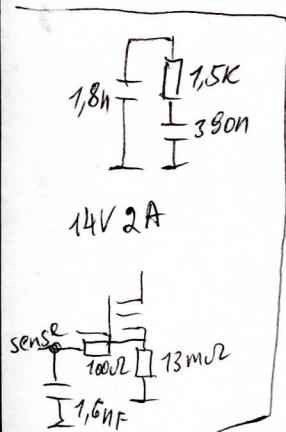
$$D = \frac{V_{out}}{V_{in} + V_{out}}$$

$$R_c = \frac{\frac{2\pi \times f_c \times C_{out} \times V_{out}^2 \times (1 + D_{max})}{G_{cs} \times G_{ma} \times V_{REF} \times V_{in} (\min) \times D_{max}}}{\frac{1}{0.005} \times 800 \mu\text{mho} \times 1.26 \times 8 \times 0.652} = \frac{2\pi \times 3 \text{kHz} \times 1500 \text{nF} \times 14.4 \times (1+0.652)}{1.26 \times 800 \mu\text{mho} \times 1.26 \times 8 \times 0.652} \approx 9.21 \text{m}\Omega$$

$$= \frac{2\pi \times 3.8 \text{k} \times 200 \text{P} \times 3.3^2 \times (1 + 0.56)}{91 \times 800 \text{P} \times 1.26 \times 3.0 \times 0.56} = 523: \quad \downarrow -6$$

*NC V898031 - SEPIC/B008T
NCV8871 106spu Dmax = 88%*

(38)



Cc1 is chosen to set the compensator zero to 1/4 off the crossover frequency:

$$Cc1 = \frac{4}{2\pi f_c R_c} = \frac{4}{2\pi \times 3.8k \times 523} = 330 \text{ nF} = \frac{4}{2\pi \times 3k \times 9.8k} = 23 \text{ nF} \quad (39)$$

The pole at $1/(2\pi R_c C_c 2)$ is to cancel the ESR zero $1/(2\pi ESR C_{out})$,

$$Cc2 = \frac{C_{out} \times ESR}{R_c} = \frac{200 \mu F \times 3m}{523} = 1.2 \text{ nF} = \frac{1500 \mu F \times 1.5 \mu R}{9k1} = 247 \mu F$$

10 References

LM3478, LM3478-Q1 High-Efficiency Low-Side N-Channel Controller for Switching Regulator Data Sheet (SNVS085)

2,2MFx50V XFR murata (GRM31)

$$\tan \delta = 0,025 \text{ max}$$

$$ESR = \frac{\tan \delta}{2\pi f_c} = \frac{0,025}{2\pi \cdot 200k \cdot 2,2MF} = 9 \mu R$$

$$6 \times 2,2MF \text{ Parallel} = 9/6 = 1,5 \mu R$$

1500MF x 25V Samwha WL series

$$ESR \approx 30 \mu R \quad I_{rms} = 2,1A$$

$$1,5 \mu R // 30 \mu R \approx 1,43 \mu R \Rightarrow 1,5 \mu R$$

$\Delta t = 10\%$	$I = \sqrt{P/R}$	$I_{max} = 1PCS$
$\Delta t = 20\%$	$= 130 \text{ mW}$	$2,7A$
$\Delta t = 30\%$	$= 196 \text{ mW}$	$3,8A$
$\Delta t = 40\%$	$= 261 \text{ mW}$	$4,6A$
$\Delta t = 50\%$	$= 326 \text{ mW}$	$5,3A$

$$\Delta t =$$

20 - 150V SEPIC

$$D_{max} = \frac{13,8 + 0,6}{20 + 13,8 + 0,6} = 0,419$$

$$D_{min} = \frac{13,8 + 0,6}{150 + 13,8 + 0,6} = 0,086$$

20 - 150V BUCK

$$D_{max} = \frac{13,8 + 0,6}{20} = 0,72$$

$$D_{min} = \frac{13,8 + 0,6}{150} = 0,096$$