Schematic Review Form

HD3SS3220 review

Pin #	Name	Info	Violations	*Description*
1	CC2	Connected to CC2		Type-C Configuration channel signal 2
2	CC1	Connected to CC1		Type-C Configuration channel signal 1
3	CURRENT_MODE	No connection, Low (900mA)		Tri-level input pin to indicate current advertisement in DFP (or DFP in DRP) mode while in GPIO mode. Don’t care in UFP mode. Provides the flexibility to advertise higher current without I2C. The pin has 250 K internal pull-down. L – Low - Default – 900 mA M - Medium (Install 500 K to VDD5 on the PCB) – 1.5 A H - High (Install 10 K to VDD5 on the PCB) – 3 A
4	PORT	4.7K pullup to upstream VBUS		Tri-level input pin to indicate port mode. The state of this pin is sampled when HD3SS3220’s ENn_CC is asserted low, and VDD5 is active. This pin is also sampled following a I2C_SOFT_RESET. H - DFP (Pull-up to VDD5 if DFP mode is desired) NC - DRP (Leave unconnected if DRP mode is desired) L - UFP (Pull-down or tie to GND if UFP mode is desired)

5	VBUS_DET	909K pullup to downstream VBUS		5-28V VBUS input voltage. VBUS detection determines UFP attachment. One 900K external resistor required between system VBUS and VBUS_DET pin.
6	TXp	Connected to upstream SSRX through 470nF capacitor		Host/Device USB SuperSpeed differential Signal TX positive
7	TXn	Connected to upstream SSRX through 470nF capacitor		Host/Device USB SuperSpeed differential Signal TX negative
8	VCC33	Connected to 3.3V voltage regulator		3.3-V Power supply
9	RXp	Connected to upstream SSTX		Host/Device USB SuperSpeed differential Signal RX positive
10	RXn	Connected to upstream SSTX		Host/Device USB SuperSpeed differential Signal RX negative
11	DIR	200K pullup to 3.3V		Type-C plug orientation. Open drain output. A pull-up resistor (that is, 200 K) must be installed for proper operation of the device.
12	ENn_MUX	Connected to ID pin		Active Low MUX Enable: L - Normal operation, and H - Shutdown.
13, 28	GND	Ground		Ground

14	RX1n	Routed to SSTX1 on USB-C connector through 470nF capacitor		Type-C Port - USB SuperSpeed differential Signal RX1 negative
15	RX1p	Routed to SSTX1 on USB-C connector through 470nF capacitor		Type-C Port - USB SuperSpeed differential Signal RX1 positive
16	TX1n	Routed to SSRX1 on USB-C connector		Type-C Port - USB SuperSpeed differential Signal TX1 negative
17	TX1p	Routed to SSRX1 on USB-C connector		Type-C Port - USB SuperSpeed differential Signal TX1 positive
18	RX2n	Routed to SSTX2 on USB-C connector through 470nF capacitor		Type-C Port - USB SuperSpeed differential Signal RX2 negative
19	RX2p	Routed to SSTX2 on USB-C connector through 470nF capacitor		Type-C Port - USB SuperSpeed differential Signal RX2 positive
20	TX2n	Routed to SSRX2 on USB-C connector		Type-C Port - USB SuperSpeed differential Signal TX2 negative
21	TX2p	Routed to SSRX2 on USB-C connector		Type-C Port - USB SuperSpeed differential Signal TX2 positive
22	ADDR	NC, GPIO mode		Tri-level input pin to indicate I2C address or GPIO mode: H (connect to VDD5) - I2C is enabled and I2C 7-bit address is 0x67. NC - GPIO mode (I2C is disabled) L (connect to GND) - I2C is enabled and I2C 7-bit address is 0x47.

				ADDR pin should be pulled up to VDD5 if high configuration is desired
23	INT_N/OUT3	200K pullup to upstream VBUS		When used as the INT_N, the pin is an open drain output in I2C control mode and is an active low interrupt signal for indicating changes in I2C registers. When used as OUT3, the pin is in audio accessory detect in GPIO mode: H - no detection, and L - audio accessory connection detected.
24	VCONN_FAULT_N	No connection		Open drain output. Asserted low when VCONN overcurrent detected.
25	SDA/OUT1	No connection		When I2C is enabled (ADDR pin is high or low), this pin is the I2C communication data signal. When in GPIO mode (ADDR pin is NC), this pin is an open drain output for communicating Type-C current mode detect when the device is in UFP mode: H – Default (900 mA) current mode detected, and L – Medium (1.5 A) or High (3 A) Current Mode detected.
26	SCL/OUT2	No connection		When I2C is enabled (ADDR pin is high or low), this pin is the I2C communication clock signal. When in GPIO mode (ADDR pin is NC), this pin is an open drain output for communicating Type-C current mode detect when the device is in UFP mode: H – Default or Medium current mode detected, and L – High current mode detected.
27	ID	200K pullup to upstream VBUS. Routed to EN pin on vbus switch and to FNn MUX		Open drain output. Asserted low when CC pin detected device attachment when port is a source (DFP), or dual-role (DRP) acting as source (DFP).

29	ENn_CC	Tied to ground		Enable signal for CC controller. Enable is active low.
30	VDD5	Connected to upstream VBUS		5-V Power supply

Comments