Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.40mil	3.5	
3	Top Layer	Copper	1.40mil		
4	Dielectric1	FR-4	5.00mil	4.2	
5	Signal Layer 1	Copper	1.40mil		
6	Dielectric 3		45.60mil	4.2	
7	Signal Layer 2	Copper	1.40mil		
8	Dielectric 2		5.00mil	4.2	
9	Bottom Layer	Copper	1.40mil		
10	Bottom Solder	Solder Resist	0.40mil	3.5	
11	Bottom Overlay				

DESIGN INFORMATION

MIN. TRACK WIDTH: 5 MIL
MIN. CLEARANCE: 0.2 mm
MIN. VIA PAD SIZE: 10 MIL
MINIMUM ANNULAR RING 0.05mm (2MIL) EXTERNAL
PER IPC-D-275 CLASS 2 LEVEL C
REGISTRATION TOLERANCES: METAL +/- 5 MIL, HOLES +/- 3 MIL
HOLE SIZE TOLERANCE (UNLESS OTHERWISE SPECIFIED): +/- 3 MIL
NOTE: Fill all 6 mil vias and plate shut then polish flat.

MATERIAL:
[ ] FR-408 [X] FR-4 High Tg [ ] OTHER
THICKNESS: [X] 62 MIL (1.6mm) +/-10% [ ] OTHER
TOLERANCE: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-
BOW & TWIST: [X] ANSI IPC-6012 TYPE 3 CLASS 2
[ ] OTHER +/-

DRILLING:
REFERENCE: [X] AS SHOWN [X] NC_DRILL FILES
PTH COPPER THICKNESS: [X] 20-30 um [ ] OTHER

BOARD FINISH:
SILKSCREEN: [X] TOP [X] BOTTOM
SILKSCREEN COLOR: [X] WHITE [ ] OTHER
SOLDER RESIST COLOR: [X] GREEN [ ] OTHER
[X] MATTE [ ] SEMI-GLOSS

SURFACE FINISH: [X] IMMERSION GOLD (ENIG) [ ] ENEPIG
[ ] IMM. TIN/SILVER OR EQUIV [ ] OTHER

ARRAY/PANEL: [ ] CUT AND TRIM PER M1 BOARD OUTLINE
[ ] N.C. ROUTE [X] V. SCORE

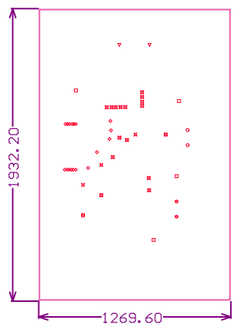
CERTIFICATION: MATERIALS AND WORKMANSHIP FOR ALL PCBS TO MEET OR EXCEED THE REQUIREMENTS OF:
[X] ANSI IPC-A-600F CLASS -> [ ] 1 [X] 2 [ ] 3
[X] RoHS [ ] OTHER PER ORDER

ALL BOARDS MUST MEET OR EXCEED UL94-V0 REQUIREMENTS.
PCB MUST BEAR THE UL94V-0 UL REGISTERED MATERIAL ID NUMBER

ADDITIONAL REQUIREMENTS:
MICROSECTION: [ ] YES
BARE BOARD ELEC. TEST: [ ] NONE [X] REQUIRED [ ] PER ORDER

Symbol	Quantity	Finished Hole Size	Plated	Hole Type	Drill Layer Pair	Tolerance
◇	17	6.00mil (0.152mm)	PTH	Round	Top Layer - Bottom Layer	
⊠	14	7.87mil (0.200mm)	PTH	Round	Top Layer - Bottom Layer	
■	3	32.00mil (0.813mm)	PTH	Round	Top Layer - Bottom Layer	
○	2	40.00mil (1.016mm)	PTH	Round	Top Layer - Bottom Layer	
⊠	3	42.00mil (1.067mm)	PTH	Round	Top Layer - Bottom Layer	
✡	2	51.18mil (1.300mm)	PTH	Round	Top Layer - Bottom Layer	
▽	2	55.12mil (1.400mm)	PTH	Round	Top Layer - Bottom Layer	
□	4	63.00mil (1.600mm)	PTH	Round	Top Layer - Bottom Layer	
	47 Total					

FAB NOTE: Fill all 6 mil vias and plate shut then polish flat.



TEXAS INSTRUMENTS

PROJECT TITLE: LMG1020EVM
DESIGNED FOR: Public Release
FILE NAME: HVP006A.PcbDoc

ALL ARTWORK VIEWED FROM TOP SIDE	BOARD #: HPV006	REV: A	SVN REV: Not In VersionControl
LAYER NAME = Dimensions	TID #: N/A		
PLOT NAME = Fabrication Drawing	GENERATED : 5/3/2018 8:21:26 AM	TEXAS INSTRUMENTS	

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ENGINEER:	LAYOUT BY:
Alberto Doronzo	Alberto Doronzo
SCALE: 1.00	ALTIUM DESIGNER VERSION: 17.1.5.472