

As current is drawn out of the FB pin the oscillator frequency will decrease based on how much FB current is drawn out of the pin. There is no information in the data sheet in regards to what exact ratio

of oscillator frequency is vs IFB current is. However, I will make an estimate/guesstimate based on slope the change of FB current (dIFB) vs estimated change in switching frequency (dfsw).

$$dfsw/IFB \approx 1\text{MHz}-35\text{kHz}/85.1\mu\text{A} \approx 11.3\text{kHz}/\mu\text{A}.$$

Based on the slope equation above we can estimate the desired current to pull out of the FB pin to get the designer minimum switching frequency (fmind).

$$IFB@fmin = fmind * (\mu\text{A}/11.3 \text{ kHz})$$

If we wanted a minimum switching frequency of 50 KHz would require a IFB@fmin of 4.42uA. Please see the calculation below.

$$IFB@fmin \approx 50 \text{ kHz} * (\mu\text{A}/11.3\text{kHz}) = 4.42 \mu\text{A}.$$

I will make an estimate on the FB pin voltage when the FB pin is open with an estimate of a Vds voltage of the internal FET being 0.25V. I estimate the FB voltage would be roughly 9V.

$$V_{FB} \approx I_{FB} * R_{FB\text{internal}} + V_{ds} \approx 85.1 \mu\text{A} * 101.5\text{K} + 0.35\text{V} = 9\text{V}$$

Based on this estimate the resistor from the FB pin to ground would be 2.03M ohm.

$$R1 = V_{FB}/I_{FB@fmin} = 9\text{V}/4.42\mu\text{A} \approx 2.03 \text{ M ohm}$$

I would suggest using a potentiometer of 5 M ohm and dialing down slowly to the exact value. You need 100 turns or more to limit the maximum frequency.

I have not tried this but it should work.

Good luck on your design.

Regards,

Mike