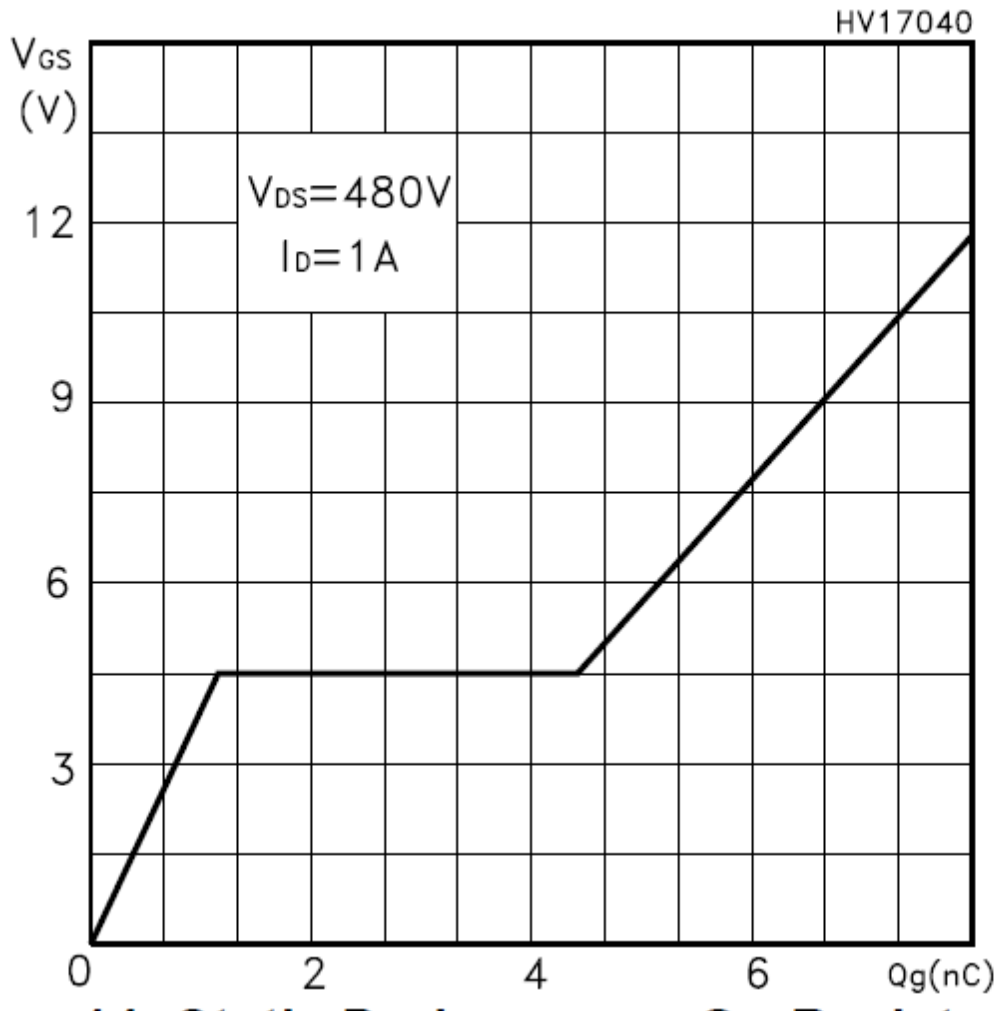


Hello Jean

1. The power dissipation of the IC will change based on the FETs gate charge and switching frequency that is used. The following V_{GS} curve vs Q_g is from the STN2HN2HNK60 data sheet.
 - a. This curve is required to calcite the IC power dissipation.



The UCC28710's gate DRV is limited to 16V, $V_{GS(max)} = 16 V$.

DRIVERS					
I_{DRS}	DRV source current	$V_{DRV} = 8 V, V_{VDD} = 9 V$	20	25	mA
R_{DRVLS}	DRV low-side drive resistance	$I_{DRV} = 10 mA$	6	12	Ω
V_{DRCL}	DRV clamp voltage	$V_{VDD} = 35 V$	14	16	V
R_{DRVSS}	DRV pull-down in start state		150	190	230 k Ω

$$P_{gate} = 2 * Q_g * f_{swmax} = 2 * 10nC * 100kHz = 3.2mW.$$

$$P_{IC} = P_{gate} + V_{DD} * I_{run} = 3.2 mW + 20V * 2.65mA = 55mW$$

BIAS SUPPLY INPUT					
I_{RUN}	Supply current, run	$I_{DRV} = 0$, run state	2.00	2.65	mA

- 2 You are correct $D_{mag} = 1 - D_{max} - F_{max} * T_r / 2$
 - a. The app note did not make the correction for T_r
- 3 The turns ratio of the aux winding to secondary winding should be $N_p / N_a \approx (V_{dd(off)} + V_d) / (V_{out_min} + V_d)$, V_d is a diode drop.
- 4 To calculate the peak aux current use the following formula.
 - a. $I_{Aux Peak} = I_{Primary Peak} * N_p / N_a$
 - b. $V_{in} / V_{out} = N_p / N_s = I_{out} / I_{in}$