Hello Zac,

I am curious if the change of the bulk capacitor (C16) ESR is changing at cold triggering an input under voltage condition fault. This is where switching stops and VDD capacitor is discharged to UVLO and then the VDD capacitor is charged back up to UVLO turn on. The thresholds are listed below.

UNDER-VOLTAGE LOCKOUT						
$V_{VDD(on)}$	VDD turn-on threshold	V_{VDD} low to high	19	21	23	V
$V_{VDD(off)}$	VDD turn-off threshold	V_{VDD} high to low	7.7	8.1	8.45	

Please note if the fault is triggered the VDD capacitor will be discharged with IFAULT of 2.1 to 2.8 mA.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNITS
BIAS SUPPLY INPUT						
I_{RUN}	Supply current, run	I_{DRV} = 0, run state		2.1	2.65	mA
I_{WAIT}	Supply current, wait	I_{DRV} = 0, wait state		85	110	µA
I_{START}	Supply current, start	I_{DRV} = 0, V_{VDD} = 18 V, start state		1	1.5	
I_{FAULT}	Supply current, fault	I_{DRV} = 0, fault state		2.1	2.8	mA

If this is the case you will observe that VDD will cycle between UVLO turn on and turn off. You can then verify this by studying the input bulk capacitor voltage, VDD and the gate drive with reference to the UCC28700 device ground.

During startup the device will give three gate drive sample pulses looking for faults. If the device senses and input under voltage the VDD capacitor will be discharge based on a fault.

When the gate driver is on the aux signal is pulled below ground. The input is sensed through the Np/Na turns ratio. If the VS pin sees greater than IVSL(RUN) current (220uA) coming out of this pin the device knows that the input voltage is high enough to run and will let switching continue. If not the device will stop switching and initiate a UVLO cycle for restart.

Vin > (Np/Na)*IVSL(Run)*R49 = (Np/Na)*220uA*115k

$I_{VSL(run)}$	VS line-sense run current	Current out of VS pin – increasing	190	220	260	µA
$I_{VSL(stop)}$	VS line-sense stop current	Current out of VS pin – decreasing	70	80	95	

Please note that if this is the case you will need to find an input bulk capacitor that is rated for the cold temperatures that you are using. You will need to verify the ESR in the capacitor is small enough not to trigger a UVLO.

Please note the high frequency current when the switch turns on will slightly drop the bulk voltage.

Ipeak = Vcs(max)/R54

The voltage drop of on the bulk capacitor

Vdrop = VC16 – Ipeak*ESR

Regards,

Mike