How to Design With TPS65560/TPS65561 Photo Flash Charger and IGBT Driver

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ABSTRACT

The Texas Instruments TPS65560/TPS65561 photo flash chargers offer a complete solution for charging a photo flash capacitor from a battery input, and subsequently discharging the capacitor to a xenon flash tube. These devices have an integrated voltage reference, power switch, IGBT driver, and control logic blocks for capacitor charging and driving IGBT applications. Compared with discrete solutions, these devices reduce the component count, shrink the solution size, and ease designs for xenon tube applications. Additional advantages are fast charging times and high efficiency from an optimized PWM control algorithm.

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1 Introduction

The TPS65560/TPS65561 photo flash chargers offer a complete solution for charging a photo flash capacitor from a battery input, and subsequently discharging the capacitor to a xenon flash tube. These devices have an integrated voltage reference, power switch, insulated gate bipolar transistor (IGBT) driver, and control logic blocks for capacitor charging and driving IGBT applications. Compared with discrete solutions, these devices reduce the component count, shrink the solution size, and ease designs for xenon tube applications. Additional advantages are fast charging times and high efficiency from an optimized PWM control algorithm. The typical application circuit is shown in Figure 1.

Among the salient features of the TPS65560/TPS65561 are programmable peak current at primary side, detecting STOP charging at primary side, and four kinds of protections.

- It is easy to program the peak current at the primary side. The peak current can be set from I(PEAK1) to I(PEAK2) by using the I_PEAK pin of the TPS65560/TPS65561 (see Figure 9). These values ($I_{(PEAK1)}$ and $I_{(PEAK2)}$) are specified in each product data sheet. Section 2.1.3 discusses this in detail.
- The target output voltage is set by the turn ratio of the transformer. The TPS65560/TPS65561 stop charging when they detect the target voltage from the primary side via the transformer. VFULL, which is the target voltage on the primary side, is specified in each product data sheet. Section 2.1.2 discusses this in detail.
- The devices have four kinds of protections: MAX ON TIME, MAX OFF TIME, OVER VDS, and THERMAL disable. Section 2.1.8 discusses these in detail.

The TPS65560/TPS65561 are particularly well suited for portable device applications, such as digital still cameras (DSCs), digital video cameras (DVCs), optical film cameras, mobile camera phones, and PDAs with cameras.

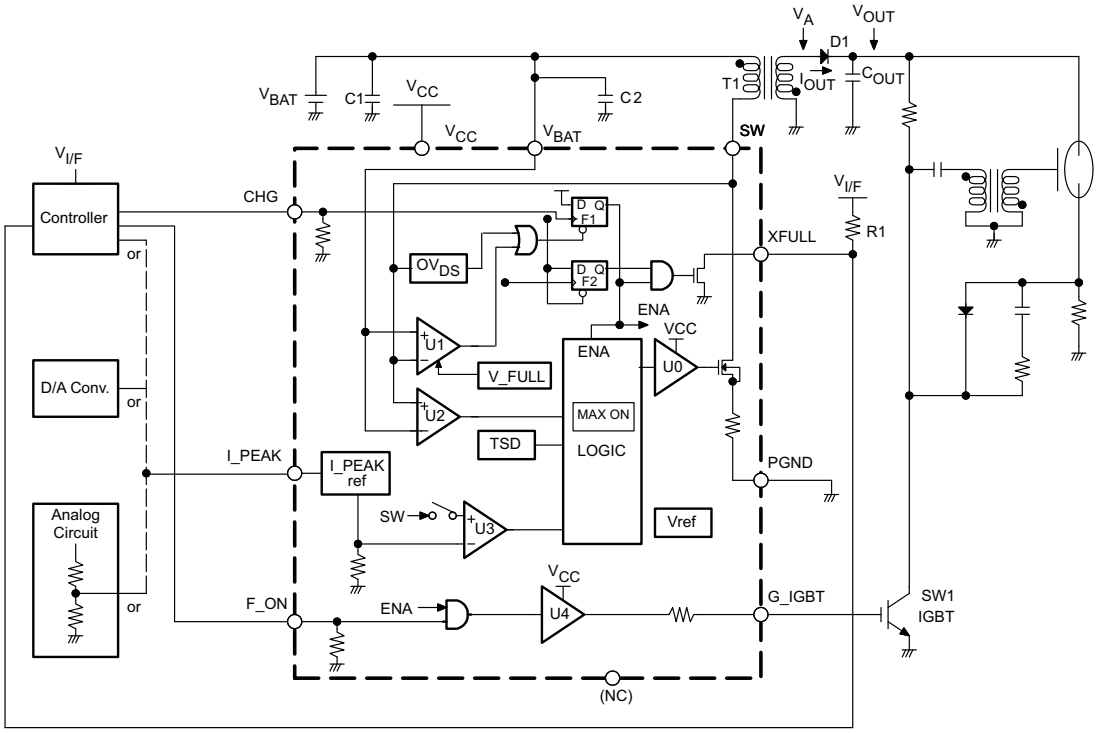


Figure 1. Typical Application Circuit

2 Operation

2.1 Basic Function

2.1.1 How to Start and Stop Charging

The TPS65560/TPS65561 have one internal enable latch, F1, that holds the state (ON/OFF status) of the device (see Figure 2). The only way to start charging is to input the rising edge into the CHG pin (see time A/C/H in Figure 4). Each time the rising edge is applied, the TPS65560/TPS65561 start charging.

The following items describe how to stop charging:

1. Forcing a STOP by setting the CHG pin to a logic low (see time B in Figure 4).
   - This manually stops the charging. Setting the CHG pin to low forces the internal enable signal (ENA) (see Figure 2) low and the internal FET switch turns off.
2. Automatic STOP by detecting the output voltage when V_{OUT} reaches the target value (see time D in Figure 4).
   - This is the standard stop function. U1 (see Figure 2) compares (V_{SW} – V_{BAT}) to VFULL, which is the target voltage on the primary side. (V_{SW} is the voltage at the SW pin and V_{BAT} is the battery voltage.) The TPS65560/TPS65561 automatically stop charging when (V_{SW} – V_{BAT}) exceeds VFULL.
3. Protected stop by detecting an overvoltage (OVDS) on the SW pin (see time I in Figure 4).
   - This function protects the TPS65560/TPS65561 from stress due to overcurrent at the SW pin when the internal FET switch is ON. The internal FET is turned off if the voltage between the drain and the source of the FET exceeds the specified OV_{DS} voltage. The value (overcurrent detection at V_{SW}) is specified in each product data sheet. Internally, exceeding OVDS makes F1 reset, forcing ENA to low and switching the internal FET off.

To prevent false operation due to noise on the CHG pin, the TPS65560/TPS65561 have a logic mask between CHG input signal and internal enable signal (ENA) (see Figure 3). The mask is valid up to the rising edge of th ENA signal. The typical mask time is approximately 12 µs.

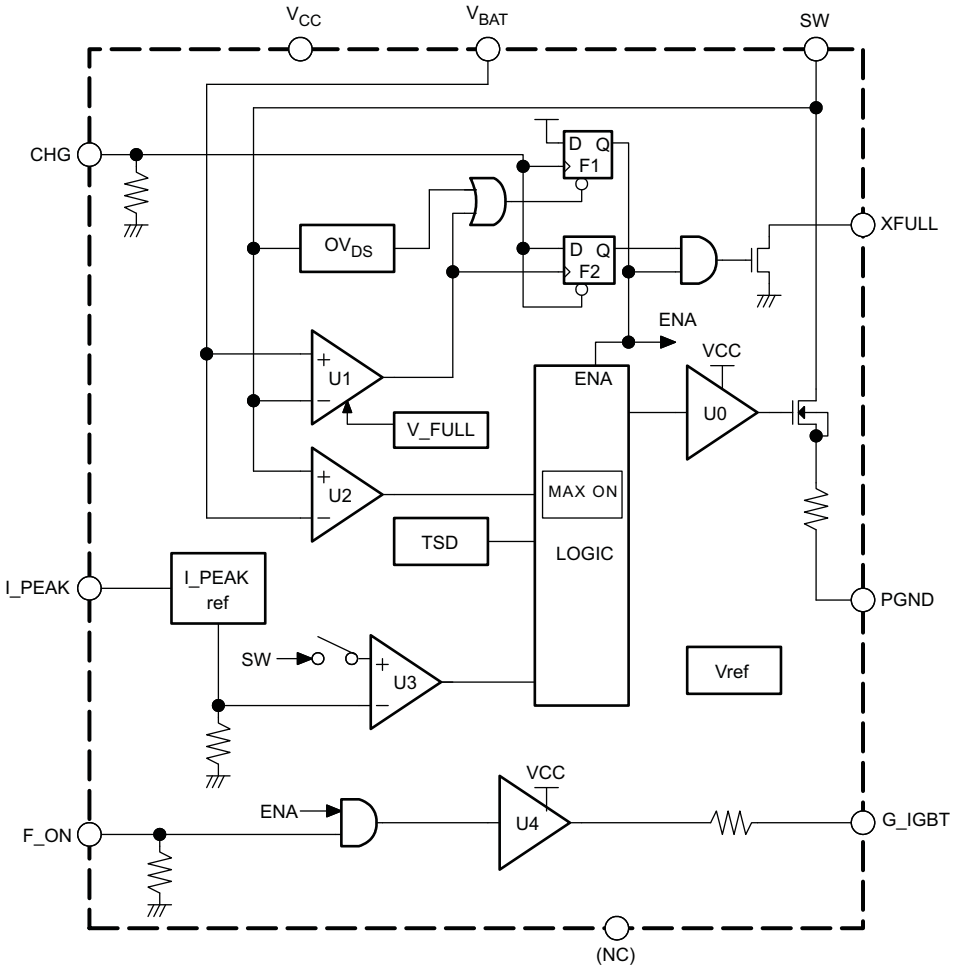


Figure 2. Block Diagram

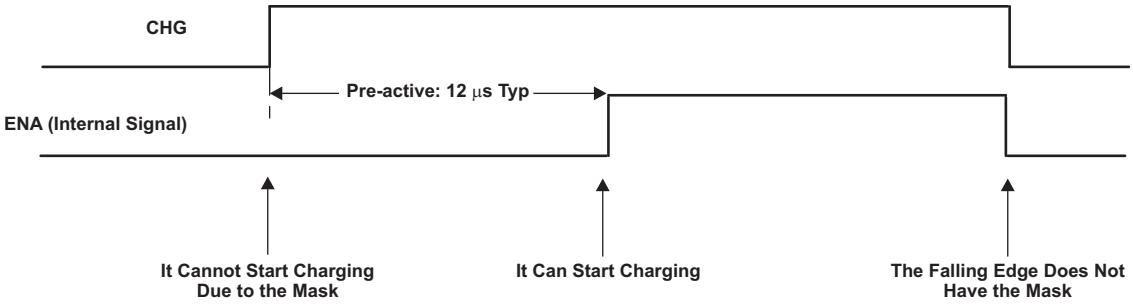


Figure 3. CHG Mask Time

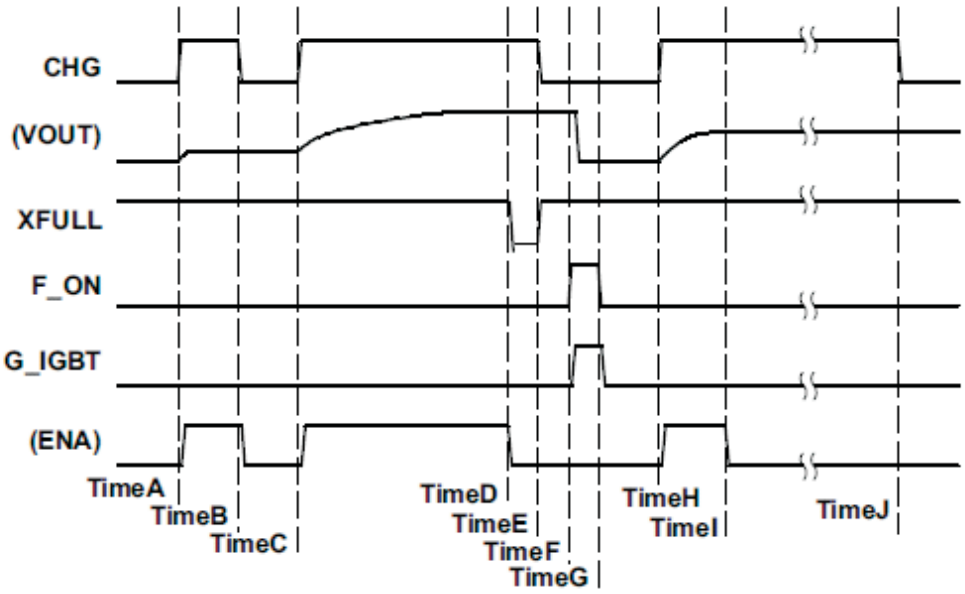


Figure 4. Whole Operation Sequence Diagram

2.1.2 Control Charging

The TPS65560/TPS65561 application circuit is based on a flyback power-supply topology. When the internal FET switch turns on, current, which is programmable by the I_PEAK pin voltage, flows into the primary side of the transformer and, thus, stores energy in the primary winding. When the internal FET switch turns off, the stored energy is transferred to the secondary side of the transformer. At that moment, the current flows in the secondary side to the photo flash capacitor (C_{OUT} in Figure 1) via the diode, D1.

The TPS65560/TPS65561 use three comparators (U1, U2, and U3) (see Figure 1 and Figure 2) to determine the state of the internal FET switch. The descriptions for these comparators follow.

- U1 (VFULL comparator): Detects charge completion
- U2 (VZERO comparator): Detects the turning ON timing
- U3 (I_PEAK comparator): Detects the turning OFF timing

While internal FET switch is ON (time1 to time2 in Figure 5), U3 monitors I_{SW}, which is the current flowing through the SW pin to PGND. When ISW exceeds the target peak current defined by the I_PEAK pin voltage, SW turns OFF (time2 in Figure 5).

When the internal FET switch turns OFF (time2 in Figure 5), the magnetic energy in the primary of the transformer is transferred to the secondary side. Meanwhile, U2 monitors the kickback voltage at the SW terminal. As the energy is discharging, the kickback voltage is increasing according to the increase of V_{OUT} (time2 to time3 in Figure 5). When most all of the energy is discharged, the system cannot continue rectification via the diode, and the charging current of I_{OUT} goes to zero (time3 in Figure 5). After rectification stops, the small amount of energy left in the transformer is released via parasitic paths, and the kickback voltage reaches zero (time3 to time4 in Figure 5). During this period, U2 makes the internal FET switch turn ON when (V(SW) – VBAT) dips from V(ZERO) (time5 in Figure 5). In the actual circuit, the period between time4 and time5 in Figure 5 is small, or does not appear dependent on the delay time from the U2 detection to the internal FET switch ON.

The ON time of internal FET switch depends on the target peak current defined by the I_PEAK pin voltage. The ON time is calculated by Equation 1. The reverse recovery time (Trr) of the diode, which is put on the secondary side, is not a constant value because it varies by temperature, forward current, and the variable current at turn OFF. Section 3.2.1 discusses this influence in detail.

$$T_{ON(n)} = L_P \frac{I\_PEAK}{V_{BAT}} + Trr(n) \quad (1)$$

Where:

$T_{ON(n)}$ = ON time at n cycle switching
L_P = Primary inductance
I_PEAK = Peak current at primary side
V_{BAT} = Battery voltage
Trr(n) = Reverse recovery time at n cycle switching

On the other hand, the OFF time depends on output voltage for each cycle. This is because the current that flows on the secondary side depends on output voltage for each cycle. The OFF time at each cycle is calculated by Equation 2.

$$T_{OFF(n)} = N \times L_P \frac{I\_PEAK}{V_{OUT(n)}} \quad (2)$$

Where:

$T_{OFF(n)}$ = OFF time at n cycle switching
N = Turn ratio of transformer
$V_{OUT(n)}$ = Output voltage at n cycle switching

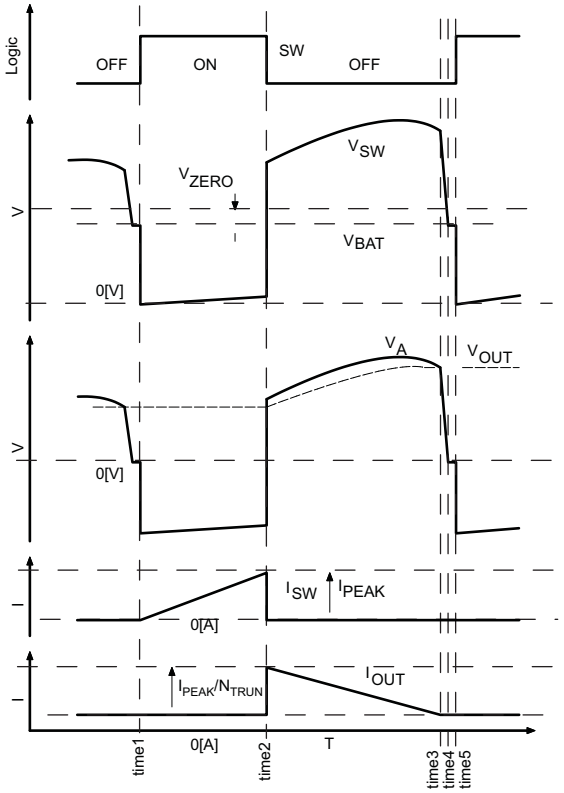


Figure 5. Timing Diagram for One Switch Cycle

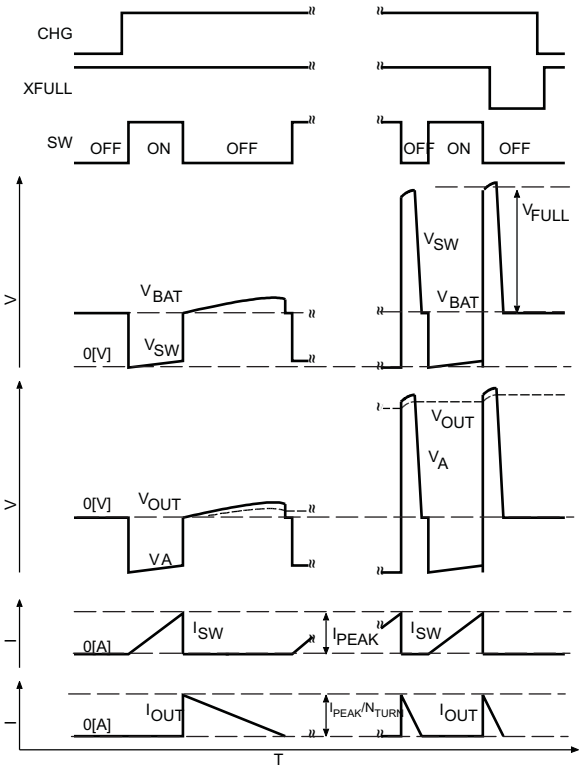


Figure 6. Timing Diagram for Beginning/Ending Cycles

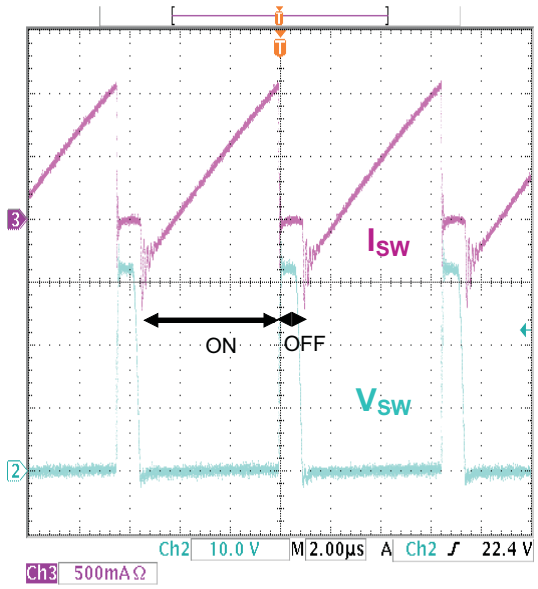


Figure 7. Waveform (Primary Side)

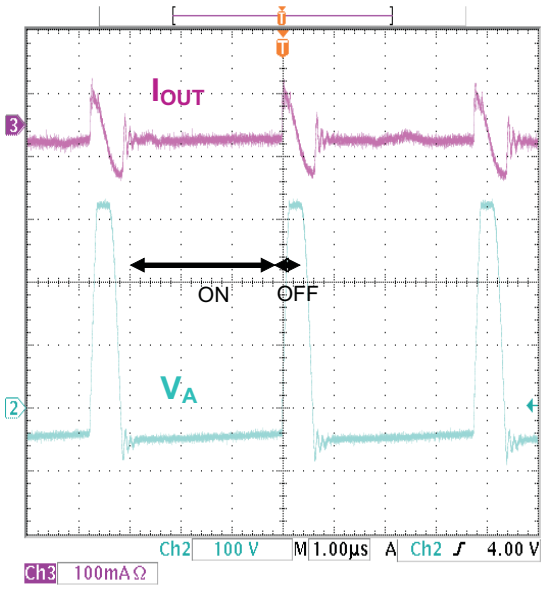


Figure 8. Waveform (Secondary Side)

2.1.3 How to Define Peak Primary Current

The I_PEAK pin of the TPS65560/TPS65561 is used to define the peak current in the primary of the transformer. The programmable range is from 0.8 A to 1.8 A. The I_PEAK input is treated as a logic input when its voltage is below $V_{(PKL)}$ (0.6 V) and above $V_{(PKH)}$ (2.4 V). If the input is less than $V_{(PKL)}$ or more than $V_{(PKH)}$, the value of the peak current is equal to $I_{(PEAK1)}$ or $I_{(PEAK2)}$ (see Figure 9). $I_{(PEAK1)}$ and $I_{(PEAK2)}$ are specified in the data sheet. For voltages between $V_{(PKL)}$ and $V_{(PKH)}$, I_PEAK input is treated as analog input. Typical usages of the variable primary current include:

- Changing I_PEAK depending on the battery capacity. For example, I_PEAK can be set high when the battery is fully charged and can supply the most current. As the battery discharges, I_PEAK can be decreased to reduce the amount of peak current the battery needs to supply.
- I_PEAK can be used for active power management. For example, I_PEAK can be reduced when the lenses' zoom motor is operating to avoid excessive current draw on the battery.

The voltage on the I_PEAK pin (V_PEAK) can be controlled in three ways (see Figure 1).

- Use an external controller, and treat I_PEAK as the logic input pin. This method produces only the two values of peak current, $I_{(PEAK1)}$ and $I_{(PEAK2)}$ (see Figure 9 and Figure 10).
- Use an external controller with a digital-to-analog converter (DAC) to force V_PEAK to follow analog information, such as battery voltage. The DAC can set the voltage on the I_PEAK pin between $V_{(PKL)}$ and $V_{(PKH)}$.
- Use an analog circuit. The function is the same as using a DAC. The voltage on I_PEAK can be set using an analog circuit as shown in Figure 1.

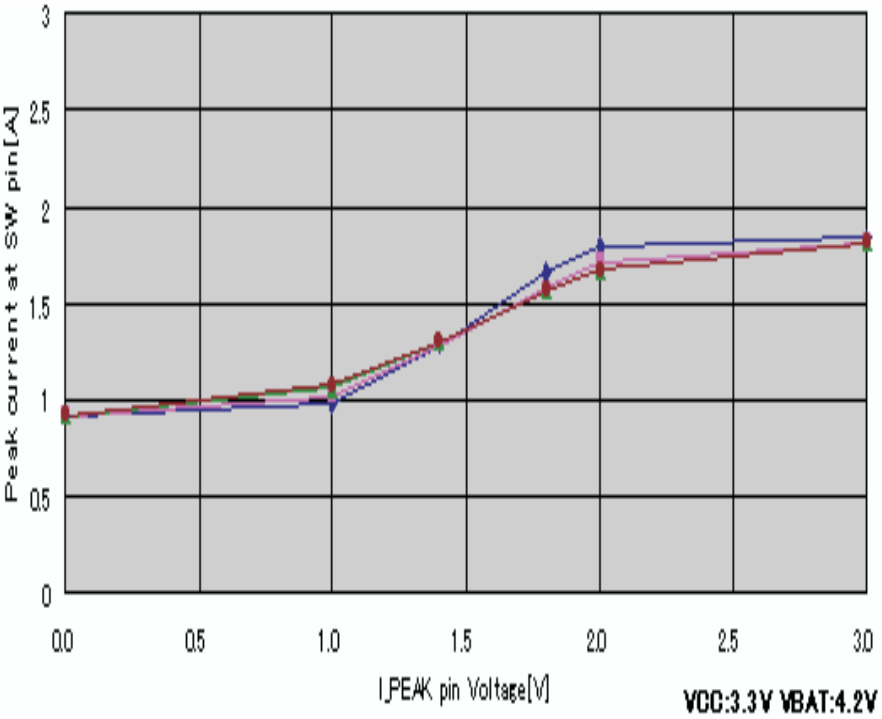


Figure 9. I_{PEAK} Pin Voltage vs Peak Current (TPS65560)

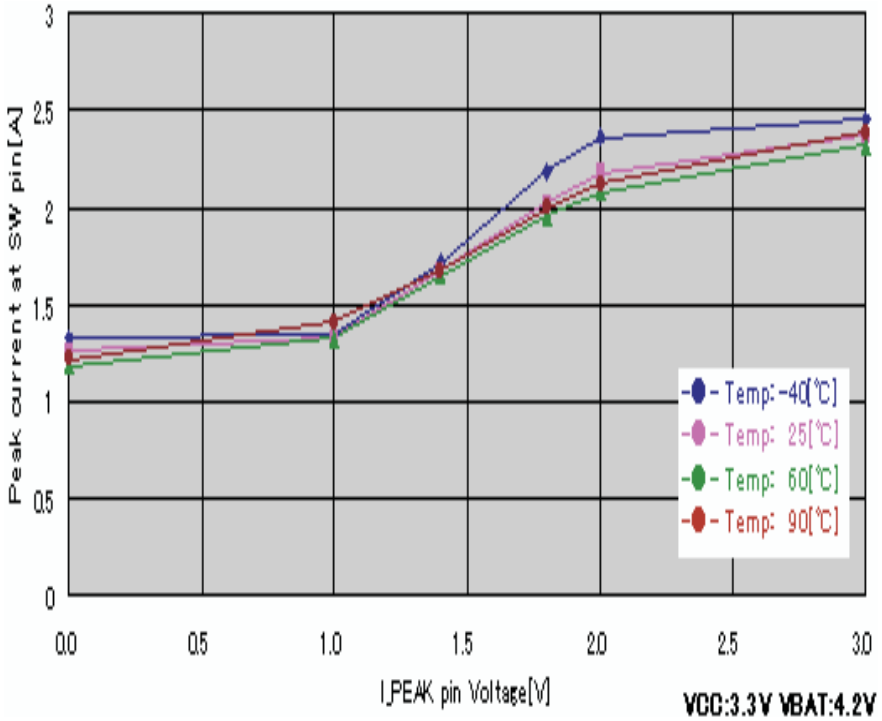


Figure 10. I_{PEAK} Pin Voltage vs Peak Current (TPS65561)

2.1.4 Peak Current Depends on Delay at I_PEAK Comparator

A typical 270-ns delay occurs from the detection of ISW exceeding the target peak current to the turning off the internal FET switch. This means that there is a difference between the target peak current and the actual peak current. Due to this, the actual peak current depends on the inductance of the primary side (see Figure 11) even though the I_PEAK pin voltage is the same. The difference depends on the average current from the battery and the charging time. Section 3.1 discusses the selection of the transformer in detail.

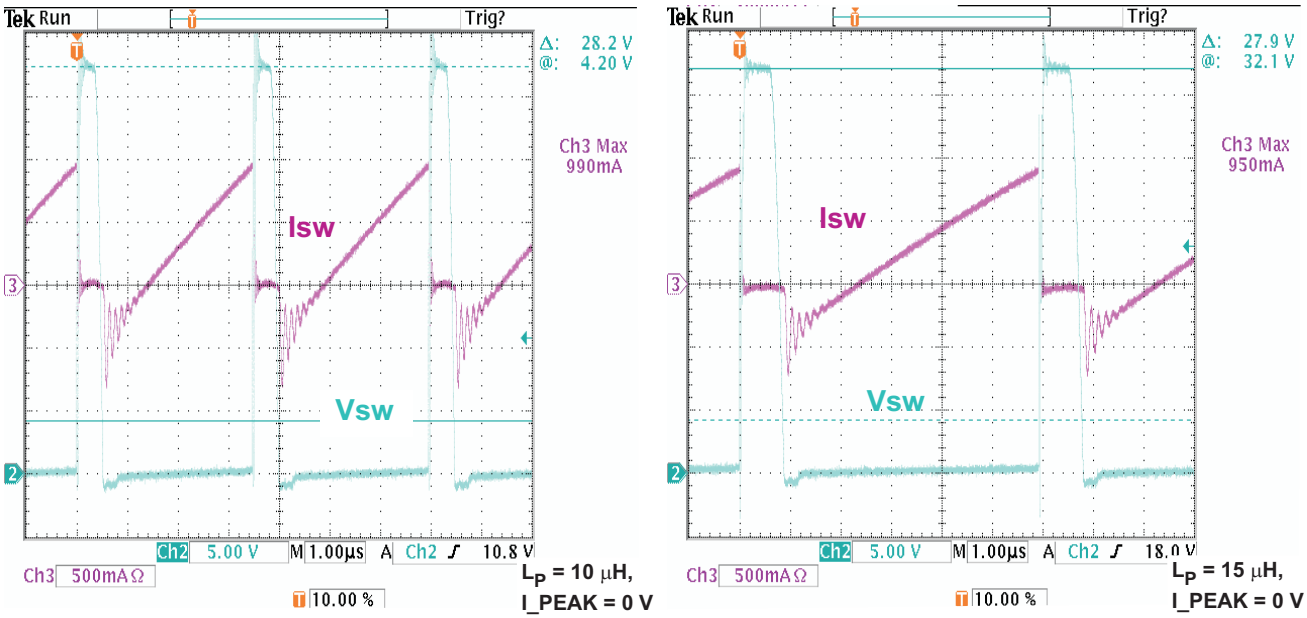


Figure 11. I_PEAK Delay Depends on Primary-Side Inductance

2.1.5 I_PEAK Temperature Characteristic

The temperature characteristic is almost flat (see Figure 12 and Figure 13). This data was measured with the following conditions: VCC: 3.3 V, VBAT: 4.2 V, primary inductance of transformer: 15 µH.

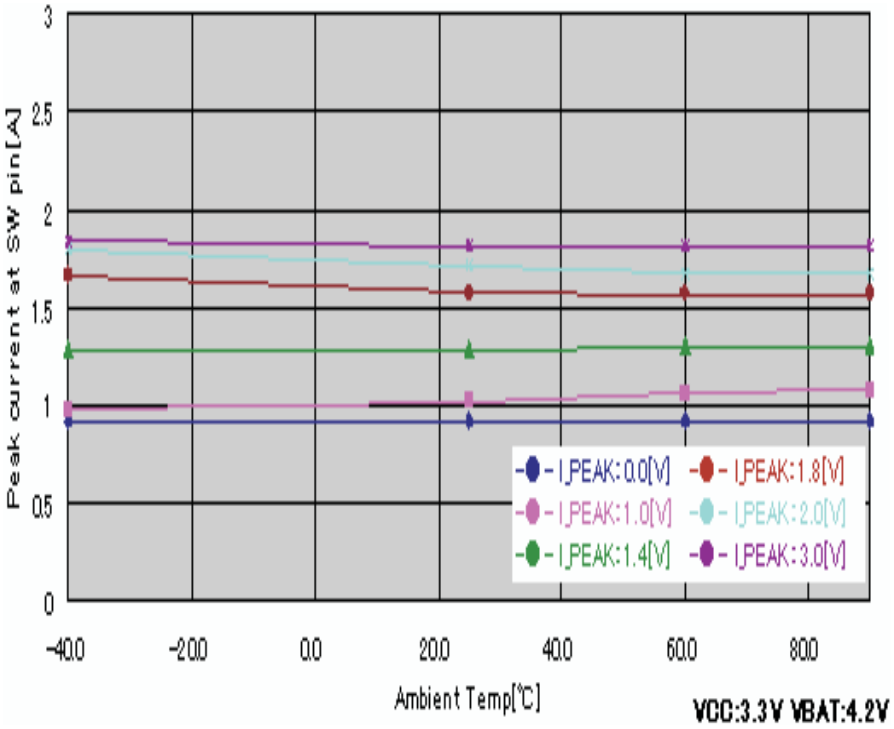


Figure 12. I_PEAK Temperature Characteristic (TPS65560)

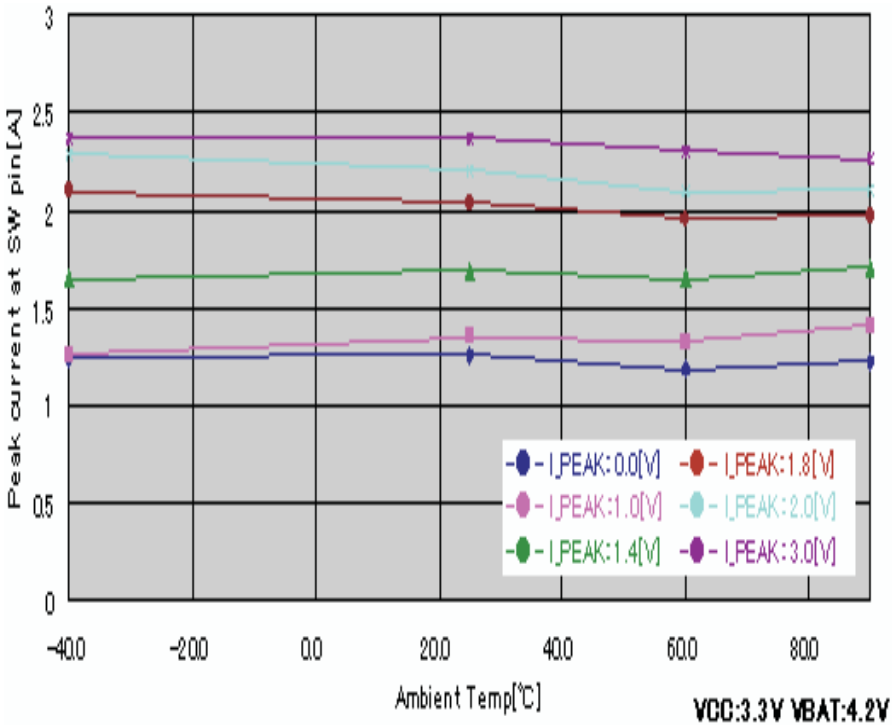


Figure 13. I_PEAK Temperature Characteristic (TPS65561)

2.1.6 Charge Status Indicator

The TPS65560/TPS65561 drive the charge complete indicator, XFULL, low when the charging operation is complete. To communicate to a controller that the charging is complete, connect the XFULL pin to the controller with a pullup resistor (see Figure 14). It is strongly recommended that the CHG pin be set to low immediately after the charging is complete. The XFULL output can also be used to drive a LED to provide a visual indication of charging status. Simply connect the anode to the interface voltage ($V_{I/F}$) and the cathode to XFULL (see Figure 15).

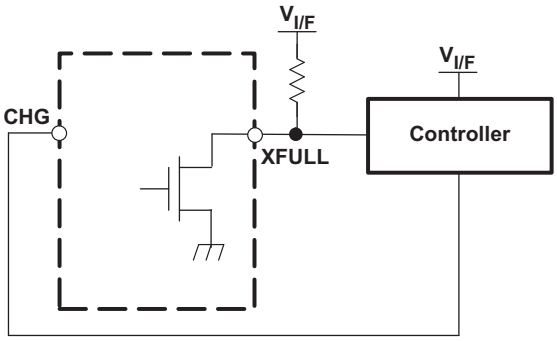


Figure 14. Connect Controller to XFULL

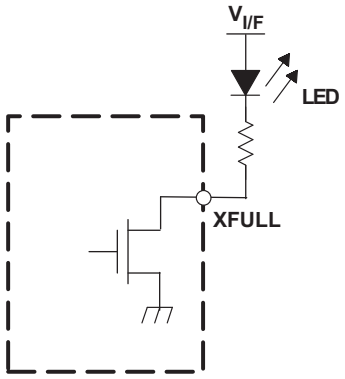


Figure 15. Connect LED to XFULL

The XFULL output is configured as an open-drain MOSFET (see Figure 2). The MOSFET has a low current sink capacity. The current sink capacity of XFULL is shown in Figure 16.

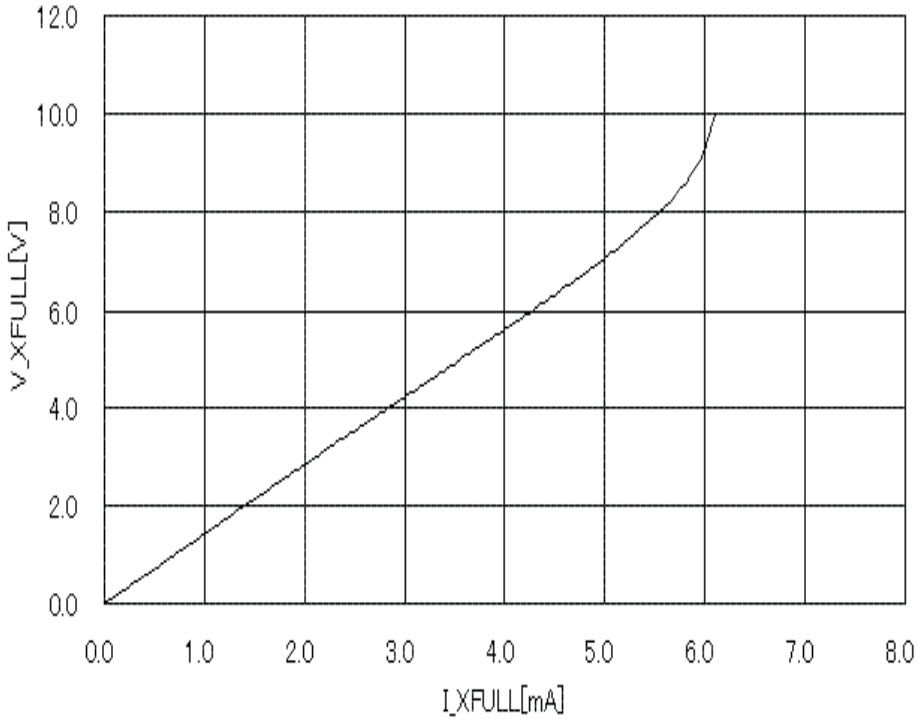


Figure 16. I_XFULL vs V_FULL

2.1.7 How to Use Integrated IGBT Driver to Flash Xenon Lamp

The TPS65560/TPS65561 have an integrated IGBT driver to drive the gate of IGBT for a lamp trigger circuit. Once the photo flash capacitor is charged, the F_ON pin is switched from Low to High to activate the lamp trigger. The CHG pin must remain at GND level when the F_ON pin is switched to High to fire the photo flash. The TPS65560/TPS65561 have a mask filter (see Figure 17). This mask filter provides some noise immunity for the CHG pin when the xenon lamp is flashing.

The TPS65560/TPS65561 have internal pullup and pulldown resistors as shown in Figure 18; these values are specified in each data sheet (SLVS608 and SLVS691). IGBTs are sensitive to fast turnoff times. To achieve a slower turnoff time, the TPS65560/TPS65561 have integrated pullup and pulldown resistors. The recommended rate of turnoff time should be verified with the IGBT data sheet. An additional series resistor can be added between the G_IGBT pin and the gate of the IGBT if slower turnoff times are required. See the TPS65560/TPS65561 data sheets to select the suitable value of pullup and pulldown resistors.

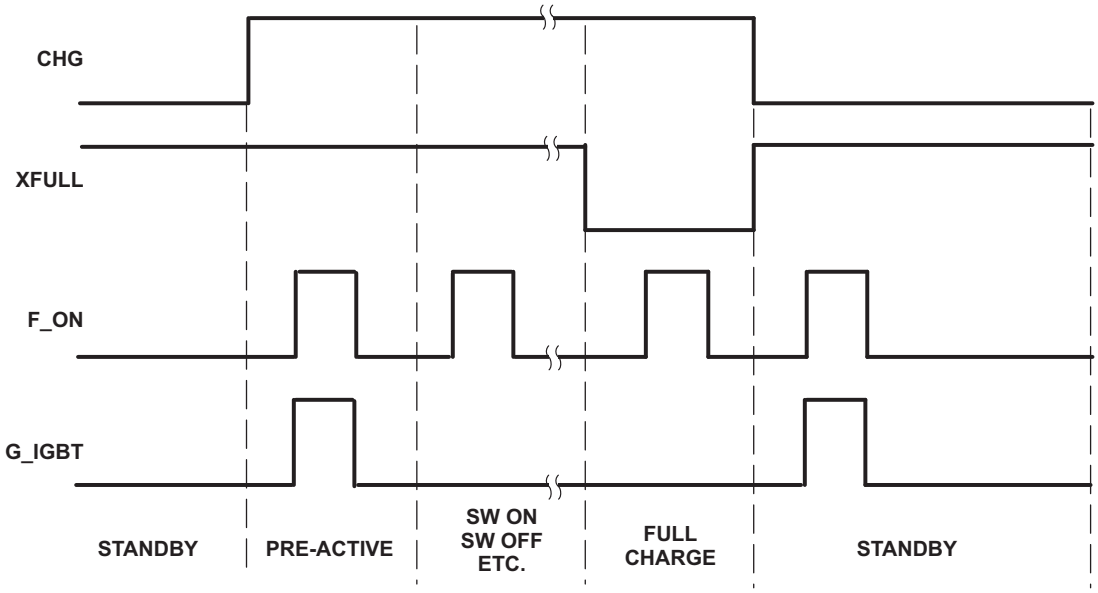


Figure 17. Relationship Between CHG Signal and F_ON Signal

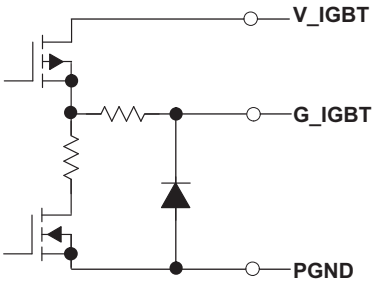


Figure 18. Equivalent Circuits of IGBT Driver

2.1.8 Protections

The TPS65560/TPS65561 photo flash chargers have four forms of protections: MAX ON TIME, MAX OFF TIME, OVER VDS SHUTDOWN, and THERMAL DISABLE.

- MAX ON TIME

  To prevent a condition, such as pulling too much current from a high-impedance power source (i.e., an almost empty battery) and never reaching peak current, the TPS65560/TPS65561 provide a maximum ON TIME function. If the ON TIME exceeds t_{MAX}, the SW pin of the TPS65560/TPS65561 are forced off, regardless of the target current defined by I_PEAK pin voltage. t_{MAX} typically is designed to be 100 µs.
- MAX OFF TIME

  To prevent a condition such as never increasing the voltage at the SW pin when the internal FET switch is OFF, the TPS65560/TPS65561 provide a maximum OFF TIME function. If the OFF TIME exceeds t_{MIN}, the TPS65560/TPS65561 are forced on, regardless of V_{ZERO} detection. t_{MIN} typically is designed to be 50 µs.
- OVER VDS SHUTDOWN

  The TPS65560/TPS65561 provide an overvoltage monitoring function of the SW pin. The TPS65560/TPS65561 are latched off if the voltage on the SW pin is above OV_{DS} during the switch ON TIME (see Figure 5). This function protects excessive current from flowing through the SW pin to PGND. The device could be damaged if not protected. The typical OV_{DS} limit is defined in the TPS65560/TPS65561 data sheets.
- THERMAL DISABLE

  If the junction temperature of the TPS65560/TPS65561 exceeds 150°C, all functions stop (see Figure 19). If the level of the CHG pin is high, the device automatically restarts when its temperature has dropped below the threshold (see Figure 20).

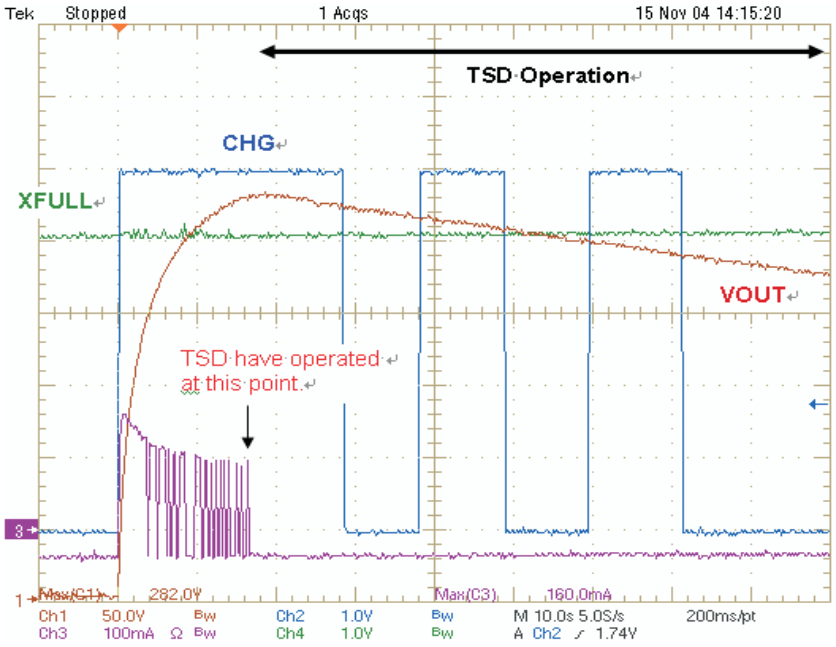


Figure 19. TSD Operation

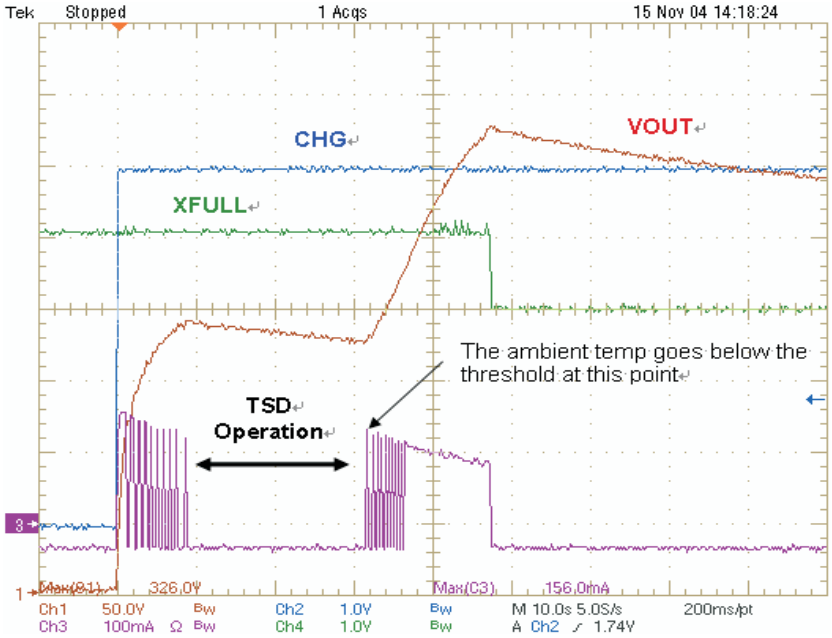


Figure 20. Charging Automatically Restarts When Ambient Temperature Reaches Threshold

2.2 How to Calculate Average Current

Average current from the battery is the key for efficiency and charging time. Equation 3 and Equation 4 show the method of the calculation for average current from the battery.

At one switching, the charge coming from the battery is calculated as shown in Equation 3:

$$\Delta Q = \int \frac{V_{BAT}}{L_P} dt = \frac{V_{BAT}}{2L_P} T^2_{ON(n)} \quad (3)$$

Where:

ΔQ = The charge coming from the battery at one switching
L_P = Primary inductance
V_{BAT} = Battery voltage
Trr(n) = On time at n cycle switching

The average current from the battery is calculated as shown in Equation 4:

$$I_{BATave} = \int_0^{T_C} \frac{\Delta Q}{T_{ON(n)} + T_{OFF(n)}} dt \quad (4)$$

Where:

T_C = Charging time
$T_{ON(n)}$ = ON time at n cycle switching
$T_{OFF(n)}$ = OFF time at an cycle switching
I_{BATave} = Average current from battery

2.3 Efficiency

Efficiency is defined as the output power divided by the input power (see Equation 5):

$$\eta = \frac{P_{OUT}}{P_{IN}} \quad (5)$$

Where:

η = Efficiency
P_{IN} = Input power
P_{OUT} = Output power

The primary charging power (P_P) charges the primary-side inductor. It is calculated as shown in Equation 6:

$$P_P = V_{BAT} \times I_{BATave} \quad (6)$$

Where:

V_{BAT} = Battery voltage
I_{BATave} = Average current from battery

The secondary discharging power (P_S) is equal to the energy discharged by the photo flash capacitor. It is calculated as shown in Equation 7:

$$P_S = \frac{1}{2 \times T} C_{OUT} \times \left(V_{OUT} - V_{ini}\right)^2 \quad (7)$$

n

Where:

C_{OUT} = Capacitance of photo flash capacitor
V_{OUT} = Output voltage after charging
V_{ini} = Output voltage before charging
T = Charging time

Therefore, efficiency is calculated as shown in Equation 8:

$$\eta = \frac{P_S}{P_P} = \left(\frac{1}{2} C_{OUT} - \left(V_{OUT} - V_{ini}\right)^2\right) / V_{VBAT} \times I_{BATave} \times T \quad (8)$$

Equation 8 computes measured efficiency with ideal conditions. However, the efficiency also depends on parameters such as DC resistance of the transformer, battery line impedance, and reverse recovery time (Trr) of the diode. These can be checked by using a target output voltage (V_{OUT}) of 320 V and a photo flash capacitor (C_{OUT}) of 120 µF. The actual efficiency can be measured with two parameters, battery voltage and I_PEAK pin voltage (see Figure 21 and Figure 22).

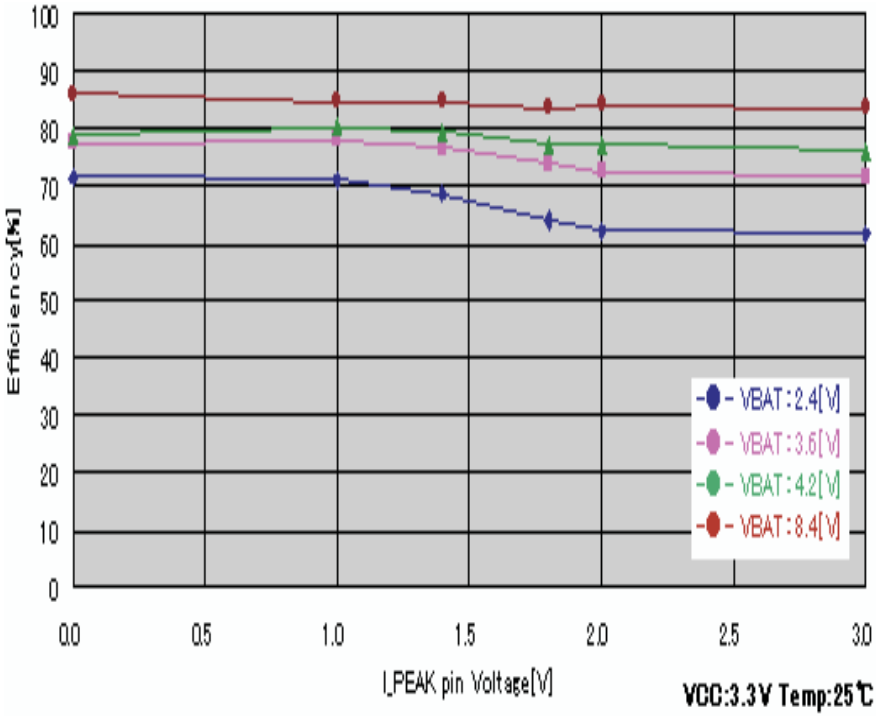


Figure 21. Efficiency at VCC 3.3 V (TPS65560)

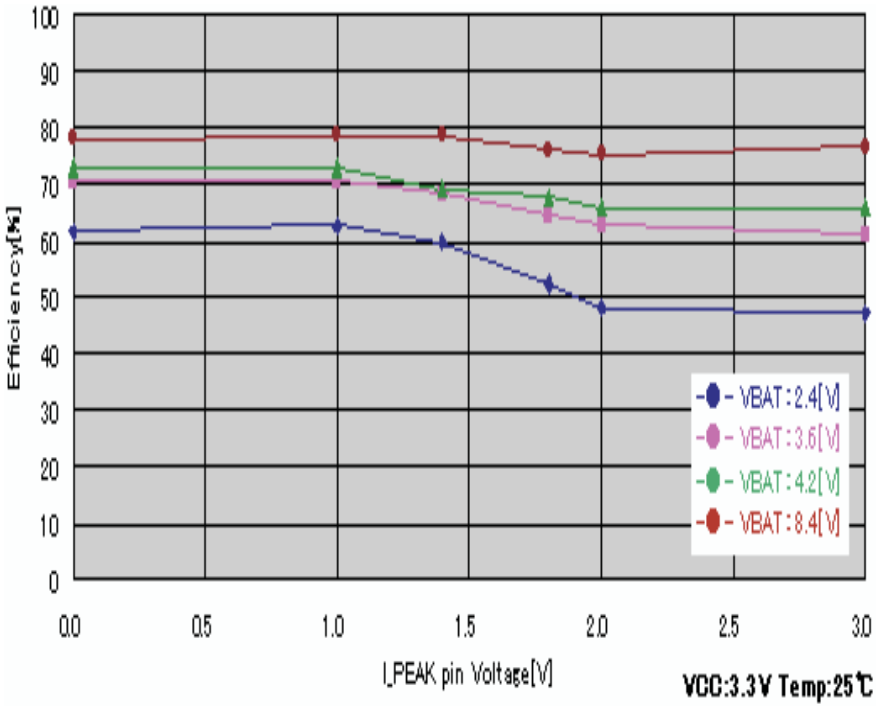


Figure 22. Efficiency at VCC 3.3 V (TPS65561)

2.4 Charging Time

Charging time is one of the most important factors of the photo flash charger. It depends on the average current from the battery, battery voltage (V_{BAT}), target output voltage (V_{OUT}), photo flash capacitor (C_{OUT}), and the efficiency (η). Average input current from the battery depends on the peak current in the primary side.

The difference in output voltage with one switching cycle (ΔV_{OUT}) is calculated as shown in Equation 9:

$$\Delta V_{OUT} \approx \frac{\Delta E_{IN}}{C_{OUT} V_{OUT(n)}} = \frac{1}{2} \times \frac{\eta}{C_{OUT} V_{OUT(n)}} \times L_P \times I\_PEAK^2 \quad (9)$$

Where:

I_PEAK = Peak current at primary side
η = Efficiency
C_{OUT} = Capacitance of photo flash capacitor
$V_{OUT(n)}$ = Output voltage at n cycle switching
L_P = Primary inductance

To improve the charging time, the following items are important:

- Efficiency

  The higher the efficiency, the better and faster the charging time. The efficiency depends on the following items:

  – Transformer

    The efficiency depends on the copper loss and the core losses in the transformer. Larger diameter wire is the only way to reduce the copper losses. This means that the size of the transformer must be larger.

    Changing the core material to another material with better frequency characteristics, increasing the effective core area, or increasing the number of turns in the winding all can reduce the core losses. But, this can also increase the size of the transformer.

  – Line impedance

    To improve the efficiency, the line impedance should be reduced as much as possible. This can be accomplished by using wide traces on the circuit board.

  – Diode

    The efficiency depends on the parametric capacitor and the reverse recovery time:

- Average current from battery

  The larger the average current, the faster the charging time. Efficiency depends on the following items:

  – Diode

    The efficiency depends on the parametric capacitor and the reverse recovery time.

  – Primary inductance

    As section 2.1.4 shows, this relates to the peak current on the primary side. To avoid the influence of I_PEAK delay, a larger inductance is recommended. From the efficiency point of view, a range from 7 µH to 15 µH is recommended.

- Photo flash capacitor/target output voltage

  A smaller output voltage value effectively reduces the charging time, but this value depends on the brightness of the xenon lamp and the flash brightness depends on the energy stored in the capacitor. The required flash intensity should be initially defined.

These can be checked with a target output voltage (V_{OUT}) of a 320-V photo flash capacitor (C_{OUT}) of 120 µF. The actual efficiency can be measured with two parameters—battery voltage and I_PEAK pin voltage (see Figure 23 and Figure 24).

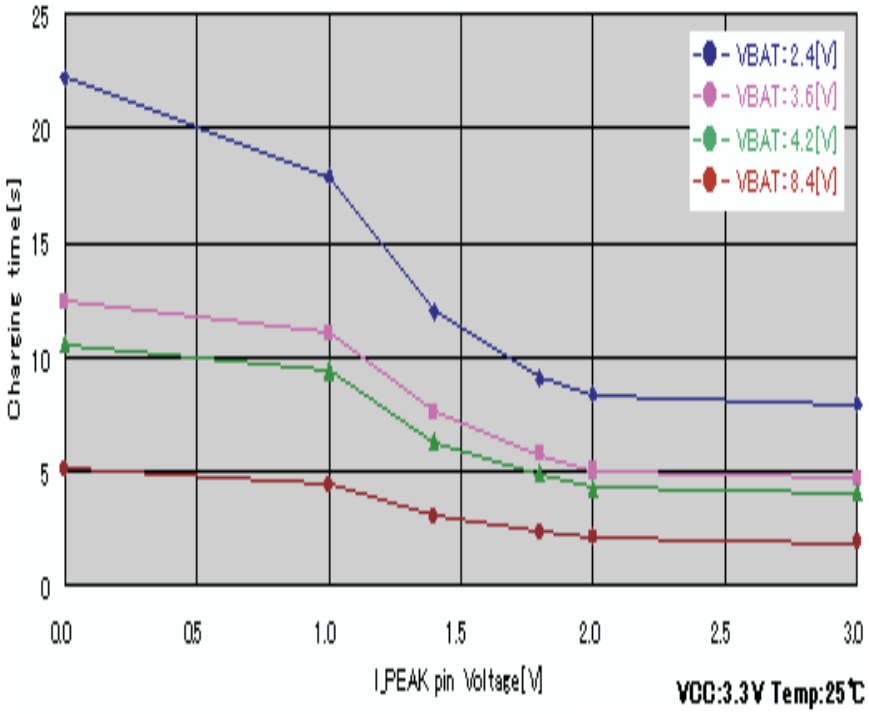


Figure 23. Charging Time at VCC 3 V (TPS65560)

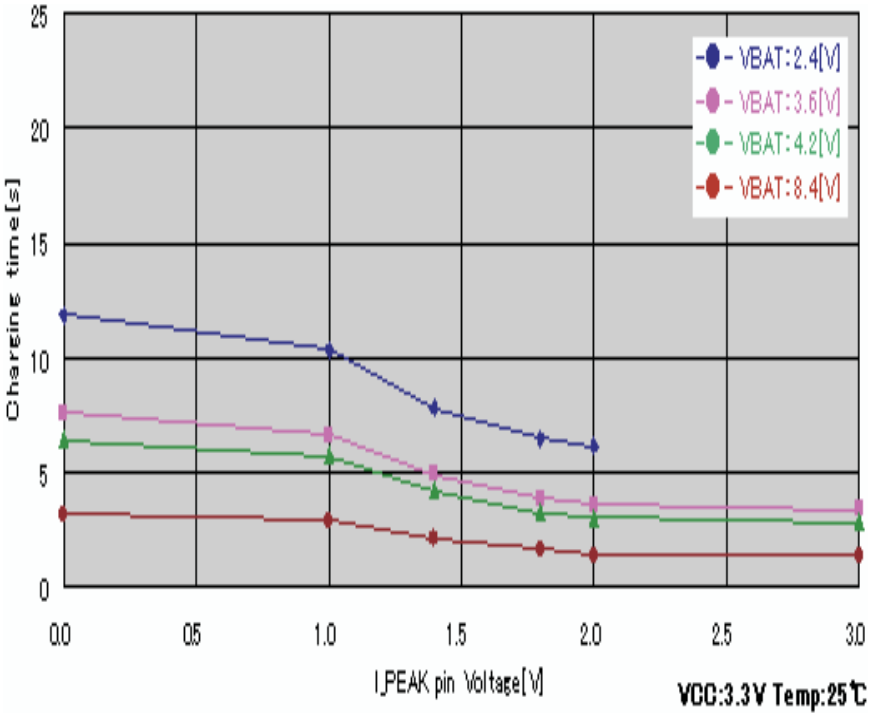


Figure 24. Charging Time at VCC 3 V (TPS65561)

3 How to Select External Components

3.1 How to Select a Transformer

The transformer is the key component for faster charging and higher efficiency. The following discussion provides useful information for selecting a transformer.

3.1.1 How to Determine Turn Ratio and Primary Inductance

First, determine the desired target output voltage, which depends on the desired brightness of the flash. After that, the turn ratio of transformer (N) is calculated by Equation 10. The recommended range of the turn ratio of transformer is from 10 to 12.

$$N = \frac{V_{OUT} + V_D}{V\_FULL} \tag{10}$$

Where:

N = Turn ratio of transformer
V_{OUT} = Target output voltage
V_O = Forward diode voltage
V_FULL = Primary target voltage

Next, determine the peak current value on the primary side to determine the voltage on the I_PEAK pin (see Section 2.1.3). The transformer's primary inductance can be calculated using Equation 11 after choosing the peak current.

$$\frac{V_{OUT} \times T_{OFF\ MIN}}{N \times I\_PEAK} \le L_P \le 600\ [\mu H] \tag{11}$$

Where:

V_{OUT} = Target output voltage
$T_{OFF\ MIN}$ = Minimum OFF time just before reaching the target voltage specified in the data sheet, XFULL after V(SW) exceeds V(FULL).
I_PEAK = Peak current at primary side
N = Turn ratio of transformer
L_P = Primary inductance

The minimum inductance for the primary side is defined by the allowable minimum OFF time ($T_{OFF\ MIN}$) at the target output voltage, and the maximum inductance at the primary side is defined by the MAX ON TIME protection. The recommendation range of primary-side inductance is from 7 µH to 15 µH from an efficiency point of view.

3.1.2 Leakage Inductance

A transformer with too much stray inductance can cause damage to the internal FET due to large voltage spikes (over 50 V) at the SW pin (see Figure 25).

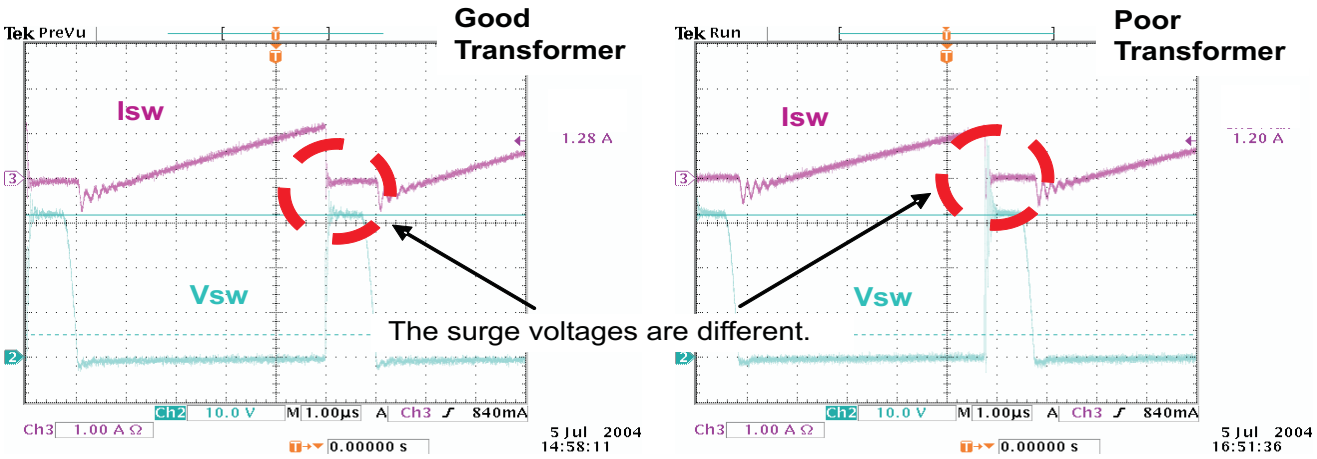


Figure 25. Surge Voltage at SW Pin

The leakage inductance of the transformer is determined by the coefficient of coupling, K, of the transformer (see Equation 12). For best results, the coefficient coupling should be more than 0.97.

$$K = \frac{L_P - L_{PL}}{L_P} \tag{12}$$

Where:

L_P = Primary inductance
L_{PL} = Primary leakage inductance

Table 1 shows the allowable maximum leakage inductance to protect the internal FET switch from inductive spikes when the internal FET switch turned OFF.

Table 1. Guideline About Leakage Inductance

I_PEAK RANGE (A)	MAXIMUM LEAKAGE INDUCTANCE [µH]
<1.1	0.20
1.1 to 1.3	0.16
1.3 to 1.5	0.14
1.5 to 1.8	0.12
>1.8	0.11

3.1.3 DC Resistance

The dc resistance is determined by the number of turns of wire in the transformer and the wire's cross-sectional area. A higher dc resistance increases the overall losses of the transformer. To get higher efficiency, select the transformer with the lower dc resistance.

3.1.4 Recommended Transformers

Table 2 and Table 3 are recommended transformers for the TPS65560.

Table 2. Recommended Transformers[1] (Tokyo Coil Engineering)

TYPE NUMBER	SIZE W × D × H (mm)	L_P (µH)	I_{SW} (Max) (A)	R_{PRI} (mΩ)	R_{SEC} (Ω)	TURN RATIO
TTRN-060S-015	6,8 × 8 × 5	14	2	200	18	1:10
TTRN-060S-014						1:11
TTRN-060S-016					21	1:12
TTRN-038S-009	6,5 × 6,4 × 4	14	1.3	86	15	1:10
TTRN-038S-006						1:11
TTRN-038S-010					18	1:12
TTRN-038S-011	6,5 × 6,4 × 4	7	2	86	10	1:10
TTRN-038S-007						1:11
TTRN-038S-012					11	1:12

(1) These values are the reference for designing.

General Enquiry (Tokyo Coil Engineering)

TEL: +81-426-56-6262
FAX: +81-426-56-6336
E-mail: tce@tokyo-coil.co.jp
Web: http://www.tokyo-coil.co.jp/

Table 3. Recommended Transformers (Kijima-musen)[1]

TYPE NUMBER	SIZE W × D × H (mm)	L_P (µH)	I_{SW} (Max) (A)	R_{PRI} (mΩ)	R_{SEC} (Ω)	TURN RATIO
SBTI-5.6-1	6,3 × 5,6 × 4	9.5	1.8	106	24.22	1:10
SBTI-5.6-2				117	26.46	1:11
SBTI-5.6-3				105	36.56	1:12

(1) These values are the reference for designing.

General Enquiry (Kijima-musen)

TEL: +81-3-3755-1101
FAX: +81-3-3755-5577
E-mail: sale@kijima-m.co.jp

3.2 How to Select a Diode

3.2.1 Principle of Reverse Current

The most important factor in selecting a diode is the reverse recovery time (Trr). Trr influences the charging time and the efficiency. During Trr, the current in the secondary side should be flowing from the capacitor to the transformer. The mechanism of reverse current is described in the following steps (see Figure 26 and Figure 27).

1. Internal FET switch = ON

   When the internal FET switch is ON, the primary current is flowing forward and starts charging. The voltage at the secondary side reverse biases the diode, so it is OFF and no current flows.

2. Internal FET switch turns OFF

   When the internal FET switch turns OFF, the primary current stops flowing and the voltage at the secondary side becomes positive, thus, forward biasing the diode, the diode turns ON, and secondary current flows to the photo flash capacitor.

3. ETRANS is almost zero and reverse current flows.

   Energy charging of the primary side (E_{TRANS}) decreases to almost zero. When this happens, the internal FET switch turns ON. However, the diode cannot immediately turn OFF because of the

reverse recovery time. Hence, reverse current flows through the diode during Trr. When current finally flows forward in the diode, the voltage on the primary side reduces to less than zero, approximately –0.7 V.

4. Recovery diode

   When its energy is moved to the photo flash charger, output voltage goes up to about 300 V and reduces the secondary-side voltage. Because of this, the anode voltage goes down and the cathode voltage goes up. The diode enters a recovering condition and recovers after Trr. When its voltage goes to approximately –0.7 V, the body diode of the internal FET switch turns ON. Its voltage goes up to GND. After Trr, the diode recovers and the reverse current stops.

The selection of a slow Trr diode results in high power consumption in the diode because of reverse current flow. Consequently, high diode power consumption results in slow charging times. To obtain faster charging time and efficiency, select a faster Trr if possible.

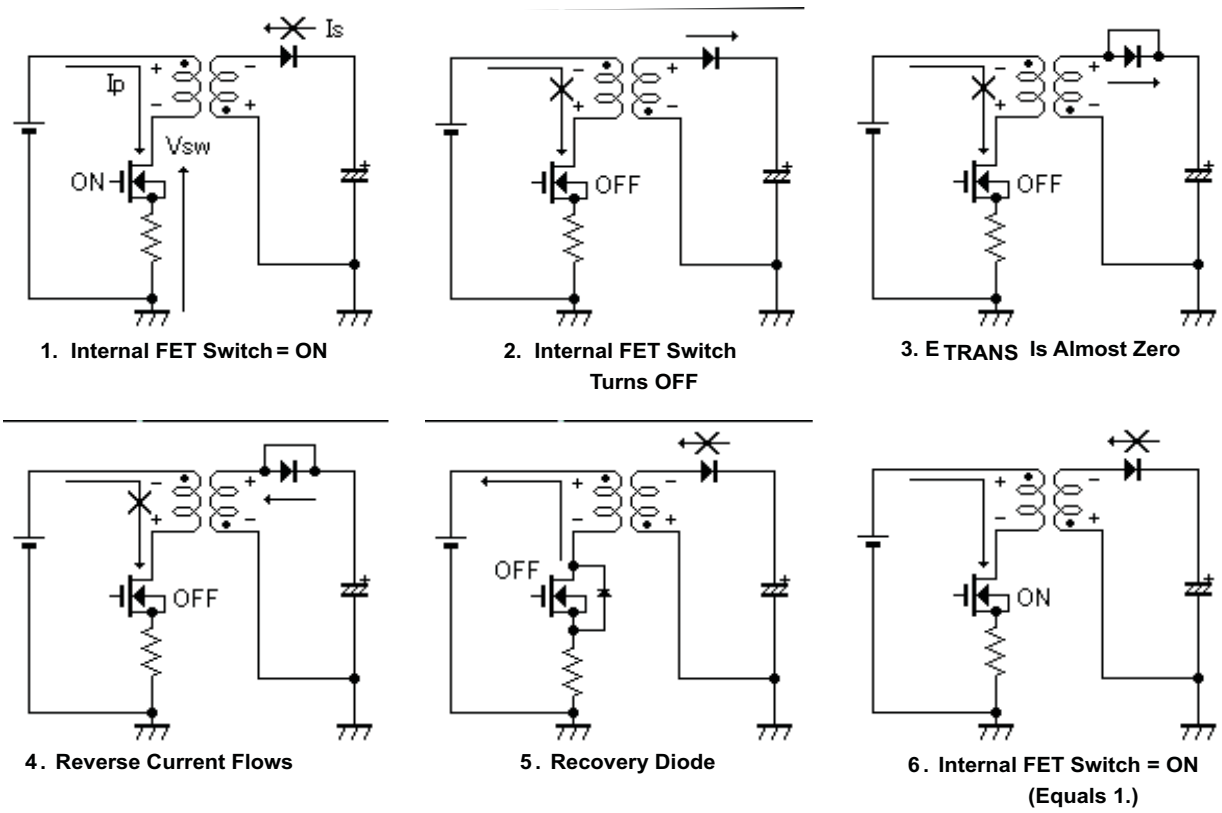


Figure 26. Mechanism of Reverse Current

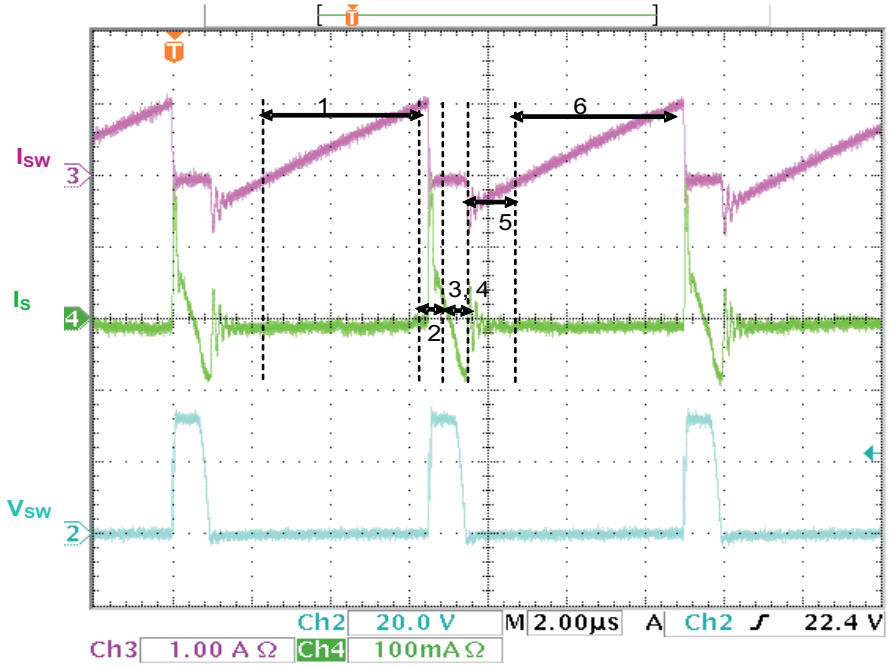


Figure 27. Diagram of Reverse Current

3.2.2 Important Reminders for Selecting Diodes

To select the proper diode for the photo flash charger, consider the following guidelines.

- Use a faster Trr. The recommended value is less than 100 ns.
- Current through the diode must not exceed the absolute maximum current flow of the forward current (I_{DIODE}). I_{DIODE} can be calculated using Equation 13.

$$I_{diode} = \frac{I\_PEAK}{N} \quad (13)$$

I_PEAK = Peak current at primary side
N = Turn ratio of transformer

- The absolute maximum reverse voltage (VR) must not be exceeded. VR can be calculated using Equation 14. The recommended value is more than 600 V.

$$V_R = V_{OUT} + N \times V_{BAT} \quad (14)$$

V_{OUT} = Output voltage
V_{BAT} = Battery voltage
N = Turn ratio of transformer

Recommended diodes are shown in Table 4 and Table 5.

Table 4. Recommended Diodes (Origin Electric)

TYPE NUMBER	MAX RESERVE VOLTAGE (V)	MAX FORWARD CONTINUOUS CURRENT (A)	Trr (ns)
F1P8	800	0.5	30(1)
FT02P80		0.2	45(1)
FT02U60	600		70(2)

(1) The measured condition is IF = 0.5 A, IR = 1 A.
(2) The measured condition is IF = IR = 100 mA.

General Inquiry (Origin Electric)

TEL: +81-3-5954-9117
FAX: +81-3-5954-9122
E-mail: h_teramoto@origin.jp
Web: http://www.origin.co.jp/

Table 5. Recommended Diodes (Toshiba)

TYPE NUMBER	MAX RESERVE VOLTAGE (V)	MAX FORWARD CONTINUOUS CURRENT (A)	Trr (ns)
	800	0.5	100(1)
	600	0.7	

(1) The measured condition is IF = 0.5 A, IR = 1 A.

General Inquiry (Toshiba)

TEL: +81-3-3457-3464
FAX: +81-3-5444-9356
E-mail: kenji.rikiishi@toshiba.co.jp
Web: http://www.semicon.toshiba.co.jp/

3.3 How to Select Photo Flash Capacitor

Ensure that the photo flash capacitor C_{OUT} is a large-value type compared to that used in a forward converter. This is because the discharging energy of a flyback transformer is greater than that of a forward transformer. Equation 15 shows the computation for determining the photo flash capacitor value. Using a larger value than the one derived by this computation could burn out the flash element.

$$C_1 \leq \frac{2 \times E}{V_{out}^{\ 2}} \tag{15}$$

Where:

C_1 = Photo flash capacitor value
E = Absolute maximum energy for xenon tube
V_{OUT} = Target output voltage

4 PCB Information

The following PCB layout considerations can also result in better performance:

Note 1: Any design factor resulting in a large leakage inductance value on the primary side should be avoided because it can lead to device failure due to overvoltage at the SW pin. The selection of a proper transformer, as discussed in the preceding section can reduce leakage inductance (see Section 3.1.2).

Note 2: The loop indicated by dotted lines shown in Figure 28 should be laid out as small as possible to reduce voltage spikes at the SW pin. If this loop is large, the parasitic inductance may cause device failure.

Note 3: The parasitic resistance in the power path from the battery to primary-side turn of the transformer should not be ignored because the large current flows from the battery to primary-side turn of the transformer. The TPS65560/TPS65561 have a single-point ground connection inside the IC at PGND PAD. Therefore, the PCB layout should also keep a single-point ground connection at the PGND terminal of TPS65560/TPS6556. A bypass capacitor (C3 in Figure 28) is required to avoid noise introduced by grounding; the recommended value is 1 µF. Also, the distance from C3 and VCC (PGND) should be minimized.

Note 4: To get an accurate output voltage, two bypass capacitors (C1 and C2 in Figure 28) are required to reduce the noise from the VBAT line. C1 is the bypass capacitor from the V_{BAT} line to PGND; the recommended value is 10 µF. Place it as close as possible to the battery. C2 is the bypass capacitor from the V_{BAT} pin to PGND; the recommended value is 1 µF. Place it as close as possible to the IC.

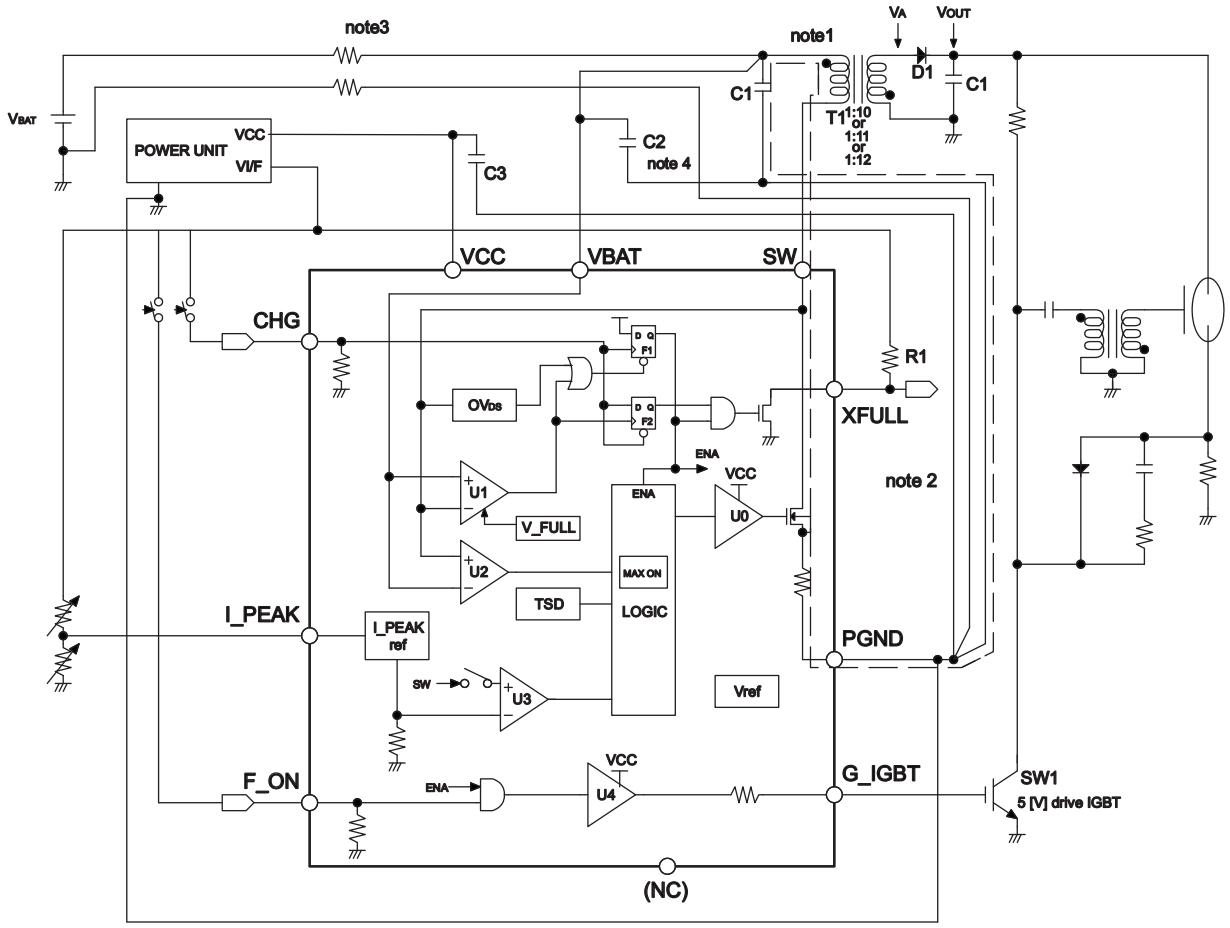


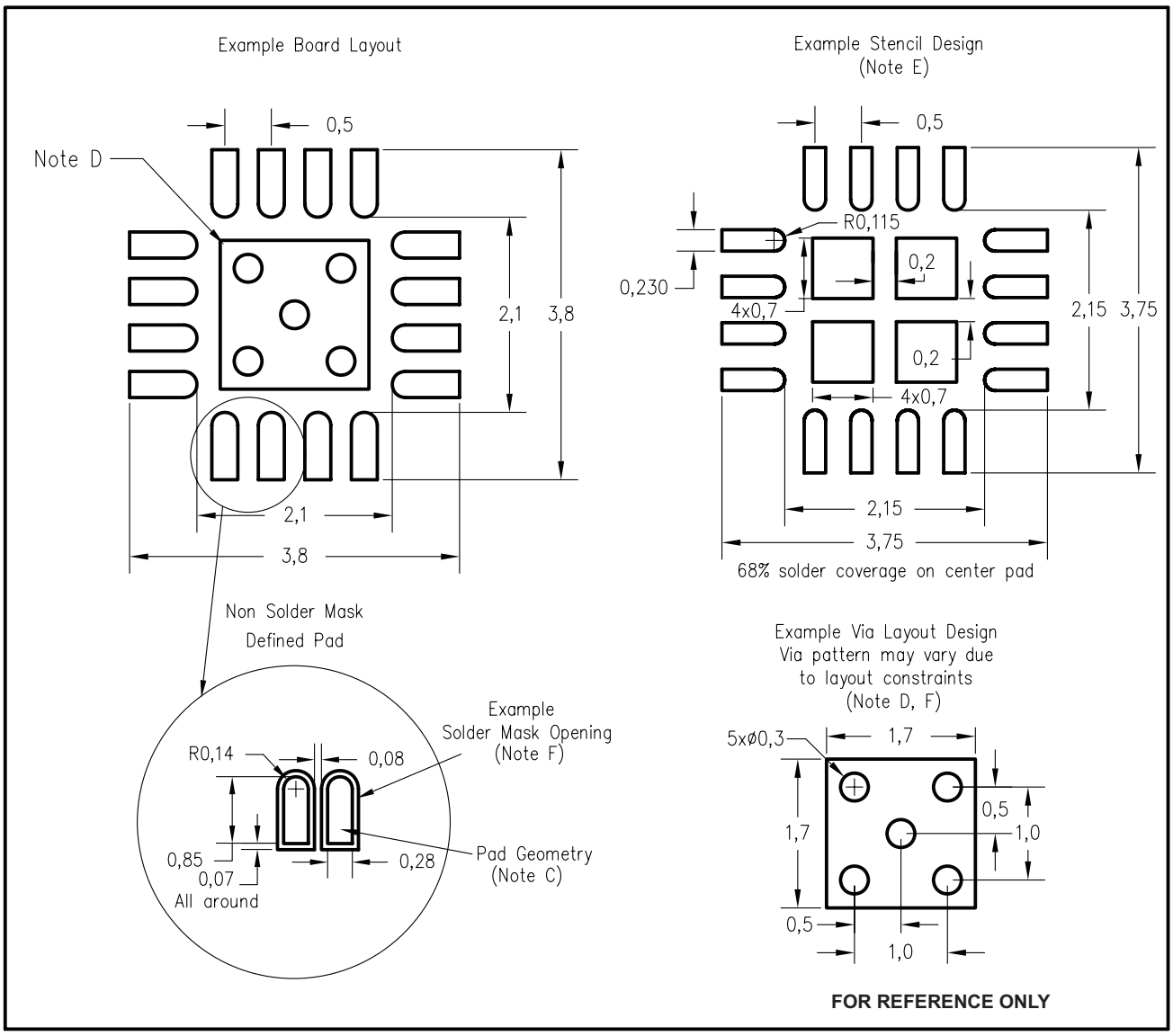
Figure 28. PCB Design Guideline

5 Recommend Foot Pattern Information

FOR REFERENCE ONLY

EXAMPLE LAND PATTERN

RGT (S–PQFP–N16)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

6 Conclusion

This application report demonstrates several advantages of the TPS65560/TPS65561 photo flash chargers:

- These devices can be designed into a smaller area and require few external components because of the integrated IGBT driver.
- The peak current on the primary-side inductor can be set to a maximum of 1.8 A (TPS65560) or 2.2 A (TPS65561) by an external voltage reference. This makes it possible to control battery life and protect against system shutdown by large currents and to change the charging time.
- By selecting the proper external components, it is possible to achieve 70% or greater efficiency and charging times that are less than 4 s with a battery voltage of 4.2 V and the voltage on the I_PEAK pin greater than 2 V for the TPS65560.

To maximize TPS65560/TPS65561 performance:

- Choose a diode with the fastest Trr speed, and select a transformer with the highest coefficient of coupling. These factors influence charging time and efficiency.
- Good system layout of the PCB can result in enhanced performance.

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