4.2 Power supplies requirements and restrictions

The system design must comply with power-up sequence, power-down sequence, and steady state guidelines as described in this section to ensure the reliable operation of the device. Any deviation from these sequences may result in the following situations:

- Excessive current during power-up phase
- Prevention of the device from booting
- Irreversible damage to the processor

4.2.1 Power-up sequence

The device has the following power-up sequence requirements:

- Supply group 0 (SNVS) must be powered first. It is expected that group 0 will typically remain always on after the first power-on.
- Supply group 1 (MAIN and SCU) and group 0 must both be powered to their nominal values prior to boot. They must power up after or simultaneously with group 0.
- Supply group 2 (I/O's and DDR interface) consists of those modules required to start the boot process by accessing external storage devices. These must be fully powered prior to POR release if booting from one of these supplies interfaces. They must power up after or simultaneously with group 1.
- Supply group 3 consists of the remaining portions of the SoC. This includes nonboot I/O voltages and supplies for the major computational units. These can be sequenced in any order and as required to perform the desired functions for the intended application. They must power up after or simultaneously with group 2.

NOTE

The definition of "power-up" refers to a stable voltage operating within the range defined in Table 8. This should be taken into consideration, along with the different capacitive loading on each rail, if considering simultaneous switch-on of the different supply groups.

4.2.2 Power-down sequence

The device processor has the following power-down sequence requirements:

- Supply group 0 must be turned off last, after all other supplies.
- Supply group 1 can be turned off just prior to group 0.

All remaining supplies can be turned off prior to group 1.

NOTE

When switching off supply group 0 (SNVS), VDD_SNVS_LDO_1P8_CAP must be fully discharged to 0 V before starting the next power-up sequence to ensure correct operation.

4.2.3 Power Supplies Usage

The following table shows the power supplies usage by group.

Table 15. Power supplies usage

Supply Groups	Voltage					
Group 0	**2.4 - 4.2v**					
	VDD_SNVS_4P2					
Group 1	**1.0v**	**1.8v**				
	VDD_MAIN	VDD_ANA1_1P8				
	VDD_LVDS**x**_1P0	VDD_ANA2_1P8				
	VDD_MIPI_CSI**x**_1P0	VDD_ANA3_1P8				
	VDD_MIPI_DSI**x**_1P0	VDD_CP_1P8				
	VDD_MIPI_DSI**x**_PLL_1P0	VDD_SCU_1P8				
		VDD_SCU_**x**_1P8				
Group 2	**1.1V**		**1.8v**	**1.8v or 3.3v**	**1.8v or 3.3v switchable**	**3.3v**
	VDD_MEMC		VDD_ADC_DIG_1P8	VDD_EMMC0_1P8_3P3	VDD_USDHC**x**_1P8_3P3	VDD_HDMI_RX0_VH_RX_3P3
	VDD_DDR_CH**x**_VDDQ		VDD_ADC_1P8	VDD_ESAI0_MCLK_1P8_3P3	VDD_SIM0_1P8_3P3	VDD_HDMI_TX0_DIG_3P3
	VDD_DDR_CH**x**_VDDQ_CKE		VDD_ANA0_1P8	VDD_ESAI1_SPDIF_SPI_1P8_3P3		VDD_USB_OTG**x**_3P3
			VDD_DDR_CH**x**_VDDA_PLL_1P8	VDD_FLEXCAN_1P8_3P3		VDD_USB_SS3_TC_3P3
			VDD_HDMI_**x**_1P8	VDD_LVDS_DIG_1P8_3P3		
			VDD_LVDS**x**_1P8	VDD_M4_GPT_UART_1P8_3P3		
			VDD_MIPI_CSI_DIG_1P8	VDD_MIPI_DSI_DIG_1P8_3P3		
			VDD_MIPI_**x**_1P8	VDD_MLB_DIG_1P8_3P3		
			VDD_MLB_1P8	VDD_PCIE_DIG_1P8_3P3		
			VDD_PCIE_SATA0_PLL_1P8	VDD_QSPI**x**_1P8_3P3		
			VDD_PCIE_**x**_1P8	VDD_SPI_SAI_1P8_3P3		
			VDD_PCIE**x**_PLL_1P8	VDD_USDHC_VSELECT_1P8_3P3		
			VDD_USB_HSIC0_1P8			
Group 3	**1.1 - 1.1v**	**1.0v internal LDO's**	**1.2v**	**1.8v or 2.5v or 3.3v**		
	VDD_A53	VDD_HDMI_TX0_1P0	VDD_USB_HSIC0_1P2	VDD_ENET_MDIO_1P8_3P3		
	VDD_A72	VDD_PCIE_SATA0_1P0		VDD_ENET0_1P8_3P3		
				VDD_ENET1_1P8_2P5_3P3		
	VDD_GPU**x**	VDD_PCIE**x**_1P0				
		VDD_USB_OTG**x**_1P0				