Intel Agilex® 7 Power Management User Guide

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1. Intel Agilex® 7 Power Management Overview

The Intel Agilex® 7 devices offer smart voltage identification (SmartVID) standard power devices in all speed grades. Fixed-voltage devices are also available, but only in –4 speed grade. All SmartVID standard power devices must be driven by the Power Management BUS (PMBus*)-compliant voltage regulator, operating either in the PMBus master or PMBus slave mode.

This user guide describes the power-optimizing features of the Intel Agilex 7 devices, and the power-up and power-down sequencing requirements for the Intel Agilex 7 devices.

1.1. Power System Design Phases

Power system design is done in the following logical phases.

1.1.1. Choosing a Power Tree

A power tree topology is chosen based on the requirements of your device.

The requirements of the power supply may not yet be known, but you can access the supply voltage and connection requirements from the *Intel Agilex 7 Device Family Pin Connection Guidelines: F-Series and I-Series*.

Related Information

Intel Agilex 7 Device Family Pin Connection Guidelines: F-Series and I-Series
Provides more information about the supply voltage and connection guidelines of each pin for F-Series and I-Series FPGAs.

1.1.2. Power Estimation

The amount of electrical power required by the various device power supplies is estimated using the Intel® FPGA Power and Thermal Calculator tool and the Power Analyzer tool.

As the design evolves to the final configuration, the quality and type of information available improve and the estimation becomes more accurate.

Related Information

Intel FPGA Power and Thermal Calculator User Guide

1.1.3. Power Optimization

The device configuration can be optimized to reduce power.

This step involves the Intel Quartus® Prime software power optimization wizard, the SmartVID feature (available in all Intel Agilex 7 devices except for –4F speed grade), system cooling decisions, and dynamic workload management strategies. This phase may occur several times during the evolution of the system and device design.

1.1.4. Power Generation

Voltage regulator modules (VRMs) are selected based on the power tree and electrical power estimates. VRM selection is critical to producing high-quality power systems with the minimum number and cost of bypass elements.

1.2. Power Supplies

For more information about the supported power supplies and the nominal voltages, refer to the device data sheet.

Related Information

- Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series
  Provides more information about the supported power supplies and the nominal voltages for F-Series and I-Series FPGAs.
- Intel Agilex 7 FPGAs and SoCs Device Data Sheet: M-Series
  Provides more information about the supported power supplies and the nominal voltages for M-Series FPGAs.

2. Intel Agilex 7 Power Basics

2.1. Power Consumption

The total power consumption of the Intel Agilex 7 device consists of the following components:

- Static power—the power that the configured device consumes when powered up but no user clocks are operating, excluding DC bias power of analog blocks, such as I/O and transceiver analog circuitry.
- Dynamic power—the additional power consumption of the device due to signal activity or toggling. Dynamic power is dependent on the operating frequency of your design, applied voltage, and load capacitance, which depends on design connectivity.
- Standby power—the component of active power that is independent of signal activity or toggling. Standby power includes, but is not limited to, I/O and transceiver DC bias power.

Intel Agilex 7 devices minimize static and dynamic power using advanced process optimizations. These optimizations allow Intel Agilex 7 designs to meet specific performance requirements with the lowest possible power.

2.2. Power Estimation Basics

The Intel power analysis features, including the Intel FPGA Power and Thermal Calculator tool and the Intel Quartus Prime software Power Analyzer, give you the ability to estimate power consumption from early design concept through design implementation, as shown in the following figure.

As you provide more details about your design characteristics, estimation accuracy is improved. Intel recommends that you switch from the Intel FPGA Power and Thermal Calculator to the Power Analyzer in the Intel Quartus Prime software once your design is available. The Power Analyzer produces more accurate results because it has more detailed information about your design, including routing and configuration information about all the resources in your design.

The accuracy of the power model is determined on a per-power-rail basis for both the Power Analyzer and the Intel FPGA Power and Thermal Calculator. For most designs, the Power Analyzer and the Intel FPGA Power and Thermal Calculator have the following accuracies, with final power models:

- Power Analyzer—within 10% of silicon for the majority of power rails and the highest power rails, assuming accurate inputs and toggle rates.
- Intel FPGA Power and Thermal Calculator—within 15% of silicon for the majority of power rails and the highest power rails, assuming accurate inputs and toggle rates. Recommended margins are shown in the **Report** tab, only after device power model status is final.

Figure 1. Power Analysis from Design Concept Through Design Implementation

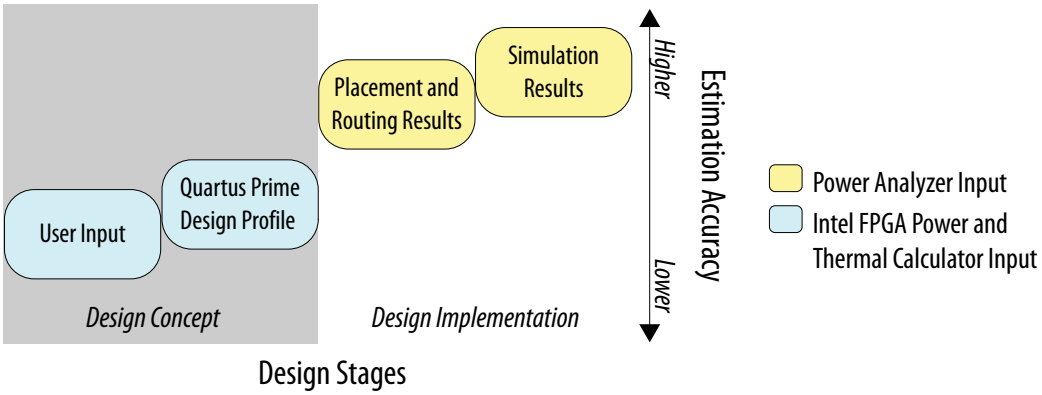


Table 1. Comparison of Intel FPGA Power and Thermal Calculator and Intel Quartus Prime Power Analyzer Capabilities

Characteristic	Intel FPGA Power and Thermal Calculator	Intel Quartus Prime Power Analyzer
When to use	Any time *Note:* For post-fit power analysis, you get better results with the Intel Quartus Prime Power Analyzer.	Post-fit
Software requirements	• The Intel Quartus Prime software • The Intel FPGA Power and Thermal Calculator — Available in a standalone version which offers the same features as the Intel FPGA Power and Thermal Calculator version integrated within the Intel Quartus Prime software	The Intel Quartus Prime software
Accuracy	Medium	Medium to very high
Data inputs	• Resource usage estimates • Clock requirements • Environmental conditions • Toggle rates	• Post-fit design • Clock requirements • Signal activity defaults • Environmental conditions • Register transfer level (RTL) simulation results (optional) • Post-fit simulation results (optional) • Signal activities per node or entity (optional)
Data outputs	• Total thermal power dissipation • Thermal static power • Thermal dynamic power • Off-chip power dissipation • Current drawn from voltage supplies	• Total thermal power dissipation • Thermal static power • Thermal dynamic power • Thermal I/O power • Thermal power by design hierarchy • Thermal power by block type • Thermal power dissipation by clock domain • Off-chip (non-thermal) power dissipation • Current drawn from voltage supplies

2.3. Intel FPGA Power and Thermal Calculator

The Intel FPGA Power and Thermal Calculator results for Intel Agilex 7 devices are based on preliminary simulated data.

The Intel FPGA Power and Thermal Calculator for Intel Agilex 7 devices provides a current and power estimate based on various conditions such as room temperature and nominal voltage.

The Intel FPGA Power and Thermal Calculator calculations are estimates only and shall not be construed as a specification or a guarantee of any kind. The actual currents must be verified during device operation, as this measurement is sensitive to the design implemented in the device and the environmental operating conditions.

Related Information

- Intel FPGA Power and Thermal Calculator User Guide
- Intel FPGA Power and Thermal Calculator Standalone
  Provides standalone Intel FPGA Power and Thermal Calculator tool. This standalone version is available for download from the Intel Download Center for FPGA page under the Additional Software tab.

2.4. Power Analyzer

The Intel Quartus Prime Power Analyzer allows you to estimate power consumption for a post-fit design.

To estimate power consumption before you compile the design, use the Intel FPGA Power and Thermal Calculator.

Related Information

Intel Quartus Prime Pro Edition User Guide: Power Analysis and Optimization

3. Intel Agilex 7 Power and I/O State Sequencing

3.1. Overview

The Intel Agilex 7 devices require a specific power sequence.

This section describes several power management options and discusses proper I/O management during device power up and power down. Design your power supply solution to properly control the complete power sequence. The requirements in this section must be followed to prevent unpredictable current draw to the FPGA device, which can potentially impact the I/O functionality.

Table 2. Power Rails Status for Intel Agilex 7 Devices

Tile	Status
E-Tile	Final
P-Tile	Final
F-Tile	Preliminary
R-Tile	Preliminary

The following descriptors designate the status level currently applicable to the relevant variant:

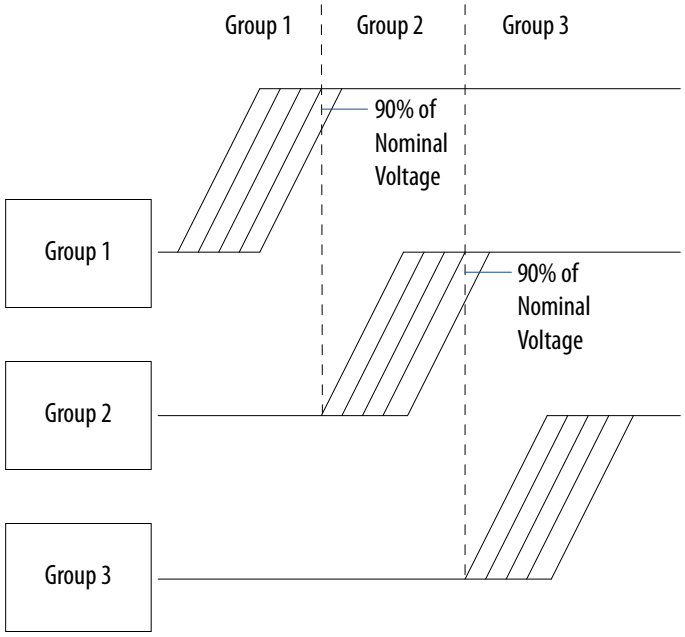
- Preliminary: Information in this document is **subject to change**. Intended for pre-production development, for production designs use with caution.
- Final: Information in this document is intended for use in **production design**.

3.2. Power-Up Sequence Requirements

The power rails in the Intel Agilex 7 devices are divided into three groups.

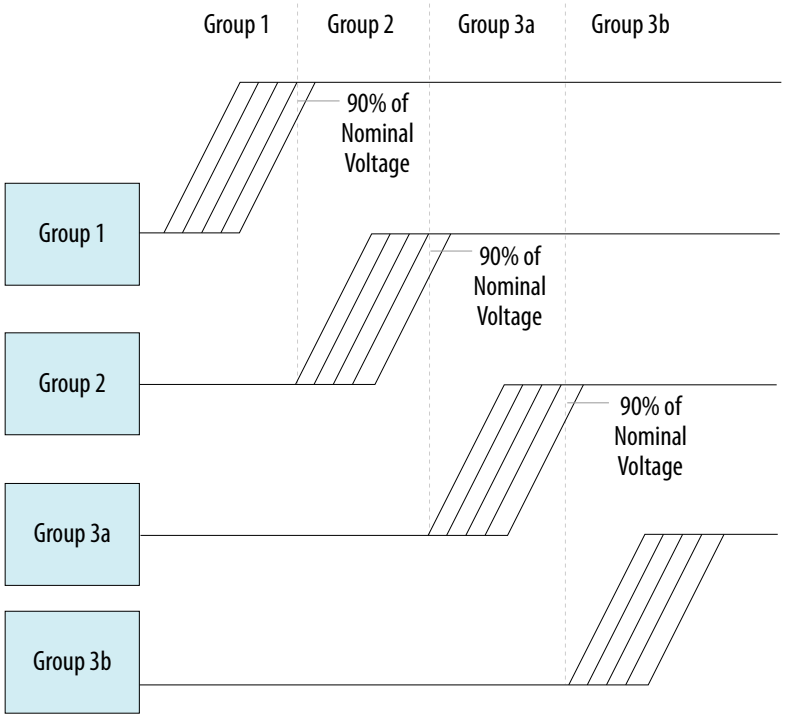
The following figure shows the voltage groups of the Intel Agilex 7 F-Series and I-Series devices and their required power-up sequence.

Figure 2. Power-Up Sequence for the Intel Agilex 7 F-Series and I-Series Devices



The following figure shows the voltage groups of the Intel Agilex 7 M-Series devices and their required power-up sequence.

Figure 3. Power-Up Sequence for the Intel Agilex 7 M-Series Devices



Note: V_{CCBAT} is not in any of the groups below. V_{CCBAT} does not have any sequence requirements. V_{CCBAT} holds the content of the security keys.

For more information about the V_{CCBAT} connection guidelines and power supply sharing guidelines, refer to the *Intel Agilex 7 Device Family Pin Connection Guidelines: F-Series and I-Series*.

Table 3. Voltage Rails Group for the Intel Agilex 7 F-Series and I-Series Devices

Power Group	FPGA Core and Hard Processor System (HPS)	Additional Voltage Rails			
		E-Tile	P-Tile	F-Tile	R-Tile
Group 1	V_{CC} V_{CCP} V_{CCH} V_{CCL_SDM} V_{CCH_SDM} $V_{CCPLLDIG\_SDM}$ V_{CCL_HPS} $V_{CCPLLDIG\_HPS}$	V_{CCRT_GXE} $V_{CC\_HSSI\_GXE}$ (1) $V_{CCRTPLL\_GXE}$	$V_{CC\_HSSI\_GXP}$ V_{CCRT_GXP} V_{CCFUSE_GXP}	$V_{CC\_HSSI\_GXF}$ $V_{CCERT\_FGT\_GXF}$ $V_{CCERT1\_FHT\_GXF}$ $V_{CCERT2\_FHT\_GXF}$	$V_{CC\_HSSI\_GXR}$ $V_{CCE\_PLL\_GXR}$ $V_{CCE\_DTS\_GXR}$ V_{CCRT_GXR}
Group 2	V_{CCPT} V_{CCPLL_SDM} V_{CCADC} V_{CCPLL_HPS}	V_{CCH_GXE} (1) V_{CCCLK_GXE} (1)	V_{CCH_GXP} V_{CCCLK_GXP}	$V_{CCFUSECORE\_GXF}$ $V_{CCFUSEWR\_GXF}$ V_{CCCLK_GXF} $V_{CCH\_FGT\_GXF}$ $V_{CCEHT\_FHT\_GXF}$	V_{CCED_GXR} V_{CCCLK_GXR} $V_{CCH\_FUSE\_GXR}$ V_{CCH_GXR}
Group 3	V_{CCA_PLL} (2) $V_{CCRCORE}$ (2) $V_{CCIO\_PIO\_SDM}$ V_{CCIO_PIO} $V_{CCFUSEWR\_SDM}$ V_{CCIO_SDM} V_{CCIO_HPS}	—	—	—	—

All power rails in Group 1 must ramp up (in any order) to a minimum of 90% of their respective nominal voltage before the power rails from Group 2 can start ramping up. The power rails within Group 2 can ramp up in any order after the last power rail in Group 1 ramps to the minimum threshold of 90% of its nominal voltage. All power rails in Group 2 must ramp to a minimum threshold of 90% of their nominal value before the Group 3 power rails can start ramping up. The power rails within Group 3 can ramp up in any order after the last power rail in Group 2 ramps up to a minimum threshold of 90% of their full value. For more information, refer to the *Intel Agilex 7 Device Family Pin Connection Guidelines: F-Series and I-Series*.

For Intel Agilex 7 devices, there is no power-down sequence requirement, except for Intel Agilex 7 devices with E-tile.

(1) For Intel Agilex 7 devices with E-tile, these voltage rails must follow the power-down sequence. For more information, refer to the *Power-Down Sequence for the Intel Agilex 7 Devices with E-Tile* figure.

(2) For Intel Agilex 7 production devices and ES (except 2486A package) devices, VCCA_PLL and VCCRCORE are part of power Group 3. For Intel Agilex 7 ES (2486A package) devices, VCCA_PLL and VCCRCORE are part of power Group 2.

For Intel Agilex 7 devices without E-tile, Intel recommends that you reverse the power-up sequence when you power down your device to ensure lowest current draw on each voltage supply.

Table 4. Voltage Rails Group for the Intel Agilex 7 M-Series Devices

Group 1	Group 2	Group 3a	Group 3b
• VCC • VCCP • VCCL_SDM • VCCH_SDM • VCCH • VCCPLLDIG_SDM • VCCL_HPS • VCCPLLDIG_HPS • VCCLPLL_NOC • VCCPLLDIG_NOC	F-Tile: • VCCEHT_FHT_GXF	• VCCFUSEWR_SDM • VCCIO_SDM • VCCIO_HPS • VCCPT • VCCPLL_NOC • VCCIO_NOC • VCCPLL_SDM • VCCADC • VCCPLL_HPS	• VCCIO_PIO • VCCN_PIO_SDM • VCCRCORE • VCCIO_UIB
F-Tile: • VCC_HSSI_GXF • VCCFUSECORE_GXF • VCCERT_FGT_GXF • VCCERT1_FHT_GXF • VCCERT2_FHT_GXF • VCCFUSEWR_GXF		F-Tile: • VCCCLK_GXF • VCCH_FGT_GXF	
R-Tile: • VCC_HSSI_GXR • VCCE_PLL_GXR • VCCE_DTS_GXR • VCCRT_GXR • VCCED_GXR • VCCCLK_GXR • VCCH_FUSE_GXR		R-Tile: • VCCH_GXR	
HBM2E: • VCCM_PUMP_HBM			

All power rails in Group 1 must ramp up (in any order) to a minimum of 90% of their respective nominal voltage before the power rails from Group 2 can start ramping up. The power rails within Group 2 can ramp up in any order after the last power rail in Group 1 ramps to the minimum threshold of 90% of its nominal voltage. All power rails in Group 2 must ramp to a minimum threshold of 90% of their nominal value before the Group 3a power rails can start ramping up. All power rails in Group 3a must ramp to a minimum threshold of 90% of their nominal value before the Group 3b power rails can start ramping up.The power rails within Group 3b can ramp up in any order after the last power rail in Group 3a ramps up to a minimum threshold of 90% of their full value. For more information, refer to the *Pin Connection Guidelines*.

All power rails must ramp up and ramp down monotonically. The power-up sequence must meet the POR delay time. For the POR specifications of the Intel Agilex 7 devices, refer to the *POR Specifications* section in the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series*.

For configuration via protocol (CvP), the total t_{RAMP} must be less than 10 ms from the first power supply ramp-up to the last power supply ramp-up. For the t_{RAMP} specifications, refer to the *Recommended Operating Conditions* section in the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series*.

Related Information

- Intel Agilex 7 Device Family Pin Connection Guidelines: F-Series and I-Series
  Provides more information about the power supply sharing guidelines for F-Series and I-Series FPGAs.
- Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series
  Provides more information about the t_{RAMP} and POR specifications for F-Series and I-Series FPGAs.
- Intel Agilex 7 FPGAs and SoCs Device Data Sheet: M-Series
  Provides more information about the t_{RAMP} and POR specifications for M-Series FPGAs.

3.2.1. Guidelines for I/O Pins in GPIO, HPS, and SDM Banks During Power Sequencing

Intel Agilex 7 devices do not support hot-socketing and require a specific power sequence. Design your power supply solution to properly control the complete power sequence.

Adhere to the following guidelines to prevent unnecessary current draw on the I/O pins located in the GPIO, HPS, and SDM banks. These guidelines are applicable for unpowered, power up to POR, POR delay, POR delay to configuration, configuration, initialization, user mode, and power down device states.

- The I/O pins in these banks can be in one the following states:
  - GPIO banks—tri-stated, driven to ground, or driven to the V_{CCIO_PIO} level.
  - HPS banks—tri-stated, driven to ground, or driven to the V_{CCIO_HPS} level.
  - SDM banks—tri-stated, driven to ground, or driven to the V_{CCIO_SDM} level.
- While the Intel Agilex 7 device is powering up or down:
  - The input signals of an I/O pin at all times must not exceed the I/O buffer power supply rail of the bank where the I/O pin resides.
  - If you use a pin in a GPIO bank with 1.5 V V_{CCIO_PIO} (for Intel Agilex 7 F-Series and I-Series) or 1.3 V V_{CCIO_PIO} (for Intel Agilex 7 M-Series), the pin voltage must not exceed the V_{CCIO_PIO} rail or 1.2 V, whichever is lower.
- While the Intel Agilex 7 device is powering up, powering down, or not turned on, the GPIO, SDM, and HPS pins can tolerate a maximum of 10 mA per pin and a total of 100 mA per I/O bank.
- After the Intel Agilex 7 device fully powers up, the voltage levels for the GPIO, SDM, and HPS pins must not exceed the DC input voltage (V_I) value.

Table 5. Guideline Examples for the Intel Agilex 7 F-Series and I-Series

Condition	Guideline
The VCCIO_SDM pin ramps up and at period *X*, the V_{CCIO_SDM} voltage is 0.9 V.	At period *X*, keep the signals driven by the device connected to the SDM I/O pin at a voltage of 0.9 V or lower.
The VCCIO_PIO pin ramps up and at period *X*, the V_{CCIO_PIO} voltage is 1.1 V.	At period *X*, keep the signals driven by the device connected to the GPIO I/O pin at a voltage of 1.1 V or lower.
The 1.5 V VCCIO_PIO pin ramps up and the voltage continues to rise pass the 1.2 V level.	Keep the GPIO I/O pin voltage at 1.2 V or lower until the Intel Agilex 7 device fully powers up.

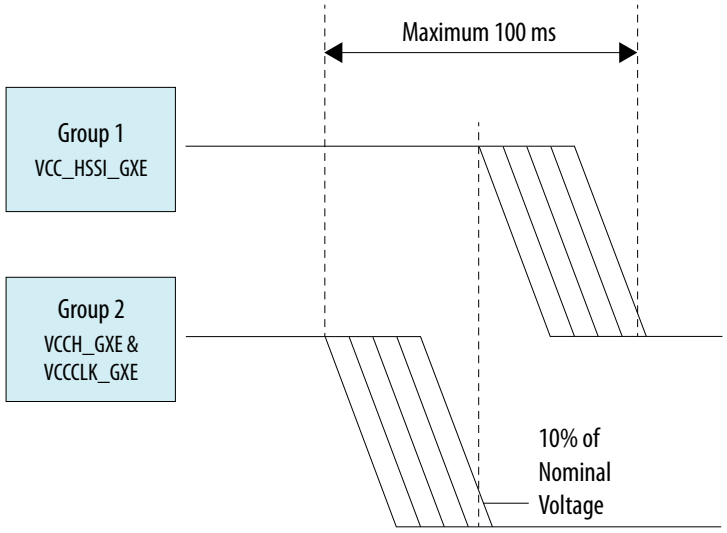
Table 6. Guideline Examples for the Intel Agilex 7 M-Series

Condition	Guideline
The VCCIO_SDM pin ramps up and at period *X*, the V_{CCIO_SDM} voltage is 1.8 V.	At period *X*, keep the signals driven by the device connected to the SDM I/O pin at a voltage of 1.8 V or lower.
The VCCIO_PIO pin ramps up and at period *X*, the V_{CCIO_PIO} voltage is 1.1 V.	At period *X*, keep the signals driven by the device connected to the GPIO I/O pin at a voltage of 1.1 V or lower.
The 1.3 V VCCIO_PIO pin ramps up and the voltage continues to rise pass the 1.2 V level.	Keep the GPIO I/O pin voltage at 1.2 V or lower until the F-Series and I-Series device fully powers up.

3.3. Power-Down Sequence Requirements for Intel Agilex 7 Devices with E-Tile

Intel Agilex 7 devices with E-tile must follow certain requirements during a power-down sequence. The power-down sequence can be a controlled power-down event via an on or off switch or an uncontrolled event such as a power supply collapse. In either situation, you must follow a specific power-down sequence.

Figure 4. Power-Down Sequence for Intel Agilex 7 Devices with E-Tile



- Power down all power rails fully within 100 ms.
- Before Group 1 (VCC_HSSI_GXE) supply power down, power down Group 2 (VCCH_GXE & VCCCLK_GXE) supplies within 10% of the nominal voltage.

For Intel Agilex 7 devices with E-tile, you can combine and ramp down other voltage rails that share the same voltage level and the same voltage regulator.

3.4. Floating Voltage

When you power up the device, you may observe a a floating voltage may be observed on the power rails as listed in the following table.

Table 7. Power Rails Floating Voltage for the Intel Agilex 7 F-Series and I-Series

Power Rail	Approximate Floating Voltage Value (V)
VCCPT	0.366
VCCIO_PIO	0.340
VCCA_PLL	0.095
VCCRCORE	0.500
VCCFUSEWR_SDM	0.229–1.360
VCCCLK_GXE[R1]	0.460
VCCRT_GXP[L1,L3]	0.547
VCCEHT_FHT_GXF[L,R]	0.091
VCCED_GXR[L,R]	0.035
VCCL_HPS	0.096

This is an expected behavior and causes neither functional nor reliability issue to the device, provided you follow the power-up or power-down sequence. The observed behavior can be avoided if the power supplies are not left to float before the device ramp up and after the device ramp down.

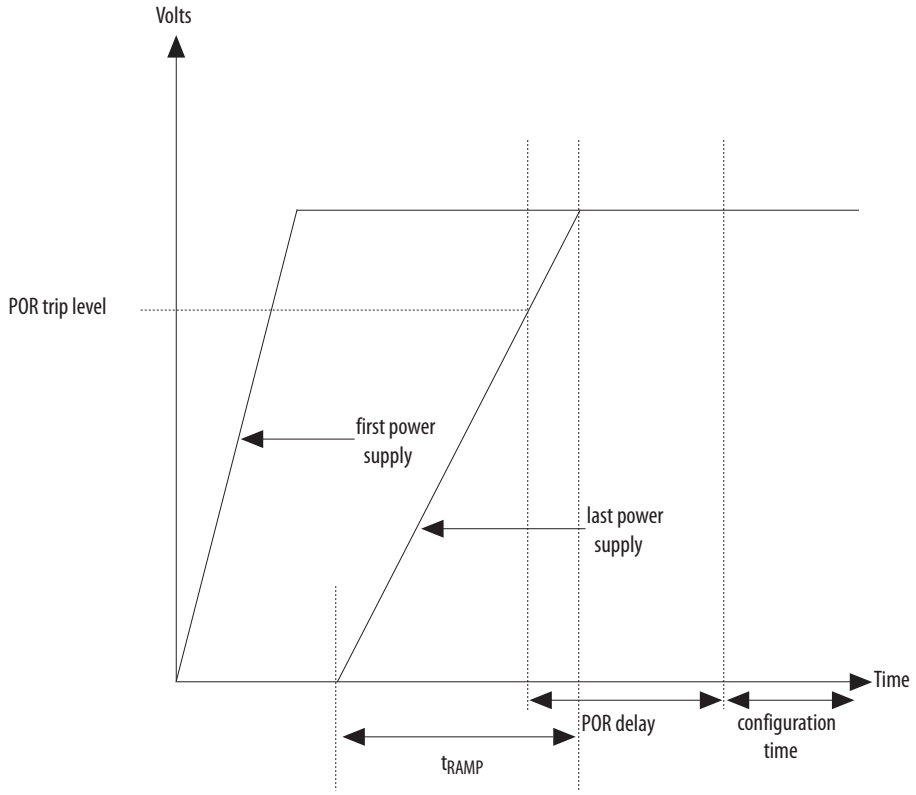
3.5. Power-On Reset

The power-on reset (POR) circuitry keeps the Intel Agilex 7 device in the reset state until the power supply outputs are within the recommended operating range.

A POR event occurs when you power up the Intel Agilex 7 device until all power supplies monitored by the POR circuitry reach the recommended operating range within the maximum power supply ramp time, t_{RAMP}. If t_{RAMP} is not met, the Intel Agilex 7 device I/O pins remain tri-stated, and programming registers remain reset, which may cause device configuration to fail.

Figure 5. Relationship Between t_{RAMP} and POR Delay

The boot ROM initialization sequence is part of the POR delay. For t_{RAMP} and POR delay specifications, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series* .



The Intel Agilex 7 POR circuitry uses individual detection circuitry to monitor each of the configuration-related power supplies independently. The POR circuitry is gated by the outputs of all the individual detectors.

POR delay is the time from when the POR trips out to the final reset signal. For POR trip level, you can use the minimum value of the last power supply as a reference.

The Intel Agilex 7 device is held in the POR state until all power supplies have passed their trigger point. After power supplies have passed the trigger point, the Secure Device Manager (SDM) waits for a configurable delay time and then starts device configuration.

Related Information

- Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series
  Provides more information about the t_{RAMP} and POR specifications for F-Series and I-Series FPGAs.
- Intel Agilex 7 FPGAs and SoCs Device Data Sheet: M-Series
  Provides more information about the t_{RAMP} and POR specifications for for M-Series FPGAs.

3.5.1. Power Supplies Monitored by the POR Circuitry

The following power supplies are monitored by the Intel Agilex 7 POR circuitry:

- V_{CCL_SDM}
- V_{CCPT}
- V_{CCIO_SDM}
- V_{CCADC}
- V_{CC}
- V_{CCH_SDM}
- V_{CCL_HPS}
- $V_{CCIO\_PIO\_SDM}$
- $V_{CCRCORE}$

The V_{CCL_SDM}, V_{CCPT}, and V_{CCIO_SDM} gate the SDM POR.

4. Intel Agilex 7 Sensor Monitoring System

Intel Agilex 7 devices provide you with on-chip voltage and temperature sensors. You can use these sensors to monitor external voltages and on-chip operation conditions such as the internal power rail and on-chip junction temperature.

The Intel Agilex 7 sensor monitoring system stores sampled data in the secure device manager (SDM). You can read the voltage and temperature values in the SDM by using the Mailbox Client Intel FPGA IP or the Mailbox Client with Avalon® Streaming Interface Intel FPGA IP.

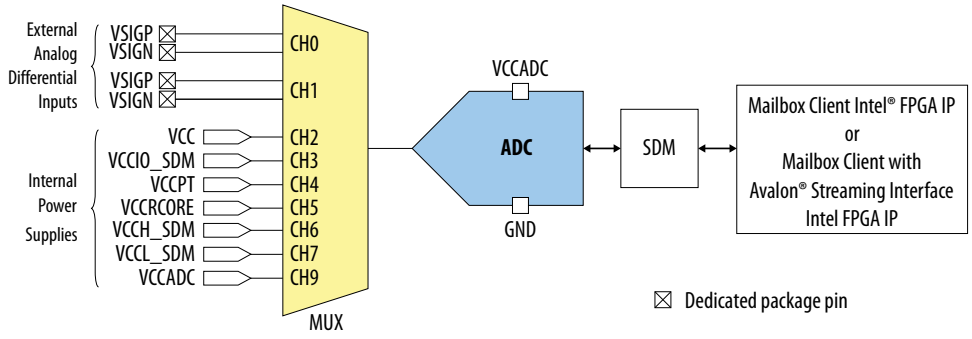
Related Information

- Operation Commands, Mailbox Client Intel FPGA IP User Guide
  Provides information about the GET_VOLTAGE and GET_TEMPERATURE commands of the Mailbox Client IP.
- Mailbox Client with Avalon Streaming Interface Intel FPGA IP User Guide
  Provides information about reading the voltage and temperature values using the Mailbox Client with Avalon Streaming Interface IP.

4.1. Voltage Monitoring System

The Intel Agilex 7 voltage monitoring system uses a built-in 7-bit analog to digital converter (ADC). The ADC can sample up to one kilo samples per second (KSPS).

Figure 6. Intel Agilex 7 Voltage Sensor



The voltage sensor has the following capabilities:

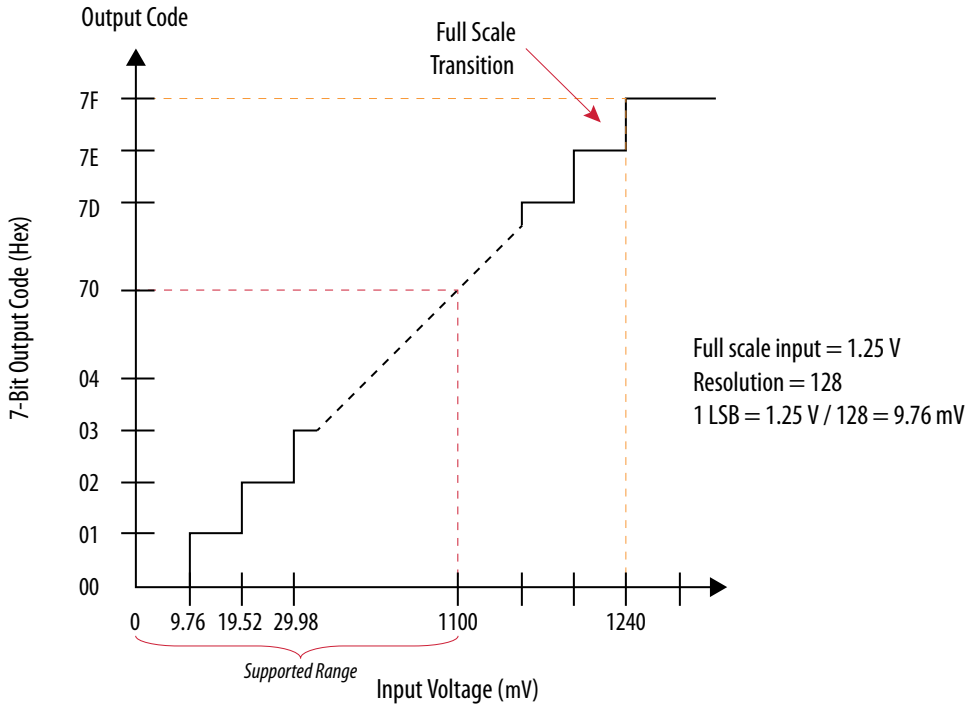
- Monitor external voltages up to 1.10 V through two pairs of differential input pins.
- Monitor internal power supplies. For internal high-voltage rails in channels 3, 4, 5, and 9, a voltage divider function divides the input voltage by half and feeds the voltage to the ADC. The SDM then doubles the ADC reading to get the actual voltage.

4.1.1. Voltage Sensor Transfer Function

The Intel Agilex 7 voltage sensor supports the ADC's unipolar operation mode.

Figure 7. Intel Agilex 7 ADC 7-Bit Unipolar Transfer Function

The analog input scale has full scale code from 00h to 7Fh. The measurement can only display up to *full scale – 1 LSB*



4.2. Temperature Monitoring System

The Intel Agilex 7 temperature monitoring system allows you to measure the on-chip temperature ($T_{JUNCTION}$) using local temperature sensors or remote temperature sensing diodes (TSDs).

Table 8. Overview of the Local and Remote Temperature Sensors

Feature	Local Temperature Sensor	Remote TSD
Temperature sensing	Uses the built-in ADC to sample the on-chip temperature.	Interfaces the TSD with an external temperature sensing chip.
Readout access	From the SDM mailbox through the Mailbox Client or Mailbox Client with Avalon Streaming Interface IPs.	From the external temperature sensing chip.
Operation capability	While the Intel Agilex 7 devices are in user mode.	While the Intel Agilex 7 devices are powered on or off.
User calibration	Not required.	Required. Refer to the related information.

Related Information

Guidelines: Calibrate Temperature Sensing Chip Interfacing the Intel Agilex 7 Remote TSD on page 29

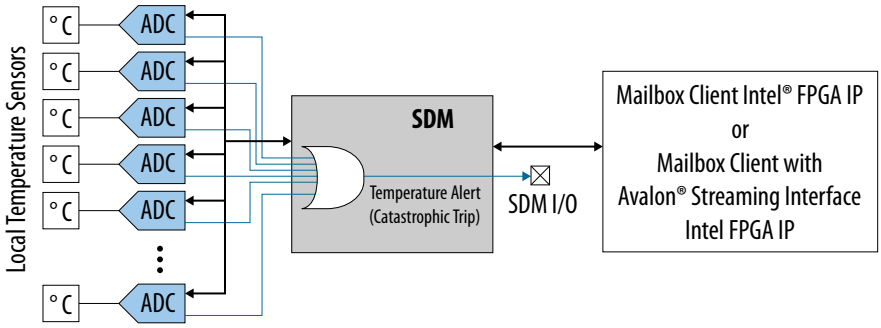
4.2.1. Local Temperature Sensor

The Intel Agilex 7 local temperature sensors use built-in 11-bit ADCs and provide temperature readouts through the SDM mailbox.

Each temperature sensor location contains up to two local TSDs in the core fabric, or up to six TSDs in transceiver tiles[3].

Figure 8. Intel Agilex 7 FPGAs Local Temperature Sensor

This figure is a block diagram of the local temperature sensors. For the physical locations of the sensors, refer to the related information.



Intel Agilex 7 devices provide up to 11 local temperature sensor locations for monitoring on-chip temperature.

- Up to five temperature sensor locations in the core fabric—with a total of up to nine local TSDs among them—allow you to monitor the temperatures around the core fabric.
- Up to six local temperature sensor locations, one in each transceiver tile, allow you to monitor the temperature of the transceiver tiles. The number of transceiver tiles varies among Intel Agilex 7 devices and package options.
- For M-Series FPGAs, up to two temperature sensor locations, one in each HBM2E tile, allow you to monitor the temperature of the HBM2E tiles. The number of HBM2E tiles varies among the M-Series FPGAs.

Refer to the related information for more details about the locations and availability of the temperature sensors in different Intel Agilex 7 series, densities, and packages.

(3) The number of local TSDs in each location for R-Tile, F-Tile, and E-Tile transceivers are six, five, and four, respectively. Other types of transceiver tiles have only one local TSD per location. For details about availability of the temperature sensors, refer to the related information.

Catastrophic Trip Signal

The catastrophic trip signal, nCATTRIP, is an optional signal that you can assign to any unused SDM_IO pin. If enabled, the nCATTRIP signal asserts and stays high. When the core temperature reaches 120° C and higher, the nCATTRIP signal drives low—you must immediately power down the FPGA to avoid permanent damage to the device. The nCATTRIP signal is only valid after the device enters user mode.

Note: The catastrophic signal is not supported for the local TSD in the SDM location.

Related Information

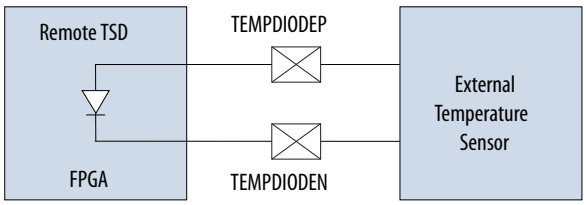
- Temperature Sensor Locations on page 21
- SDM Pin Mapping, Intel Agilex 7 Configuration User Guide
  Provides more details about enabling and assigning the nCATTRIP signal to an SDM_IO pin.

4.2.2. Remote Temperature Sensing Diode

The remote TSD interface allows you to monitor the temperature of the core fabric and transceiver tiles using an external temperature sensor.

Figure 9. External Temperature Sensor Connection to the Remote TSD

The remote TSD requires a two-pins connection.



- In the device pin-out files, the remote TSD pins are marked as TEMPDIODEP and TEMPDIODEN.
- For the remote TSD characteristics, refer to the relevant section in the device datasheet.

Related Information

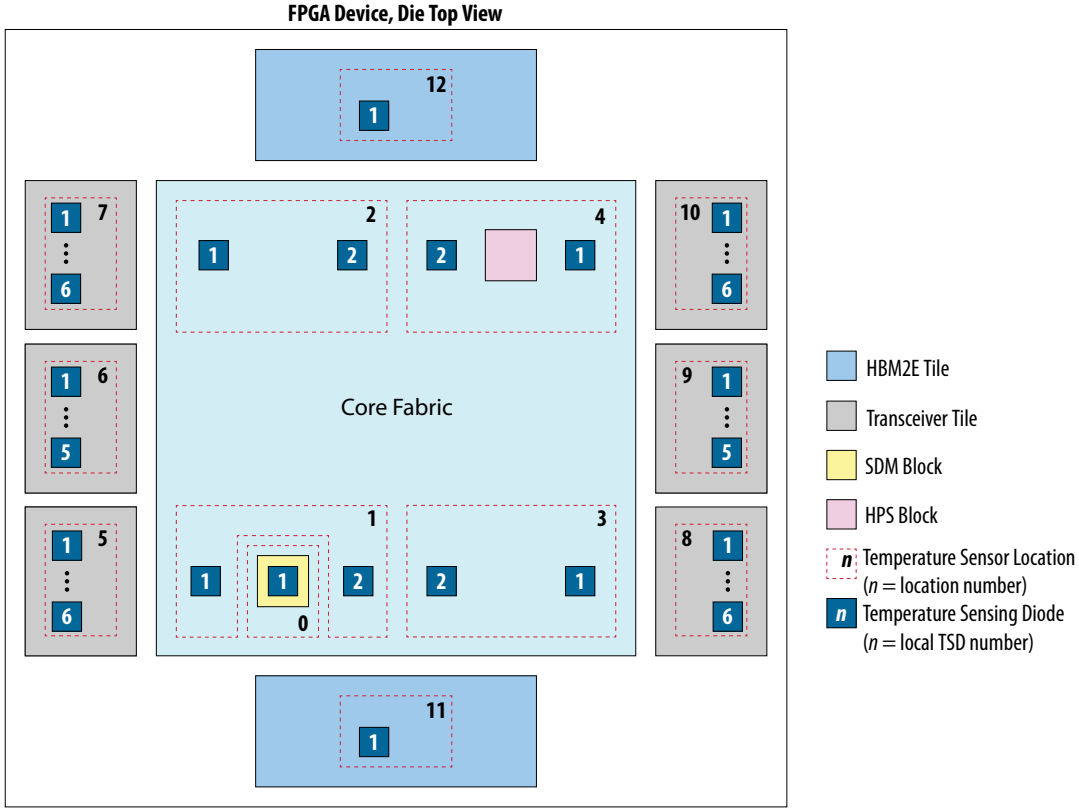
Temperature Sensor Locations on page 21

4.2.3. Temperature Sensor Locations

The Intel Agilex 7 local and remote TSDs are located in the core fabric and tiles. There are several local temperature sensor locations within the core fabric and one location in each transceiver or HBM2E tile.

Figure 10. Temperature Sensing Diode Locations

This figure shows approximate locations of the temperature sensors and is not to scale. The figure shows the view of the die as shown in the Intel Quartus Prime **Chip Planner**. In the **Pin Planner**, this corresponds to the "Bottom View".



Note: Availability of the transceiver tiles varies among different Intel Agilex 7 series, densities, and packages. The HPS block is only available in Intel Agilex 7 SoC FPGAs. The HBM2E tiles are only available in M-Series FPGAs.

- To monitor the HPS temperature, use TSD 1 in location 4.
- To monitor the SDM temperature, use the TSD in location 0.

Table 9. Temperature Sensor Locations Availability—Core Fabric

This table lists the availability of the temperature sensor locations and TSDs in the core fabric for different Intel Agilex 7 device densities. For more information about the device densities, refer to the Intel Agilex 7device overview.

Location	TSD	F-Series		I-Series		M-Series
		AGF 006 AGF 008 AGF 019 AGF 023	AGF 012 AGF 014 AGF 022 AGF 027	AGI 019 AGI 023	AGI 022 AGI 027 AGI 035 AGI 040 AGI 041	AGM 032 AGM 039
0	1	Yes	Yes	Yes	Yes	Yes
1	1	Yes	Yes	Yes	Yes	Yes

continued...

Location	TSD	F-Series		I-Series		M-Series
		AGF 006 AGF 008 AGF 019 AGF 023	AGF 012 AGF 014 AGF 022 AGF 027	AGI 019 AGI 023	AGI 022 AGI 027 AGI 035 AGI 040 AGI 041	AGM 032 AGM 039
	2	—	Yes	—	Yes	Yes
2	1	Yes	Yes	Yes	Yes	Yes
	2	—	Yes	—	Yes	Yes
3	1	Yes	Yes	Yes	Yes	Yes
	2	Yes	Yes	Yes	Yes	Yes
4	1	Yes	Yes	Yes	Yes	Yes
	2	Yes	Yes	Yes	Yes	Yes

Table 10. Temperature Sensor Locations Availability—Transceivers and HBM2E Tiles

This table lists the availability of the temperature sensor locations and TSDs in the transceiver and HBM2E tiles for different Intel Agilex 7 package codes. For more information about the package codes, refer to the Intel Agilex 7 device overview.

Loc.	TSD	F-Series					I-Series					M-Series
		R16A	R24B	R24C	R25A	R31C	R18A	R29A	R31A	R31B	R39A	R47A
5	1	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	2	Yes	—	Yes	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	3	Yes	—	Yes	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	4	Yes	—	Yes	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	5	Yes	—	Yes	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	6	—	—	—	—	—	—	—	Yes	—	—	—
6	1	—	—	—	—	—	—	—	—	—	Yes	—
	2	—	—	—	—	—	—	—	—	—	Yes	—
	3	—	—	—	—	—	—	—	—	—	Yes	—
	4	—	—	—	—	—	—	—	—	—	Yes	—
	5	—	—	—	—	—	—	—	—	—	Yes	—
7	1	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	2	—	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	3	—	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	4	—	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	5	—	—	—	—	Yes	Yes	Yes	Yes	Yes	Yes	Yes
	6	—	—	—	—	—	Yes	Yes	—	—	—	Yes
8	1	Yes	Yes	Yes	Yes	Yes	—	Yes	Yes	Yes	Yes	Yes
	2	Yes	Yes	Yes	Yes	Yes	—	Yes	Yes	Yes	Yes	Yes

continued...

Loc.	TSD	F-Series					I-Series					M-Series
		R16A	R24B	R24C	R25A	R31C	R18A	R29A	R31A	R31B	R39A	R47A
	3	Yes	Yes	Yes	Yes	Yes	—	Yes	Yes	Yes	Yes	Yes
	4	Yes	Yes	Yes	Yes	Yes	—	Yes	Yes	Yes	Yes	Yes
	5	Yes	—	Yes	—	Yes	—	Yes	Yes	Yes	Yes	Yes
	6	—	—	—	—	—	—	Yes	—	—	—	—
9	1	—	—	—	—	—	—	—	—	—	Yes	—
	2	—	—	—	—	—	—	—	—	—	Yes	—
	3	—	—	—	—	—	—	—	—	—	Yes	—
	4	—	—	—	—	—	—	—	—	—	Yes	—
	5	—	—	—	—	—	—	—	—	—	Yes	—
10	1	—	—	—	—	Yes	—	Yes	Yes	Yes	Yes	Yes
	2	—	—	—	—	Yes	—	Yes	Yes	Yes	Yes	Yes
	3	—	—	—	—	Yes	—	Yes	Yes	Yes	Yes	Yes
	4	—	—	—	—	Yes	—	Yes	Yes	Yes	Yes	Yes
	5	—	—	—	—	Yes	—	Yes	Yes	Yes	Yes	Yes
	6	—	—	—	—	—	—	Yes	—	—	—	—
11	1	—	—	—	—	—	—	—	—	—	—	Yes
12	1	—	—	—	—	—	—	—	—	—	—	Yes

Table 11. Local Temperature Sensor Locations and Corresponding Bank Names

The temperature sensor locations are as shown in the preceding figure. The bank name of each location varies between different types of transceiver tiles. For example, if location 7 is an E-tile, the bank name is 8C. If the same location is a P-tile, the bank name is 10C.

Location	Bank Name					
	Transceivers				HBM2E	
	F-Series	F-Series	F-Series I-Series M-Series	I-Series M-Series	M-Series	
	E-Tile	P-Tile	F-Tile	R-Tile	Top	Bottom
5	8A	10A	12A	14A	—	—
6	—	—	12B	—	—	—
7	8C	10C	12C	14C	—	—
8	9A	11A	13A	15A	—	—
9	—	—	13B	—	—	—
10	9C	11C	13C	15C	—	—
11	—	—	—	—	—	U50
12	—	—	—	—	U51	—

Table 12. Local Temperature Sensor Locations and Equivalent Remote TSD Pin Names

The temperature sensor locations are as shown in the preceding figure. Not all locations have a remote TSD. In locations with a remote TSD, the remote TSD is physically located next to the local TSDs that are marked as local TSD 1.

Loc.	Availability in Devices				Sensor Location [31..16] (Hex. code)	Supported Channel (4) (Specify sensor bitmask[15..0] as hex. value)	Equivalent Remote TSD Pin Name (Next to local TSD 1 in sensor location)
	AGF 006 AGF 008 AGF 012 AGF 014	AGF 019 AGF 022 AGF 023 AGF 027 AGI 019 AGI 022 AGI 023 AGI 027 AGI 041	AGI 035 AGI 040	AGM 032 AGM 039			
0	Yes	Yes	Yes	Yes	0000	0 (5)	TEMPDIODE0Ap / TEMPDIODE0An
1	Yes	Yes	Yes	Yes	0001	2, 1, 0 (6)	—
2	Yes	Yes	Yes	Yes	0002	2, 1, 0 (6)	TEMPDIODE0Cp / TEMPDIODE0Cn
3	Yes	Yes	Yes	Yes	0003	2, 1, 0 (6)	—
4	Yes	Yes	Yes	Yes	0004	2, 1, 0 (6)	—
5	Yes	Yes	Yes	Yes	0005	6, 5, 4, 3, 2, 1, 0 (7)	TEMPDIODE1p / TEMPDIODE1n
6	—	—	Yes	—	0006	5, 4, 3, 2, 1, 0	TEMPDIODE2p / TEMPDIODE2n
7	—	Yes	Yes	Yes	0007	6, 5, 4, 3, 2, 1, 0 (7)	TEMPDIODE3p / TEMPDIODE3n
8	Yes	Yes	Yes	Yes	0008	6, 5, 4, 3, 2, 1, 0 (7)	TEMPDIODE4p / TEMPDIODE4n
9	—	—	Yes	—	0009	5, 4, 3, 2, 1, 0	TEMPDIODE5p / TEMPDIODE5n
10	—	Yes	Yes	Yes	000A	6, 5, 4, 3, 2, 1, 0 (7)	TEMPDIODE6p / TEMPDIODE6n
11	—	—	—	Yes	000B	1, 0	—
12	—	—	—	Yes	000C	1, 0	—

(4) For sensor locations with several local TSDs, channel 0 (mask [0]) returns the highest temperature among the local TSDs in the particular location. For sensor locations with one local TSD, channel 0 returns the same value as channel 1.

(5) For location 0, only channel 0 (mask [0]) is supported, returning the temperature reading for the TSD in that location.

(6) Channel 2 (mask [2]) is available only in selected production devices.

(7) Channels 2 to 6 (masks [6..2]) are applicable only to R-tile ([6..2]), F-tile ([5..2]), and E-tile ([4..2]) transceiver tiles. Availability of the transceiver tiles varies among different Intel Agilex 7 series, densities, and packages.

Related Information

- Operation Commands, Mailbox Client Intel FPGA IP User Guide
  Provides information about the GET_VOLTAGE and GET_TEMPERATURE commands of the Mailbox Client IP.
- Mailbox Client with Avalon Streaming Interface Intel FPGA IP User Guide
  Provides information about reading the voltage and temperature values using the Mailbox Client with Avalon Streaming Interface IP.
- Intel Agilex 7 FPGAs and SoCs Device Overview
  Provides more information about Intel Agilex 7 FPGA densities and available package codes.

4.2.4. Retrieving Local Temperature Sensor Reading

To retrieve the temperature readings, provide the location code and sensor masks to the Mailbox Client with Avalon Streaming Interface Intel FPGA IP. The Mailbox Client with Avalon Streaming Interface IP accepts a 32-bit value in fixed length hexadecimal format.

Bits [27..16] carry the local TSD location code while bits [15..0] represent the temperature channels in the location. Bits [31..28] are reserved.

Figure 11. Bit Format to Mailbox Client with Avalon Streaming Interface IP to Specify Local TSDs to Read

To specify which local TSD to read, provide the Mailbox Client with Avalon Streaming Interface IP with the 32-bit value in fixed length hexadecimal codes.

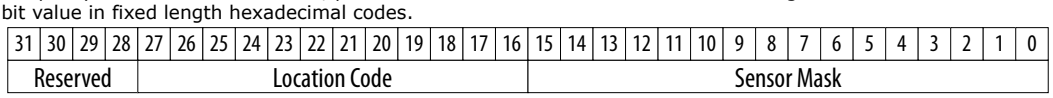


Table 13. Sensor Mask Function for Each Local TSD Location

For locations that have only a single local TSD, the sensor mask defaults to 0. You can specify only the location code.

Function	Series	Location		Applicable Sensor Masks
		Type	Max TSD Count	
Specify the local TSDs to read	F-Series	E-Tile	4	[4..1]
	F-Series	P-Tile	1	[0]
	F-Series I-Series M-Series	F-Tile	5	[5..1]
	I-Series M-Series	R-Tile	6	[6..1]
	M-Series	HBM2E tile	1	[1]
	F-Series I-Series M-Series	Core fabric	2	[2..1]
			1	[0]
Read the TSD with the highest temperature in the location	F-Series I-Series M-Series	All locations except location 0	Varies	[0]

Table 14. Examples for Reading Temperature through the SDM Mailbox

This table provides examples for reading the temperature from the different tiles and TSDs. Availability of the transceiver tiles varies among different Intel Agilex 7 series, densities, and packages.

Location		Channels to Read in the Location	Hexadecimal Code to Send	Values Returned
Type	Number			
E-Tile	5	Temperature from all local TSDs in location 5 and the highest temperature in the location.	0x0005001F	Returns five values—temperature for local TSDs 1, 2, 3, and 4 in the location, and the highest temperature among them.
		Temperature from TSD with the highest temperature in location 5.	0x00050001	Returns one value—the value of the TSD with the highest temperature in the location.
P-Tile	8	Temperature of the local TSD in location 8.	0x00080002	Because P-Tile transceivers only have a single local TSD in the location, both hexadecimal code returns the same value.
		Temperature of TSD with the highest temperature in location 8.	0x00080001	
R-Tile	5	Temperature from all local TSDs in location 5 and the highest temperature in the location.	0x0005007F	Returns seven values—temperature for local TSDs 1, 2, 3, 4, 5, and 6 in the location, and the highest temperature among them.
		Temperature from TSD with the highest temperature in location 5.	0x00050001	Returns one value—the value of the TSD with the highest temperature in the location.
Core fabric	1 (8)	Temperature from all local TSDs in location 1.	0x00010006	Returns two values—temperature for local TSDs 1 and 2.
		Temperature from all local TSDs in location 1 and the highest temperature in the location.	0x00010007	Returns three values—temperature for local TSDs 1 and 2 in the location, and the highest temperature among them.

Note: Intel recommends that you read all local TSDs in an E-Tile location and use the highest temperature readout as the critical point for the transceiver tile. Alternatively, you can query sensor mask [0] for the highest temperature in the E-Tile location.

Related Information

- Operation Commands, Mailbox Client Intel FPGA IP User Guide
  Provides information about the GET_VOLTAGE and GET_TEMPERATURE commands of the Mailbox Client IP.
- Mailbox Client with Avalon Streaming Interface Intel FPGA IP User Guide
  Provides information about reading the voltage and temperature values using the Mailbox Client with Avalon Streaming Interface IP.

4.2.5. Temperature Sensor Error Codes

Table 15. Temperature Sensor Error Codes and Solutions

Error Code	Invalid Condition	Solution
0x80000000	Selected temperature sensor channel is currently inactive.	Ensure that the tile where the TSD is located is actively in use.
0x80000001	Selected temperature sensor channel returned a value that is not the latest reading.	Retrieve the temperature reading again

continued...

(8) Example is applicable to devices with two local TSDs in location 1

Error Code	Invalid Condition	Solution
0x80000002	Selected temperature sensor channel is invalid for the device.	Ignore the returned data because the temperature sensor channel location is invalid
0x80000003	System is corrupted or failed to respond	Contact Intel FPGA support
0x80000004		
0x80000005	Communication mechanism is busy	Retrieve the temperature reading again
0x800000FF	System is corrupted or failed to respond	Contact Intel FPGA support

4.3. Sensors Design Considerations

To ensure the success of your designs, follow the recommended design guidelines. These guidelines apply to all variants of the device family unless noted otherwise.

4.3.1. Voltage Monitor Design Guidelines

- Connect the power pins and VSIG pins according to the requirements in the device pin connection guidelines.
- If you use the voltage sensor in single-ended mode, tie the VSIGN pin to the GND pin.
- To prevent damage, do not drive VSIGP and VSIGN pins until the VCCADC power rail has reached 1.62 V.

Related Information

Intel Agilex 7 Device Family Pin Connection Guidelines: F-Series and I-Series
Provides more information about the connection guidelines and the supported power supplies for F-Series and I-Series FPGAs.

4.3.2. Temperature Monitor Design Guidelines

You can measure the on-chip temperature of the core fabric or transceiver tiles through the remote TSDs while the device is powered on or powered off. However, the local temperature sensors are available only after the device is powered up and configured.

- Connect the remote TSD pins to external temperature sensing devices to monitor the on-chip temperature.
- To interface with the remote TSD, use temperature sensing chips with features that allow you to perform calibration and measurement compensation to improve accuracy, such as:
  - Configurable ideality factor
  - Offset adjustment with or without Beta compensation
- Keep the resistance of both board traces to the remote TSD p and n pins to less than 0.2 Ω.
- Route both traces in equal lengths and shield them.
- Intel recommends a 10-mils width and space for both traces.
- Route both traces through the most minimum number of vias and crossunders possible to minimize the thermocouple effects.

- Ensure that the number of vias for both traces are the same.
- To avoid coupling, insert a GND plane between the remote TSD pins traces and high-frequency toggling signals, such as clocks and I/O signals.
- To filter high-frequency noise, place an external capacitor between the traces close to the external sensors.
- If you use only the local temperature sensors, you can leave the remote TSD p and n pins unconnected.

For details about device specifications and connection guidelines, refer to the external temperature sensor manufacturer's documentation.

4.3.3. Transceiver Tile Local Temperature Sensor Design Guidelines

The R-Tile, E-Tile, and F-Tile transceiver tiles[9] have multiple built-in local TSDs, spread across each transceiver die. When you query the sensors, the readings from the TSDs may vary slightly from each other because of the different activities run in each TSD location of the transceiver tile.

- For temperature reading through the SDM mailbox, you can query all local TSDs.
- Intel recommends that you read all local TSDs in a transceiver tile temperature sensor location and use the highest temperature readout as the critical point for the tile.

4.3.4. Guidelines: Calibrate Temperature Sensing Chip Interfacing the Intel Agilex 7 Remote TSD

If you interface an external temperature sensing chip to the Intel Agilex 7 remote TSD, you must calibrate the external chip to avoid temperature measurement inaccuracy.

The calibration of the external temperature sensing chip identifies optimized settings such as the temperature offset and change in ideality factor. The external chip uses these settings to accurately sample the temperature from the Intel Agilex 7 remote TSD.

Related Information

AN 769: Intel FPGA Remote Temperature Sensing Diode Implementation Guide
Provides guidelines for selecting external temperature sensing chips to use with Intel Agilex 7 FPGAs.

4.3.5. Guidelines: Reading the R-Tile Local Temperature Sensor

Adhere to these guidelines if you use the debug toolkit or the heterogeneous interface for portability (HIP) reconfiguration interface.

Before reading the R-Tile local temperature sensor value from the SDM mailbox:

- Close the debug toolkit.
- Wait for completion of the HIP reconfiguration transactions.

(9) Availability of the transceiver tiles varies among different Intel Agilex 7 series, densities, and packages.

4.4. Temperature Reading Design Example

You can use the Temperature Reading design example to understand better how to set up and use the Intel Agilex 7 temperature sensors with the Mailbox Client with Avalon Streaming Interface Intel FPGA IP.

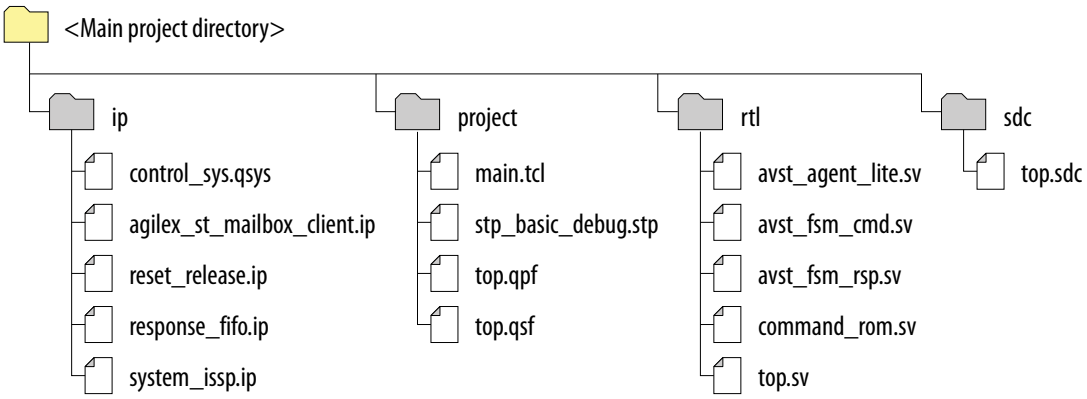
Related Information

- Mailbox Client with Avalon Streaming Interface Intel FPGA IP User Guide
  Provides information about reading the voltage and temperature values using the Mailbox Client with Avalon Streaming Interface IP.
- Temperature Reading Design Example File
  Downloads the `Intel-Agilex-TemperatureReadingDesignExample.qar` design example archive.
- Temperature Reading Design Example Description on page 31

4.4.1. Directory Structure

After unarchiving the Temperature Reading design example, it consists of a main directory with several subdirectories and files.

Figure 12. Temperature Reading Design Example Directory Structure



Related Information

Temperature Reading Design Example File
Downloads the `Intel-Agilex-TemperatureReadingDesignExample.qar` design example archive.

4.4.2. Hardware and Software Requirements

Intel uses the following hardware and software to test the Temperature Reading design example.

- Temperature Reading design example Intel Quartus Prime archive
- Intel Quartus Prime Pro Edition software, version 20.4
- Intel Quartus Prime In-System Sources and Probes Editor

- Intel Quartus Prime Signal Tap Logic Analyzer
- Intel Quartus Prime System Console
- Intel Agilex 7 FPGA F-Series Development Kit

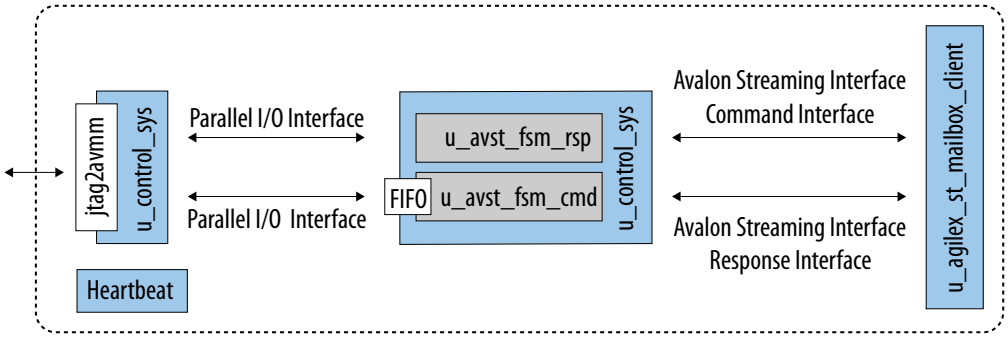
Related Information

- Temperature Reading Design Example File
  Downloads the `Intel-Agilex-TemperatureReadingDesignExample.qar` design example archive.
- Intel Agilex 7 FPGA Development Kits
  Provides more information and allow you to order the Intel Agilex 7 FPGA F-Series development kits.

4.4.3. Temperature Reading Design Example Description

The Temperature Reading design example exposes a JTAG-to-Avalon streaming interface that allows you to interact with the design example modules through the Intel Quartus Prime System Console.

Figure 13. Temperature Reading Design Example Block Diagram



All the Intel Quartus Prime System Console read and write commands control a set of parallel I/O IPs that select a command for the Mailbox Client with Avalon Streaming Interface IP to execute. At the same time, the parallel I/O IPs control a FIFO IP that stores all the Mailbox Client with Avalon Streaming Interface IP responses.

Table 16. Description of Modules in the Design Example

Module	Description
`u_avst_fsm_cmd`	This module connects to a four-bit wide bus that selects a command for a finite state machine to send to the Mailbox Client with Avalon Streaming Interface IP. The available commands are hardcoded in a look-up table (LUT) modeled in the `command_rom.sv` file. You can modify the LUT to edit existing commands or include new commands.

continued...

Module	Description
	Command LUT ROM bit order: • [37..34]—the command ROM address that contains the next argument of the command. All final arguments for a command points to address 0x0. • [33]—the finite state machine uses this bit to identify and assert the "start of packet" protocol signal. • [32]—the finite state machine uses this bit to identify and assert the "end of packet" protocol signal. • [31..0]—The command header or argument that the design example sends to the Mailbox Client with Avalon Streaming Interface IP.
u_avst_fsm_rsp	This module receives the response from the Mailbox Client with Avalon Streaming Interface IP. The module handles the Avalon streaming interface protocol and stores the header and arguments from the response in a FIFO. The design example exposes the read interface of the FIFO the **u_control_sys** module so you can access through the Intel Quartus Prime System Console.

- You can access the master reset signal for the system through an In-System Sources and Probes instance. By default, the system is in the reset state.
- The same In-System Sources and Probes instance connects to a heartbeat counter. Therefore, you must verify that the system has a free running clock.
- A 100 MHz clock constrains all the design example logic.
- The protocol finite state machine of the design example can handle only a single command at a time. Before sending the next command, wait until the system has stored the response from the previous command in the response FIFO.

4.4.4. Using the Temperature Reading Design Example

To use the Temperature Reading design example, you generate and program the design example to the development kit. Then, you can start the design and send commands. You can verify the design using Signal Tap.

4.4.4.1. Opening the Temperature Reading Design Example

1. Download the design example project archive (`Intel-Agilex-TemperatureReadingDesignExample.qar`).
2. In the Intel Quartus Prime Pro Edition software, click **File ➤ Open Project** and select the `Intel-Agilex-TemperatureReadingDesignExample.qar` project archive.
3. In the **Restore Archived Project** window, specify the **Destination folder**.
4. Click **OK**.

The Intel Quartus Prime software extracts the files from the archive and opens the `top.qpf` project.

After the project opens, you can compile the design example and generate the `.sof` file.

Related Information

- Temperature Reading Design Example File
  Downloads the `Intel-Agilex-TemperatureReadingDesignExample.qar` design example archive.

- Compiling the Temperature Reading Design Example and Generating the Software Object File on page 33
- Directory Structure on page 30

4.4.4.2. Compiling the Temperature Reading Design Example and Generating the Software Object File

Before you begin, use Intel Quartus Prime software to extract and open the Temperature Reading design example.

1. With the Temperature Reading design example open, from the Intel Quartus Prime menu, select **Processing ➤ Start Compilation** to compile the design example.
2. Wait for the compilation to complete successfully,
3. Navigate to the `<Main project directory>\project\output_files` directory to find the generated software object file (`.sof`).

After generating the `.sof` file, you can program the design example into the development kit and run the design.

Related Information

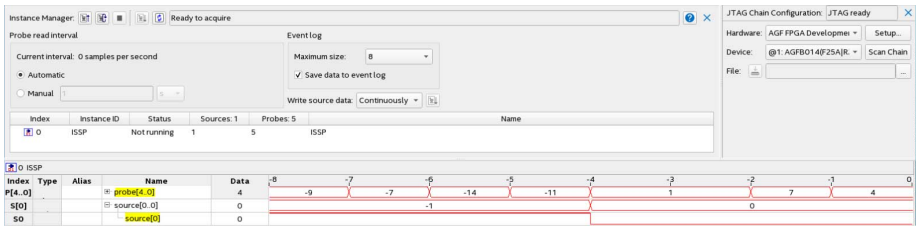
- Opening the Temperature Reading Design Example on page 32
- Programming and Starting Up the Temperature Reading Design Example on page 33
- Directory Structure on page 30

4.4.4.3. Programming and Starting Up the Temperature Reading Design Example

Before you begin, generate the Temperature Reading design example `.sof` file.

1. From the Intel Quartus Prime menu, select **Tools ➤ Programmer**
2. In the **Programmer** window, click **Add File**.
3. Select the generated `<filename>.sof` file and click **Open**
4. In the **Program/Configure** column of the `<filename>.sof` row, turn on the check box.
5. Click **Start** to load the `<filename>.sof` to the Intel Agilex 7 FPGA F-Series Development Kit and wait until the progress is 100%.
6. From the Intel Quartus Prime menu, select **Tools ➤ In-System Sources and Probes Editor**.

Figure 14. Temperature Reading Design Example in the In-System Sources and Probes Editor



7. In the **In-System Sources and Probes Editor** window, verify that the **probe[4..0]** signal is toggling.
8. Set the **source[0]** signal that controls the system reset to Low. The system exits the reset state.

After you set the design example to run, you can start sending command using the Intel Quartus Prime System Console.

Related Information

- Compiling the Temperature Reading Design Example and Generating the Software Object File on page 33
- Sending Commands to the Temperature Reading Design Example on page 34

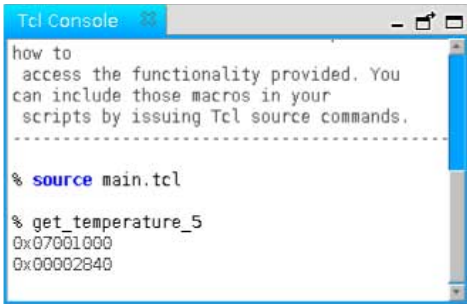
4.4.4.4. Sending Commands to the Temperature Reading Design Example

Before you begin, program the `.sof` of the Temperature Reading design example into the Intel Agilex 7 FPGA F-Series Development Kit.

1. From the Intel Quartus Prime menu, select **Tools ➤ System Debugging Tools ➤ System Console**.
2. In the **System Console** window, click inside the **TCL Console** tab.
3. Enter the following command: `source main.tcl`
   The console loads the `main.tcl` script.
4. Enter a supported command in the System Console, for example, `get_temperature_5`.

   Refer to the related information for the commands supported by the `main.tcl` script.

Figure 15. Running a Command Routine in the System Console



The System Console displays the results after the command. The first element of the results represents the header of the Mailbox Client with Avalon Streaming Interface IP response.

The header shows the executed command routine number, the number of expected argument for the command, and an error code if there is an error with the request. In the example, `get_temperature_5` is routine number seven (`07`), it expects one (`01`) argument, and there is no error.

Note: The System Console does not allow you to run another command routine until it has received a response from the Mailbox Client with Avalon Streaming Interface IP.

Related Information

- Programming and Starting Up the Temperature Reading Design Example on page 33
- Default Commands for the Temperature Reading Design Example on page 35

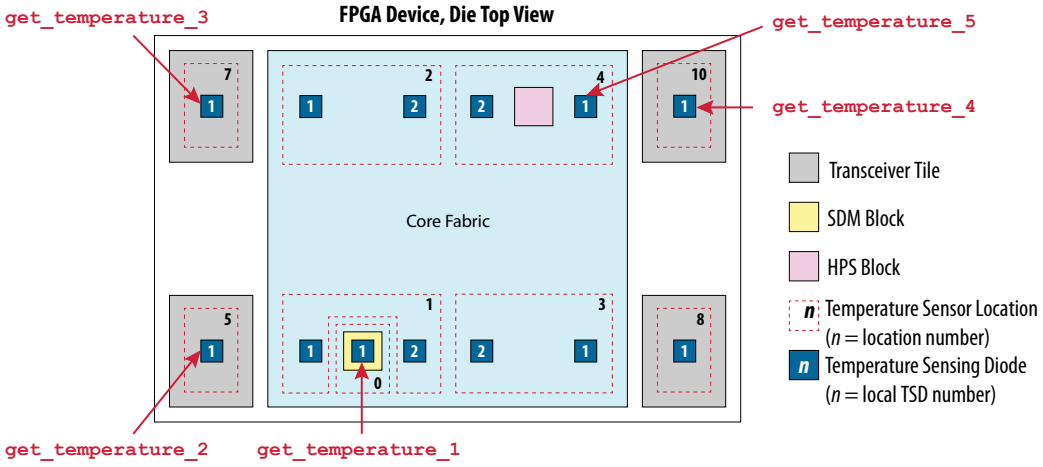
4.4.4.4.1. Default Commands for the Temperature Reading Design Example

The Temperature Reading design example contains a `main.tcl` script that provides a set of commands you can run.

Table 17. Command Routines in the `main.tcl` Script

Command Routine	Description
`send_noop`	Sends the `NOOP` command of the Mailbox Client with Avalon Streaming Interface IP.
`get_voltage`	Sends the `GET_VOLTAGE` command of the Mailbox Client with Avalon Streaming Interface IP.
`get_temperature_1`	Reads local TSD 1 in core fabric sensor location 0.
`get_temperature_2`	Reads local TSD 1 in transceiver tile sensor location 5.
`get_temperature_3`	Reads local TSD 1 in core fabric location 2.
`get_temperature_4`	Reads local TSD 1 in transceiver tile location 10.
`get_temperature_5`	Reads local TSD 1 in core fabric sensor location 4.
`get_idcode`	Sends the `GET_IDCODE` command of the Mailbox Client with Avalon Streaming Interface IP.
`get_chipid`	Sends the `GET_CHIPID` command of the Mailbox Client with Avalon Streaming Interface IP.

Figure 16. Locations of TSDs Read by the `get_temperature_n` Commands



Related Information

- Sending Commands to the Temperature Reading Design Example on page 34
- Temperature Sensor Locations on page 21
  Provides more information about the physical locations of the temperature sensors and how to address them.

4.4.5. Verifying the Interaction between the Design Example and the Mailbox Client with Avalon Streaming Interface IP

To verify the interaction between the state machines of the design example with the Mailbox Client with Avalon Streaming Interface IP, use the `stp_basic_debug.stp` Signal Tap file provided with the design example.

The provided Signal Tap file keeps track of the following signals:

- The parallel I/O IPs connected to the state machines
- The command and response interfaces from the Mailbox Client with Avalon Streaming Interface IP
- The internal state of the state machines
- The response FIFO

Figure 17. Capturing an Outgoing Command

To capture an outgoing command to the Mailbox Client with Avalon Streaming Interface IP, set a rising edge trigger condition on the `usr_start_edge` signal of the **User Interface** group.

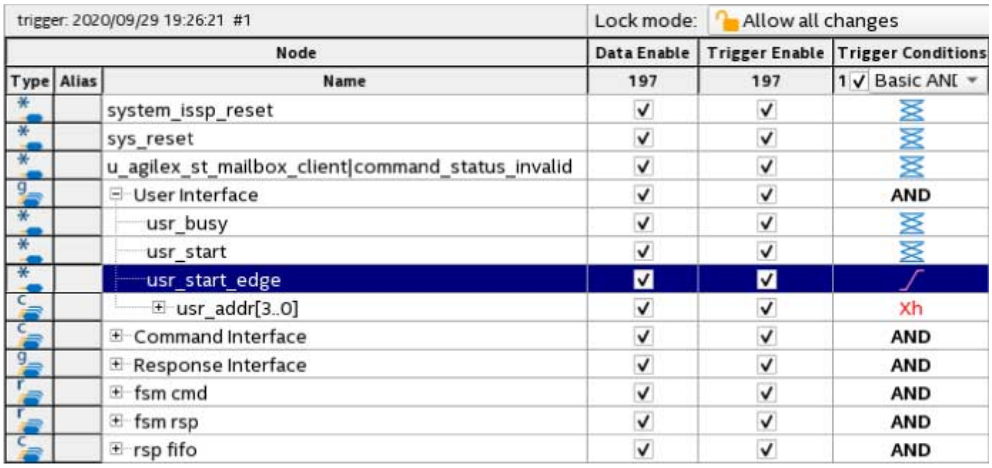


Figure 18. Capturing an Incoming Response

To capture a command incoming to the Mailbox Client with Avalon Streaming Interface IP, set an edge trigger condition on the `response_valid` signal of the **Response Interface** group.

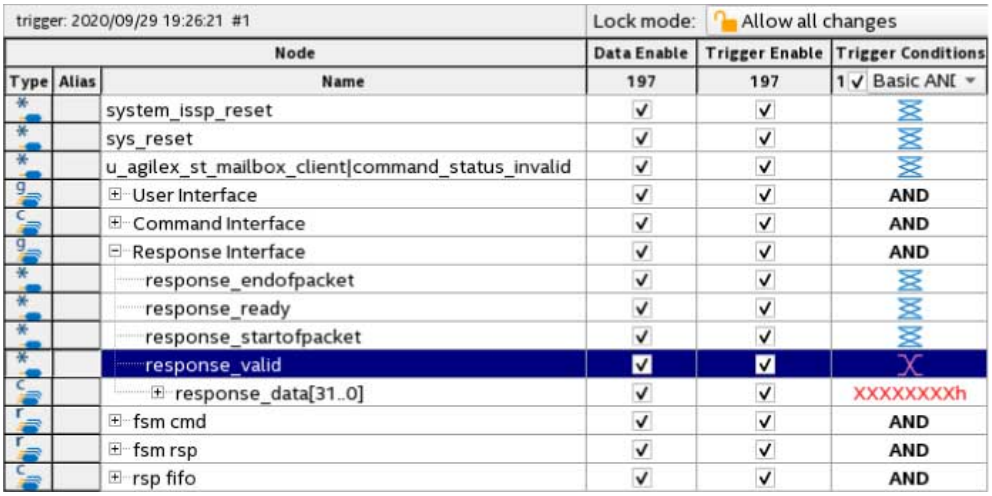


Figure 19. Signal Tap Capture of Outgoing GET_TEMPERATURE Command to the Mailbox Client with Avalon Streaming Interface IP

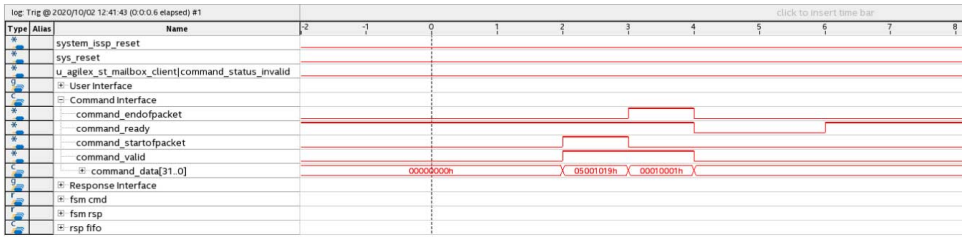
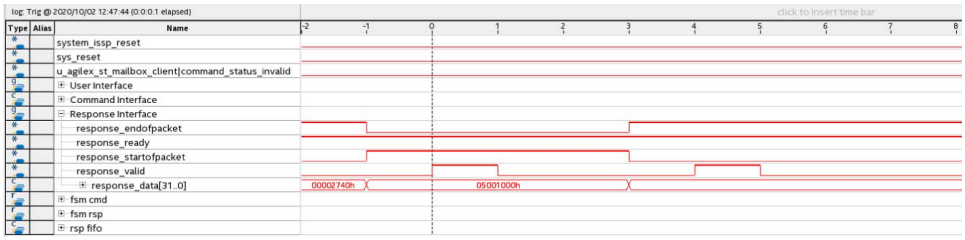


Figure 20. Signal Tap Capture of Response for GET_TEMPERATURE Command from the Mailbox Client with Avalon Streaming Interface IP



Note: The Mailbox Client with Avalon Streaming Interface IP can hold the Start of Packet and End of Packet signals in a high state even if there is no traffic between the IP and the finite state machine.

5. Intel Agilex 7 Power Optimization Techniques and Features

Intel Agilex 7 devices leverage on advanced 10-nm process technology, an enhanced core architecture, and various optimizations to reduce total power consumption. The power optimization techniques and features are listed below:

- SmartVID Standard Power Devices
  - Temperature Compensation
- Digital signal processing (DSP) and M20K Power Gating
- Clock Gating
- Power Sense Line

5.1. SmartVID Standard Power Devices

The SmartVID feature compensates for process variation by narrowing the process distribution using voltage adaptation.

This feature is supported in all Intel Agilex 7 devices with the –V, –E, and –X power options only. For the –V, –E, and –X power option devices, you must connect the PWRMGT_SCL and PWRMGT_SDA pins in both the Power Management BUS (PMBus) master and PMBus slave modes. The PWRMGT_ALERT pin is required for the Intel Agilex 7 device in the PMBus slave mode. The PWRMGT_ALERT pin is an active low pin and is used to perform the handshake flow between the FPGA device and an external PMBus master. All connections must be set up on the circuit board and in the Intel Quartus Prime software.

Table 18. The PMBus Master and Slave Modes Interfaces for the Intel Agilex 7 Devices

PMBus Interfaces	Operating Modes	
	PMBus Master Mode	PMBus Slave Mode
PWRMGT_SCL	Required	Required
PWRMGT_SDA	Required	Required
PWRMGT_ALERT	—	Required

The PMBus master and PMBus slave modes only support the 1.8-V single-ended I/O standard.

Note: The PWRMGT_SDA, PWRMGT_SCL, and PWRMGT_ALERT signals are in the undetermined state during device power-up and power-down. The PWRMGT_SDA, PWRMGT_SCL, and PWRMGT_ALERT signals are only valid after the device is fully powered up.

For more information about how to connect these pins on the circuit board, refer to the *Intel Agilex 7 Device Family Pin Connection Guidelines: F-Series and I-Series*.

For instructions on how to set up the connections in the Intel Quartus Prime software, refer to the Specifying Power Management and VID Parameters and Options on page 51.

Note: Intel Agilex 7 standard power devices (–1V, –2V, –3V, –3E, and –4X power grades) are SmartVID devices. The core voltage supplies (V_{CC} and V_{CCP}) for each SmartVID device is mandatory to be driven by a PMBus-compliant voltage regulator dedicated to the –V, –E, and –X power option devices that is connected to that Intel Agilex 7 devices via PMBus. Intel Agilex 7 devices do not configure or function correctly if the core voltage is driven by a non-PMBus compliant regulator with a fixed output voltage.

Intel programs the optimum voltage level required by each individual FPGA device into a fuse block during device manufacturing. The Secure Device Manager (SDM) Power Manager reads these values and can communicate them to an external power regulator or a system power controller through the PMBus interface.

The SmartVID feature allows a power regulator to provide the Intel Agilex 7 devices with V_{CC} and V_{CCP} voltage levels that maintain the performance of the specific device speed grade. When the SmartVID feature is used:

1. Intel Agilex 7 devices are powered up at 0.80V regardless of speed grade for both V_{CC} and V_{CCP}.
2. After the VID-fused value in the FPGA is determined and propagated to the external voltage regulator, both the V_{CC} and V_{CCP} voltages are regulated based on the boosted VID-fused value.

Related Information

- Intel Agilex 7 Device Family Pin Connection Guidelines: F-Series and I-Series
  Provides more information about the connection guidelines of each pin for F-Series and I-Series FPGAs.
- Specifying Power Management and VID Parameters and Options on page 51
  Provides instructions on how to set up the connection in the Intel Quartus Prime software.
- AN 974: Intel Stratix® 10 and Intel Agilex SmartVID Debug Checklist and Voltage Regulator Guidelines

5.1.1. SmartVID Feature Implementation in Intel Agilex 7 Devices

Devices supporting the SmartVID feature have a VID-fused value programmed into a fuse block during device manufacturing. The VID-fused value represents a voltage level in the range of 0.7 V to 0.9 V. Each device has its own specific VID-fused value.

The boosted VID-fused value is sent to the external regulator or system power controller through the PMBus interface. Upon receiving the boosted VID-fused value, an adjustable regulator tunes the V_{CC} and V_{CCP} voltage levels to the voltage specified by the VID-fused value.

Intel Agilex 7 devices perform the SmartVID setup in the early stage of the configuration process. The SmartVID process continues to monitor the V_{CC} and V_{CCP} voltage rails in user mode. The Power Manager monitors the temperature and adjusts the voltage when required. For more information, refer to the *Temperature Compensation* section.

Table 19. SmartVID Regulator Requirements

Specification[10]	Value
Voltage range	0.6 V – 1.0 V
Voltage step	5 – 10 mV
Ramp time	• Non-CvP—10 mV/10 ms to 10 mV/20 µs • Configuration via Protocol (CvP)—10 mV/60 µs to 10 mV/20 µs [11]

Table 20. Supported Voltage Output Format for Intel Agilex 7 Devices with the –V, –E, and –X Power Options

Voltage Output Format	Operating Modes	
	PMBus Master Mode	PMBus Slave Mode
Linear mode	Yes	No
VID mode	No	No
Direct mode	Yes	Yes, with coefficient m=1, b=0, and R=0. Translated output voltage is in millivolts (mV).

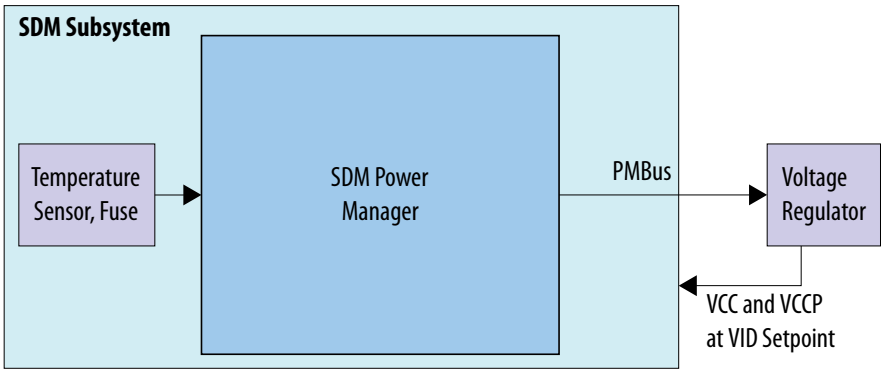
Related Information

Temperature Compensation on page 51

5.1.2. SDM Power Manager

In Intel Agilex 7 devices, the SmartVID feature is managed by the SDM subsystem. The SDM subsystem is powered up after V_{CC} and V_{CCP} voltage levels are powered up to 0.8V. The SDM Power Manager reads the VID-fused value and communicates this value to the external voltage regulator through the PMBus interface.

Figure 21. SDM Power Manager Block Diagram



(10) To ensure the specifications are meeting requirements, refer to your selected voltage regulator data sheet.

(11) When the system is required to support the CvP functionality and meet the PCI Express* (PCIe*) link-up timing budget during the initial power up, the minimum ramp time is 10 mV/60 µs.

The SDM Power Manager has the following stages:

- Initial stage
  - Set the external voltage regulator to supply power to V_{CC} and V_{CCP} to the voltage level based on the boosted VID-fused value and the device temperature.
  - Configures the FPGA and switches the FPGA to user mode.
- Monitor stage
  - Monitors temperature and updates V_{CC} and V_{CCP}.

5.1.2.1. PMBus Master Mode

In the PMBus master mode:

- During the initial stage—the voltage is set to the maximum value, regardless of the temperature. This is a safety measure to assume the device is operating in the worst case temperature (–40 °C).
- After the initial stage—the voltage is set based on the ambient temperature and VID-fused value.

After entering user mode (in the monitor stage), the SDM Power Manager monitors temperature changes and decides if the V_{CC} and V_{CCP} output voltage values need to be updated. If voltages require updating, the SDM Power Manager identifies the voltage value based on the fuse values and the current temperature and sends the desired voltage value to the voltage regulators through the PMBus interface.

Figure 22. PMBus Master Mode

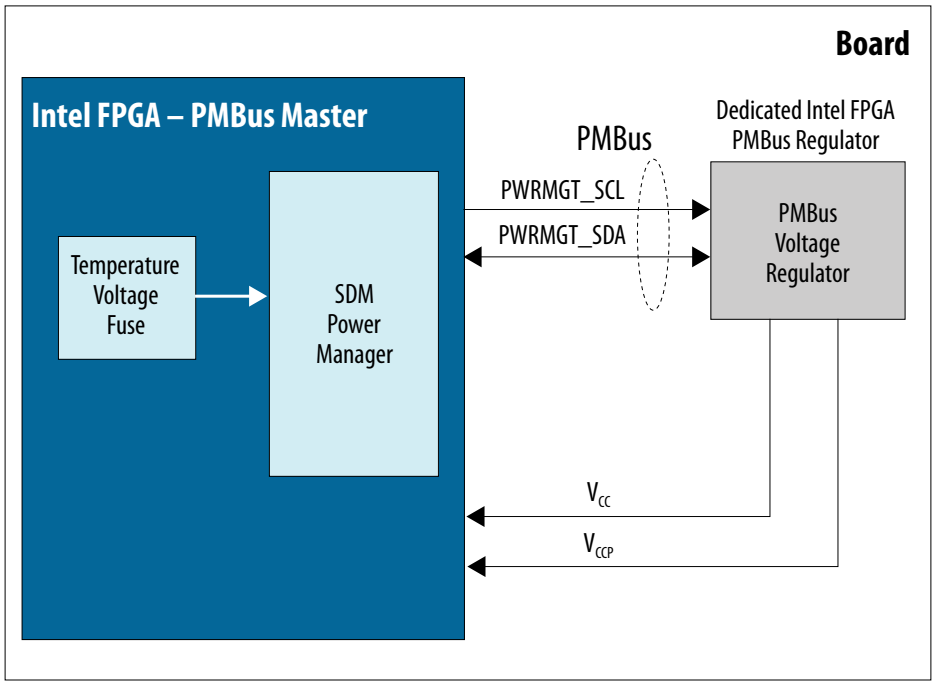


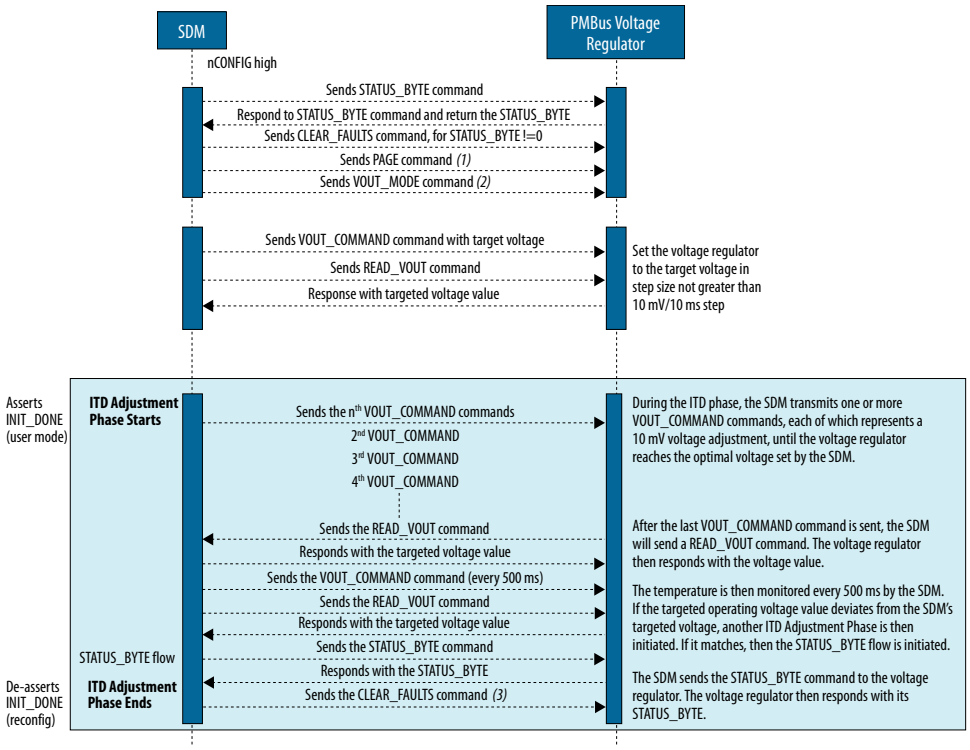
Table 21. Supported Commands for the PMBus Master Mode

Command Name	Command Code	Default	PMBus Transaction Type	Number of Bytes
PAGE(12)	00h	—	Write byte	1
VOUT_MODE	20h	—	Read byte	1
VOUT_COMMAND	21h	—	Write word	2
READ_VOUT	8Bh	—	Read word	2
MFR_ADC_CONTROL(13)	D8h	—	Write byte	1
STATUS_BYTE	78h	00h	Read byte	1
CLEAR_FAULTS	03h	—	Write byte	0

(12) This is an optional command. This command is only applicable if you enable the PAGE command parameter. For more information, refer to the Power Management and VID Parameters section.

(13) This command is sent when you set the device type to LTM4677 only.

Figure 23. Flow between the PMBus Voltage Regulator and FPGA in the PMBus Master Mode



Notes:
(1) The PAGE command is only sent if PAGE is enabled in the Intel Quartus GUI setting.
(2) This command is only sent if the slave device type selected is not "Other" in the Intel Quartus GUI setting.
(3) The SDM sends the CLEAR_FAULTS command to the voltage regulator only if any bits in the lower 8 bits of the STATUS_BYTE is set. If no bits are set, exit the ITD flow.

Multi-Master Mode

The PMBus master mode supports the multi-master mode.

When multiple devices start to communicate at the same time, the device writing the most zeros to the bus or the slowest device wins the arbitration. The other devices immediately discontinue any operation on the bus. When there is an on-going bus communication, all devices must detect the communication and not interrupt it. The devices must wait for a stop condition to appear before starting communication to the bus. Once the stop condition is received on the bus, the next device that wins arbitration sends a start condition by pulling the PWRMGT_SDA low to re-initialize the bus communication.

In this mode, all master devices must be multi masters in a multi-master system. Single-master systems may not understand the arbitration and the busy detection mechanisms can cause unpredictable results.

5.1.2.2. PMBus Slave Mode

Intel Agilex 7 devices can also be configured in the PMBus slave mode with an external power management controller acting as the PMBus master. The external power management controller that interact with Intel Agilex 7 devices over PMBus

must support clock stretching. The external power management controller is responsible for driving all PMBus transactions, querying the FPGA for its target voltage requirements and interacting with the voltage regulators to configure them to the FPGA's target voltage.

For the PMBus slave mode with PWRMGT_ALERT, you must follow the guidelines listed below for the external PMBus flow:

- Figure: *Handshake Flow between the External PMBus Master and FPGA in the PMBus Slave Mode with the PWRMGT_ALERT Signal*
- Figure: *Handshake between the External PMBus Master and FPGA in the PMBus Slave Mode Timing Diagram with PWRMGT_ALERT*
- Table: *Stage Flow for the External PMBus Master when the PWRMGT_ALERT Signal is Asserted and STATUS_BYTE = 0*
- Table: *Stage Flow for the External PMBus Master when the PWRMGT_ALERT Signal is Asserted and STATUS_BYTE is not Equal to 0*

Figure 24. PMBus Slave Mode

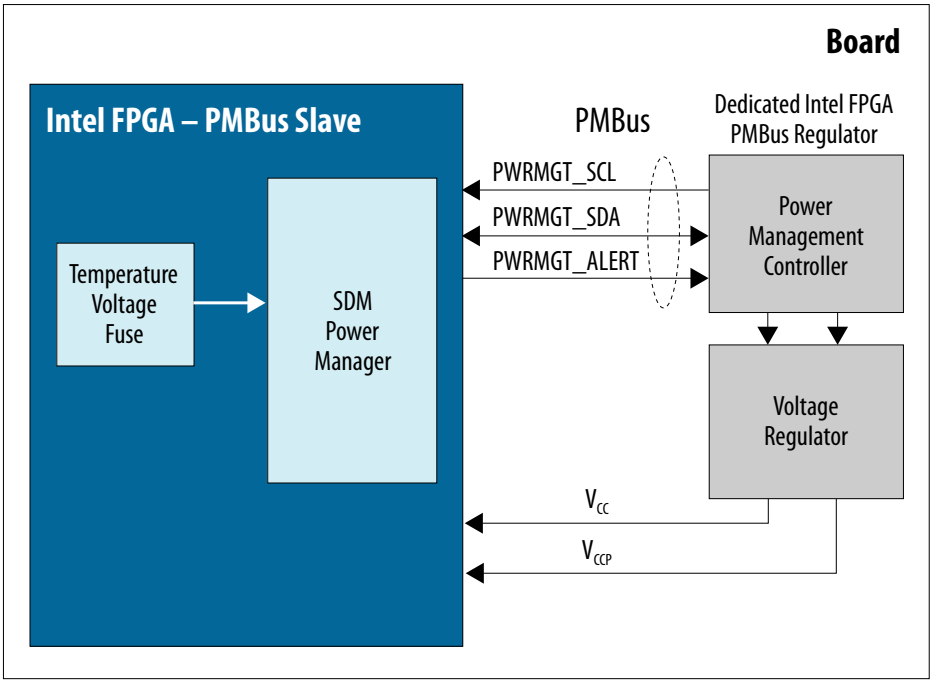
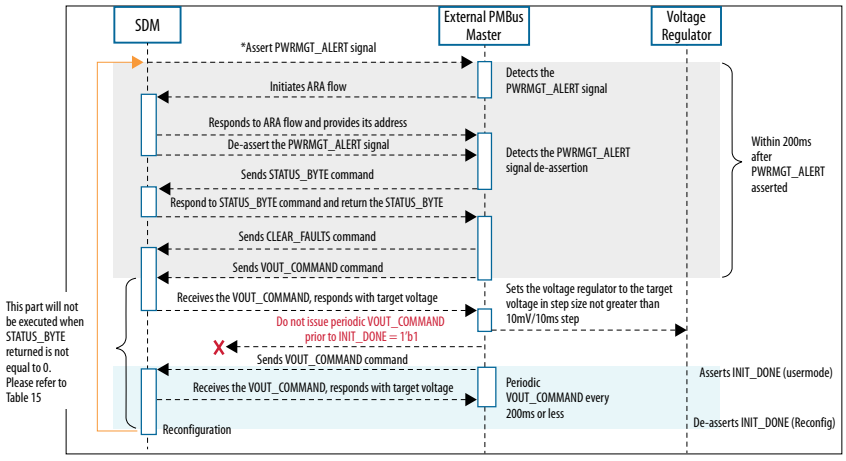


Table 22. Supported Commands for the PMBus Slave Mode

Command Name	Command Code	Default	PMBus Transaction Type	Number of Bytes
CLEAR_FAULTS	03h	—	Send byte	0
VOUT_MODE	20h	40h	Read byte	1
VOUT_COMMAND	21h	—	Read word	2
STATUS_BYTE	78h	00h	Read byte	1

Figure 25. Handshake Flow between the External PMBus Master and FPGA in the PMBus Slave Mode with the PWRMGT_ALERT Signal



*The external PMBus master must poll the state of the PWRMGT_ALERT pin periodically, at an interval not longer than 100 ms until the PWRMGT_ALERT signal is asserted.

Note:

(1) The following are the details of the alert response address (ARA) flow:

(a) When operating in the slave mode with PWRMGT_ALERT PMBus connection, the slave device uses the PWRMGT_ALERT signal to indicate the master device that an update is required.
(b) Upon reception of the PWRMGT_ALERT signal, the external master device uses the ARA flow to determine which slave device has asserted the PWRMGT_ALERT signal.
(c) The ARA flow is one-byte, broadcast read from the master device to the reserved Alert Response Address (0x0C).
(d) The slave device that has asserted the PWRMGT_ALERT signal responds to this ARA flow with its address.
(e) The slave device de-asserts the PWRMGT_ALERT signal after providing its address. The external master device uses the address provided to communicate with the correct slave device.

Table 23. Stage Flow for the External PMBus Master when the PWRMGT_ALERT Signal is Asserted and STATUS_BYTE=0

Sequence	SDM	PMBus Master	Notes
1	Asserts the PWRMGT_ALERT signal	—	—
2	—	Detects the PWRMGT_ALERT signal	—
3	—	Initiates the ARA flow	—
4	Responds to the ARA flow and provides its address	—	Only the device which has asserted the PWRMGT_ALERT signal in step 1 responds to the ARA flow by providing its address.
5	De-asserts the PWRMGT_ALERT signal	—	The PWRMGT_ALERT signal is only de-asserted after the SDM responds with its address in the ARA flow.
6	—	Reads the STATUS_BYTE	—
7	Returns STATUS_BYTE=0	—	Indicates the FPGA voltage requires an update.
8	—	Sends CLEAR_FAULTS	—
9	—	Sends VOUT_COMMAND	The VOUT_COMMAND must be received by the SDM within 200ms after the

continued...

Sequence	SDM	PMBus Master	Notes
			PWRMGT_ALERT signal is asserted. Failure to meet this requirement causes configuration error. (14)
10	Receives the VOUT_COMMAND, responds with the target voltage	—	Calculated based on the temperature, the VID fuse and the coefficient for the direct format (you need to specify this input).
11	—	Sets the voltage regulator to the target voltage in step size not greater than 10mV/ 10ms step	—

Table 24. Stage Flow for the External PMBus Master when the PWRMGT_ALERT Signal is Asserted and STATUS_BYTE is not equals to 0

Sequence	SDM	PMBus Master	Notes
1	Asserts the PWRMGT_ALERT signal	—	The SDM detects fault and asserts the PWRMGT_ALERT signal. (15)
2	—	Detects the PWRMGT_ALERT signal	—
3	—	Initiates the ARA flow	—
4	Responds to the ARA flow and provides its address	—	Only the device which has asserted the PWRMGT_ALERT signal in step 1 responds to the ARA flow by providing its address.
5	De-asserts the PWRMGT_ALERT signal	—	The PWRMGT_ALERT signal is only de-asserted after the SDM responds with its address in the ARA flow.

continued...

(14) When there is an error triggered by the SDM because it did not receive the VOUT_COMMAND within the specified time, you must power cycle the device to recover from the error. If you do not power cycle the device to recover from the error, you cannot configure the device successfully.

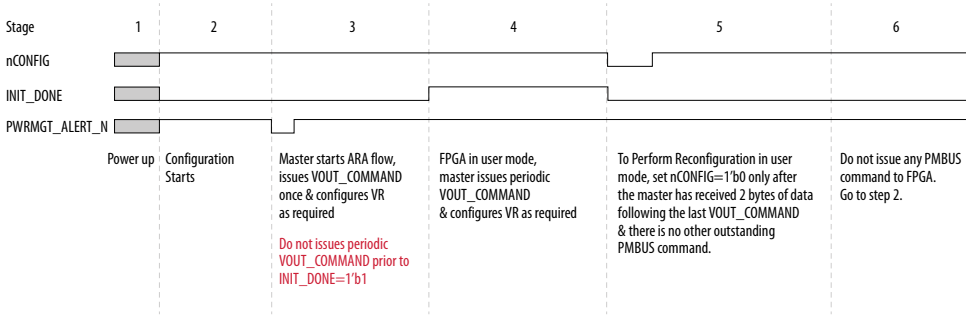
(15) The following faults can raise the PWRMGT_ALERT signal:

- PMBUS_ERR_RD_TOO_MANY_BYTES (Error with the length of the PMBus/I2C message length)
- PMBUS_ERR_WR_TOO_MANY_BYTES (Error with the length of the PMBus/I2C message length)
- PMBUS_ERR_UNSUPPORTED_CMD (VOUT_COMMAND, VOUT_MODE, READ_STATUS, and CLEAR_FAULTS are the only supported commands in the PMBUS Slave Mode)
- PMBUS_ERR_READ_FLAG (Received duplicate command before being able to respond to the first command)
- PMBUS_ERR_INVALID_DATA (Invalid or malformed PMBus/I2C message)

If any of the above errors are detected, the PWRMGT_ALERT signal is raised and bit 1 of the status register is set.

Sequence	SDM	PMBus Master	Notes
6	—	Reads the STATUS_BYTE	—
7	Returns the STATUS_BYTE when not equal to 0	—	Indicates that other fault has occurred
8	—	Sends CLEAR_FAULTS	To reset the STATUS_BYTE.
9	—	Reads the STATUS_BYTE	To confirm that STATUS_BYTE=0.
10	—	External master to handle the faults	—

Figure 26. Handshake between the External PMBus Master and FPGA in the PMBus Slave Mode Timing Diagram with PWRMGT_ALERT



The Intel Agilex 7 devices in the PMBus slave mode sends the VOUT_COMMAND value in the direct format only. To read the actual voltage value, use the following equation to convert the VOUT_COMMAND value from the Intel Agilex 7 devices.

Figure 27. Direct Format Equation

$$X = \frac{1}{m}\left(Y \times 10^{-R} - b\right)$$

The equation shows how to convert the direct format value where:

- X, is the calculated, real value in mV;
- m, is the slope coefficient, a 2-byte two's complement integer;
- Y, is the 2-byte two's complement integer received from the Intel Agilex 7 devices;
- b, is the offset, a 2-byte two's complement integer;
- R, is the exponent, a 1-byte two's complement integer

The following example shows how an external power management controller retrieves values from the Intel Agilex 7 devices. Coefficients used in the VOUT_COMMAND are as follows:

- m = 1
- b = 0
- R = 0

If the external power management controller retrieved a value of 0384h, it is equivalent to the following:

$X = (1/1) \times (0384h \times 10^{-0} - 0) = 900\ mV = 0.90\ V$

5.1.2.3. Fail Safe Mechanism

If a miscommunication situation happens between the FPGA device and the external voltage regulator, the voltage regulator might be supplying unexpected voltage to the FPGA device.

To avoid voltage supply issue to the FPGA device, a safety net check processing is implemented in the Intel Quartus Prime software against your input setting (coefficient value—m, b, r for the direct mode and N for the linear mode) in the power management GUI.

The fail safe mechanism detects the early issue during the configuration phase, before the PMBus communication is established with the voltage regulator, prior to any voltage adjustment. If an error occurred, configuration is unsuccessful.

The Intel Quartus Prime software maintains a list of Intel validated voltage regulator's coefficient values. During configuration, the firmware performs the calculation and conversion based on the information of your selected voltage regulator in the Intel Quartus Prime GUI to obtain the respective voltage regulator data, using the PMBus Direct or Linear format formula. The calculated data is then compared against the Intel's maintained voltage regulator information in the Intel Quartus Prime software. If there is no matching data, configuration fails and the VOUT_COMMAND is not sent. However, this safety net check is not applicable when you select the voltage regulator type as "Other" in the Intel Quartus Prime GUI.

5.1.2.4. Fault Management and Error Reporting

The SDM firmware has the capability to detect error, fault, or warning in the PMBus throughout the initialization and monitor states. The firmware analyzes any error and put it into the Error Message Queue (EMQ). During configuration, the CONFIG_STATUS mailbox command notifies you about the error.

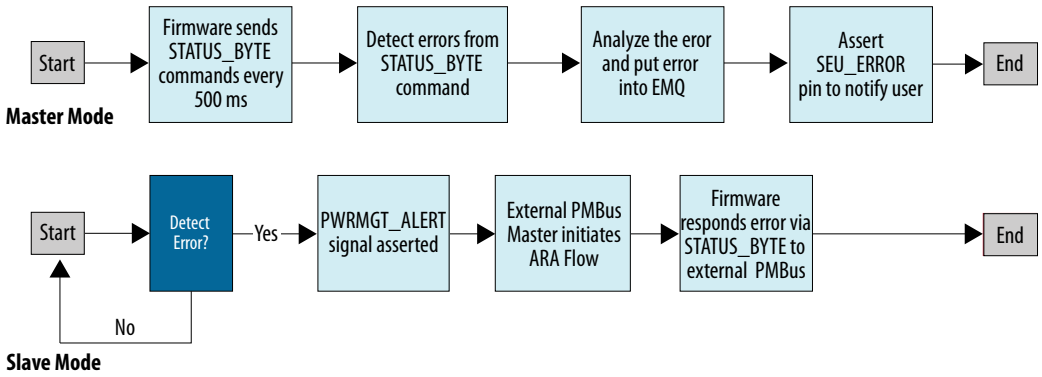
In the master mode while running the monitor state, the SDM firmware queries the voltage regulator with a STATUS_BYTE command for every 500 ms. If the value returned from the STATUS_BYTE is not equal to zero, it indicates an error, fault, or warning within the voltage regulator. This firmware reports the error through the EMQ and assert the SEU_ERROR pin to notify you of this error.

The SDM firmware asserts the PWRMGT_ALERT signal whenever there is an error occurred. The external PMBus master has to initiate the ARA flow to handshake with the FPGA to read the error from the firmware.

The STATUS_BYTE Polling

The STATUS_BYTE polling is an optional feature. By default, the STATUS_BYTE polling is disabled when choosing slave device type "Other" and enabled when selecting voltage regulator listed in the Intel Quartus Prime software. To change the setting of the STATUS_BYTE polling, refer to the *Specifying Power Management and VID Parameters and Option* section and Table: *Power Management and VID Parameters*.

Figure 28. Fault Management and Error Reporting



Note: The polling of the STATUS_BYTE every 500 ms in the master mode is applicable when you select the voltage regulator that has been validated by Intel. If you select "Others" in the Intel Quartus Prime GUI, the STATUS_BYTE polling is disabled.

The following table shows the error of the STATUS_BYTE based on the return bit.

Table 25. STATUS_BYTE Error Definition

Command	Error Definition
STATUS_BYTE (78h)	Bit[7]: Busy, unable to respond
	Bit[6]: Off, not enabled
	Bit[5]: Output over voltage fault occurred
	Bit[4]: Output over current fault occurred
	Bit[3]: Input under voltage fault occurred
	Bit[2]: Temperature fault or warning occurred
	Bit[1]: Communication, memory, or logic fault occurred
	Bit[0]: The fault occurred that are not listed above

Each bit returns from the STATUS_BYTE indicate a different error occurring in the voltage regulator and firmware reports each of them into the EMQ. For example, a value of `0x6` (`b'0000_0110`) returns from the STATUS_BYTE read reports that the voltage regulator is having communication, memory, or logic fault and temperature fault or warning asserted, the firmware inputs there 2 error entries into the EMQ for each of the error or fault occurred.

You must program non-volatile memory (NVM) in the voltage regulator correctly to ensure the error flag is not asserted incorrectly for the expected operating condition.

For Intel Agilex 7 SmartVID devices, V_{CC} and V_{CCP} operate within the 0.70 V to 0.90 V voltage range. The following is the example settings that works for this voltage range. You may revise the settings based on your system requirements.

```
VOUT_OV_WARN_LIMIT to VID_MAX 920mV
VOUT_OV_FAULT_LIMIT to VID_MAX 930mV
VOUT_MAX to VID_MAX 950mV
VOUT_UV_WARN_LIMIT to VID_MIN 690mV
VOUT_UV_FAULT_LIMIT to VID_MIN 680mV
```

Limit should be wider or larger than the expected operating conditions, but within the absolute maximum rating for the device. For more information, refer to the *Intel Agilex 7 FPGAs and SoCs Device Data Sheet: F-Series and I-Series*.

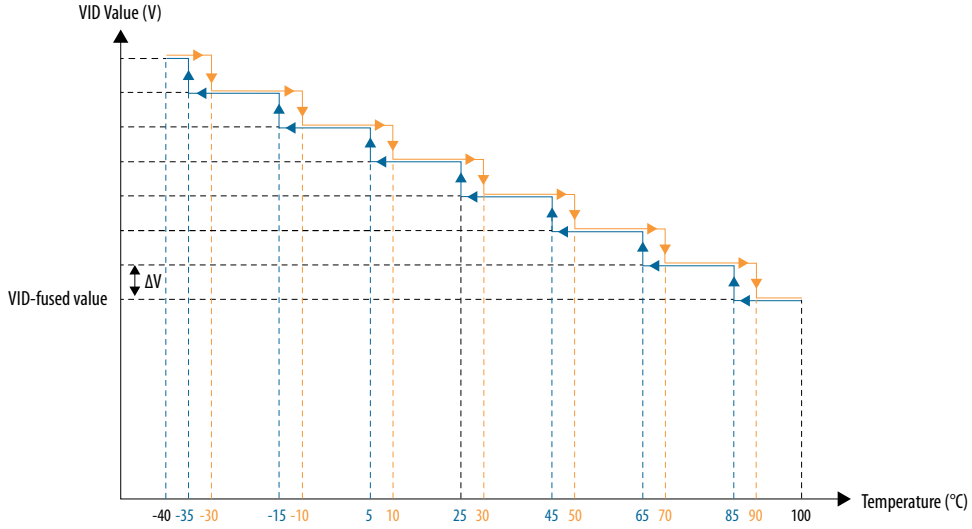
5.1.3. Temperature Compensation

Intel Agilex 7 devices are able to compensate for performance degradation at colder temperatures by raising the voltage. While raising the voltage increases the dynamic power consumption, the increase in dynamic power consumption is countered by lower leakage at cold temperatures, thus enabling total power consumption at cold temperatures to still be equal or lower than at hot temperatures.

The SmartVID feature supports this dynamic voltage adjustment. The SDM Power Manager checks for local temperature sensor changes and updates the new VID value with voltage step not more than 5 mV if the temperature crosses the threshold point.

Figure 29. Temperature Compensation for SmartVID for Intel Agilex 7 Devices—Preliminary

The SDM monitors the temperature, normally at every 100 ms, and adjusts the voltage by communicating with the power management system. Dynamic voltage adjustment is made by the SDM after the sensor detects the temperature setting changes for every 20±5 °C.



5.1.4. Intel Agilex 7 Power Management and VID Implementation Guide

The Intel Agilex 7 SDM Power Management Firmware manages the SmartVID configuration and enables the FPGA to power up before you can access the FPGA.

The Intel Agilex 7 Power Management and VID interface is installed as part of the Intel Quartus Prime software.

5.1.4.1. Specifying Power Management and VID Parameters and Options

1. Create an Intel Quartus Prime project using the **New Project Wizard** available from the File menu.
2. On the **Assignments** menu, click **Device**.
3. On the **Device** dialog box, click **Device and Pin Options**.

4. On the **Device and Pin Options** dialog box, click **Configuration**.
5. On the **Configuration** page, specify the **VID Operation mode**. There are two modes available—PMBus Master and PMBus Slave.
6. The PMBus modes consist of these pins—PWMGT_SDA, PWMGT_SCL, and PWRMGT_ALERT. To configure these pins, on the **Configuration** page, click **Configuration Pin Options**. The PWRMGT_ALERT pin is only available and is required to be used in the slave mode. For the configuration pin parameters, refer to Table: *Configuration Pin Parameters*.
7. On the **Configuration Pin** dialog box, assign the appropriate SDM_IO pin to the power management pins. Click **OK**.
8. On the **Device and Pin Options** dialog box, click **Power Management and VID** to specify the device settings if your device is in the PMBus Master mode. Click **OK**. For the power management and VID parameters, refer to Table: *Power Management and VID Parameters*.

This completes the SmartVID setup for the Intel Agilex 7 device.

5.1.4.1.1. Configuration Pin Parameters

Table 26. Configuration Pin Parameters

Use the parameter editor to configure these options.

Parameters	Value	Description
Use PWRMGT_SCL output	SDM_IO0 SDM_IO14	This is a required PMBus interface for the power management when the VID operation mode is the PMBus Master or PMBus Slave mode. Disable this parameter for the non-SmartVID device. Intel recommends using the SDM_IO14 pin for this parameter.
Use PWRMGT_SDA output	SDM_IO11 SDM_IO12 SDM_IO16	This is a required PMBus interface for the power management when the VID operation mode is the PMBus Master or PMBus Slave mode. Disable this parameter for the non-SmartVID device. Intel recommends using the SDM_IO11 pin for this parameter.
Use PWRMGT_ALERT output	SDM_IO0 SDM_IO12	This is a required PMBus interface for the power management when the VID operation mode is the PMBus Slave mode. Disable this parameter for the non-SmartVID device. Intel recommends using the SDM_IO12 pin for this parameter.

5.1.4.1.2. Power Management and VID Parameters

You can use the following parameters to configure the Power Management and VID interface if the VID operation is in the PMBus Master mode.

Table 27. Power Management and VID Parameters

Parameters	Value	Description
Bus speed mode[16]	100 KHz	Bus speed mode of PMBus interface when operating in the PMBus Master mode.
	400 KHz	
STATUS_BYTE polling	Enable	By enabling the STATUS_BYTE polling in the master mode, the firmware sends the STATUS_BYTE command for every 500 ms. This allows the firmware to analyze the error and put it into the EMQ.
	Disable	
Slave device type[16]	ISL682XX	Supported device types. Intel recommends you to use one of the slave device type listed in the drop-down menu that has been tested with the Intel FPGA tools. If you are not using one of the slave device type listed in the drop-down menu, select **Other** option. When you select **Other** option, refer to Table: *SmartVID Regulator Requirements*, Table: *Supported Voltage Output Format for F-Series and I-Series Devices with –V, –E, and –X Power Options*, and Table: *Supported Commands for the PMBus Master Mode* for the voltage regulator requirements details.
	LTC3888	
	LTM4677	
	Other	
Device address in PMBus Slave mode[17]	7-bit hexadecimal value	Device address in the PMBus Slave mode.
Number of slave device	1 to 7, or All	Indicates the number of voltage regulator in the system.
Slave device_0 address[16]	7-bit hexadecimal value	External power regulator address. This parameter must be non-zero when you are using the PMBus Master mode.
Slave device_1 address[16]	7-bit hexadecimal value	External power regulator address.
Slave device_2 address[16]	7-bit hexadecimal value	External power regulator address.
Slave device_3 address[16]	7-bit hexadecimal value	External power regulator address.
Slave device_4 address[16]	7-bit hexadecimal value	External power regulator address.
Slave device_5 address[16]	7-bit hexadecimal value	External power regulator address.
Slave device_6 address[16]	7-bit hexadecimal value	External power regulator address.
Slave device_7 address[16]	7-bit hexadecimal value	External power regulator address.
Voltage output format[16], [18]	Direct format	The voltage output format when the operation mode is PMBus Master.

continued...

(16) This parameter is used for the PMBus Master mode.

(17) This parameter is used for the PMBus Slave mode.

Parameters	Value	Description
	Linear format	If the voltage output format is the Direct format, you must set the following parameters: • Direct format coefficient m • Direct format coefficient b • Direct format coefficient R If the voltage regulator is the Linear format, you must set the Linear format N parameter. (19) For more information about the parameters, refer to your selected voltage regulator data sheet. For all voltage output format, you must also select the correct "translated voltage output unit".
Direct format coefficient m(16)	Signed integer: -32768 to 32767	Direct format coefficient m of the slave device type when the operation mode is PMBus Master.
Direct format coefficient b(16)	Signed integer: -32768 to 32767	Direct format coefficient b of the slave device type when the operation mode is PMBus Master.
Direct format coefficient R(16)	Signed integer: -128 to 127	Direct format coefficient R of the slave device type when the operation mode is PMBus Master.
Linear format N(16)	Signed integer: –16 to 15	Output voltage command when the voltage output format is set to the Linear format.
Translated voltage value unit(16)	millivolts	Indicates the translated output voltage is in millivolts (mV) or volts (V).
	volts	
Enable PAGE command(16)	Enable	By enabling the PAGE command, the FPGA PMBus Master uses the PAGE command to set all the output channels (0xFF) on registered regulator modules to respond to VOUT_COMMAND. If only specified output channels on registered regulator modules must respond to VOUT_COMMAND, enter the corresponding page value (0x00 – 0xFF).
	Disable	

5.1.4.1.3. Power Management and VID Interface QSF Constraint Guide

You can specify the **Power Management and VID** parameters and options through QSF constraints command.

(18) The Auto Discovery format is no longer available in the GUI selection for the Intel Agilex 7 devices starting from the Intel Quartus Prime software version 22.2 onwards. When migrating your design project from the Intel Quartus Prime software version 22.1 (or older) to the Intel Quartus Prime software version 22.2 (or later), you can select either the Direct format or Linear format listed in the GUI.

(19) N is the exponent of a 5-bit two's compliment integer.

For the configuration pin parameters, refer to Table: *Configuration Pin Parameters*. For the power management and VID parameters, refer to Table: *Power Management and VID Parameters*.

The following is the example of the VID parameter settings in the QSF. The value maybe different based on your usage and choice of voltage regulator.

Example 1. Specifying the Power Management and VID Parameters through QSF Constraints

```
set_global_assignment -name USE_PWRMGT_SDA SDM_IO11
set_global_assignment -name USE_PWRMGT_SCL SDM_IO14
set_global_assignment -name PWRMGT_SLAVE_DEVICE_TYPE LTM4677
set_global_assignment -name PWRMGT_SLAVE_DEVICE0_ADDRESS41
set_global_assignment -name PWRMGT_SLAVE_DEVICE1_ADDRESS42
set_global_assignment -name PWRMGT_SLAVE_DEVICE2_ADDRESS43
set_global_assignment -name PWRMGT_SLAVE_DEVICE3_ADDRESS44
set_global_assignment -name PWRMGT_SLAVE_DEVICE4_ADDRESS45
set_global_assignment -name PWRMGT_SLAVE_DEVICE5_ADDRESS46
set_global_assignment -name PWRMGT_SLAVE_DEVICE6_ADDRESS47
set_global_assignment -name PWRMGT_SLAVE_DEVICE7_ADDRESS48
set_global_assignment -name VID_OPERATION_MODE "PMBUS MASTER"
set_global_assignment -name PWRMGT_BUS_SPEED_MODE "100 KHZ"
set_global_assignment -name PWRMGT_PAGE_COMMAND_ENABLE ON
set_global_assignment -name PWRMGT_VOLTAGE_OUTPUT_FORMAT "LINEAR FORMAT"
set_global_assignment -name PWRMGT_LINEAR_FORMAT_N "-12"
set_global_assignment -name PWRMGT_TRANSLATED_VOLTAGE_VALUE_UNIT VOLTS
set_global_assignment -name PWRMGT_PAGE_COMMAND_PAYLOAD xx
```

5.2. DSP and M20K Power Gating

Intel Agilex 7 devices support power gating for both DSP blocks and M20K memory blocks. By default, the Intel Quartus Prime software automatically configures unused DSP blocks and M20K memory blocks to be power gated.

5.3. Clock Gating

Clock gating can be used to reduce dynamic power consumption. When an application is idle, its clock can be gated temporarily and ungated based on wake-up events. This is done using user logic to enable or disable the programmable clock routing.

You can perform dynamic power reduction by gating the clock signals of any circuitry not used by the design in the Intel Agilex 7 devices.

Clock networks can be gated using one of the following methods:

Root Clock Gate

You can dynamically gate each clock network at the root level using the Clock Control Intel FPGA IP Core.

Sector Clock Gate

You can dynamically gate each clock network at the clock sector level using the Clock Control Intel FPGA IP Core.

I/O PLL Clock Gate

You can dynamically gate each output counter of the Intel Agilex 7 I/O PLLs using IOPLL Reconfiguration.

Clock gating a large portion of your FPGA design could cause significant current change over a short time period when the gated circuitry is enabled or disabled. The maximum current step resulting from this clock gating should be sized such that it does not create noise exceeding the maximum allowed AC noise specification, as determined by the PDN decoupling design on your PCB. You can control the current step size by dividing a large gated area into smaller sub-regions and staging those regions to enter or exit power gating sequentially.

For more details, refer to the *Clock Gating* section in the *Intel Agilex 7 Clocking and PLL User Guide: F-Series and I-Series*.

Related Information

- Intel Agilex 7 Clocking and PLL User Guide: F-Series and I-Series
  Provides more information about clock gating for F-Series and I-Series FPGAs.
- Intel Agilex 7 Clocking and PLL User Guide: M-Series
  Provides more information about clock gating for M-Series FPGAs.

5.4. Power Sense Line

Intel Agilex 7 devices support the power sense line feature. VCCLSENSE and GNDSENSE pins are differential remote sense pins used to monitor the V_{CC} power supply.

You must connect the VCCLSENSE and GNDSENSE pins to the remote sense inputs for the regulator supplying V_{CC} rail that supports the remote voltage sensing feature.

5.5. Power Optimization Techniques in the Intel Quartus Prime Software

The Intel Quartus Prime software offers power-driven compilation to fully optimize device power consumption.

Power-driven compilation focuses on reducing the design's total power consumption in synthesis and place-and-route stages. For detailed information, refer to the *Intel Quartus Prime Pro Edition User Guide: Power Analysis and Optimization*.

Related Information

Intel Quartus Prime Pro Edition User Guide: Power Analysis and Optimization

6. Document Revision History for the Intel Agilex 7 Power Management User Guide

Document Version	Changes
2023.07.17	• Added the STATUS_BYTE polling parameter in Table: *Power Management and VID Parameters*. • Updated the *Power-Up Sequence Requirements* section. • Updated the *Fault Management and Error Reporting* section. • Updated *The STATUS_BYTE Polling* section. • Updated Figure: *Flow between the PMBus Voltage Regulator and FPGA in the PMBus Master Mode*. • Updated Figure: *Fault Management and Error Reporting*.
2023.07.05	• Updated the ALERT_n guidelines in the *Fault Management and Error Reporting* section. • Updated Table: *Voltage Rails Group for the Intel Agilex 7 M-Series Devices*. • Removed the note about restricted support for Intel Agilex 7 M-Series FPGAs.
2023.04.03	• Added support for Intel Agilex 7 M-Series FPGAs. • Added guidelines for reading the R-Tile local temperature sensor. • Updated the *Power-Up Sequence Requirements* section. • Updated the *Guidelines for I/O Pins in GPIO, HPS, and SDM Banks During Power Sequencing* section. • Updated the *Power-On Reset* section. • Updated the *Power Supplies Monitored by the POR Circuitry* section. • Updated the *SmartVID Standard Power Devices* section. • Updated the *PMBus Slave Mode* section. • Updated Table: *Power Rails Floating Voltage for the Intel Agilex 7 F-Series and I-Series*. • Updated Table: *The PMBus Master and Slave Modes Interfaces for the Intel Agilex 7 Devices*. • Updated the *Specifying Power Management and VID Parameters and Options* section. • Updated Table: *Power Management and VID Parameters* to include the supported voltage output format. • Updated the description of the *Use PWRMGT_ALERT output* parameter in Table: *Configuration Pin Parameters*. • Updated Figure: *PMBus Slave Mode*. • Updated Figure: *Fault Management and Error Reporting*. • Updated the topic about the temperature sensor locations: — Updated the temperature sensing diode locations figure to show all possible locations for all Intel Agilex 7 devices. — Added tables listing the availability of the temperature sensors in different Intel Agilex 7 series, densities, and packages. • Removed Table: *Stage Flow for the External PMBus Master without the PWRMGT_ALERT Signal and STATUS_BYTE=0*. • Removed Table: *Stage Flow for the External PMBus Master without the PWRMGT_ALERT Signal and STATUS_BYTE is not Equal to 0*. • Removed Figure: *Handshake Flow between the External PMBus Master and FPGA in the PMBus Slave Mode without PWRMGT_ALERT*. • Removed Figure: *Handshake between the External PMBus Master and FPGA in the PMBus Slave Mode Timing Diagram without the PWRMGT_ALERT Signal*. • Retitled the document from *Intel Agilex™ 7 Power Management User Guide: F-Series and I-Series* to *Intel Agilex 7 Power Management User Guide*.

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Document Version	Changes
2023.02.20	• Added the AGI 041 device. • Updated product family name to "Intel Agilex 7". • Retitled the document from *Intel Agilex F-Series and I-Series Power Management User Guide* to *Intel Agilex 7 Power Management User Guide: F-Series and I-Series*.
2022.12.19	• Added the *Floating Voltage* section. • Updated the document title from *Intel Agilex Power Management User Guide* to *Intel Agilex F-Series and I-Series Power Management User Guide*. • Updated the VID-fused value in the *SmartVID Feature Implementation in Intel Agilex Devices* section. • Updated the *PMBus Master Mode* section. • Updated the default value of the VOUT_MODE command and the PMBus transaction type of the CLEAR_FAULTS command in Table: *Supported Commands for the PMBus Master Mode*.
2022.09.06	Updated the *Multi-Master Mode* section.
2022.08.08	Updated the F-tile and R-tile bank names for location 7 in the table listing the local temperature sensor locations and corresponding transceiver bank names.
2022.06.21	• Updated the topic about the temperature sensor locations: — Updated the list of devices for each location diagram. — Added a table listing the local temperature sensor locations and corresponding transceiver bank names. • Updated Table: *Voltage Rails Group*. • Updated Figure: *Flow between the PMBus Voltage Regulator and FPGA in the PMBus Master Mode*.
2022.05.27	Removed instances of Enpirion from *Choosing a Power Tree* and *Power Generation* sections and *Power Management and VID Parameters* table.
2022.04.15	• Updated the *Power-Up Sequence Requirements* section to include details for the V_{CCBAT} power supply. • Removed the V_{CCBAT} power supply from the *Power Supplies Monitored by the POR Circuitry* section.
2022.04.04	• Added the *Fail Safe Mechanism* section. • Added the *Fault Management and Error Reporting* section. • Added Figure: *Flow between the PMBus Voltage Regulator and FPGA in the PMBus Master Mode*. • Updated the *Clock Gating* section. • Updated the *Intel Agilex Power Management and VID Interface QSF Constraint Guide* section. • Updated Figure: *Handshake Flow between the External PMBus Master and FPGA in the PMBus Slave Mode without PWRMGT_ALERT*. • Updated the $V_{CCH\_FGT\_GXF}$ and $V_{CCEHT\_FHT\_GXF}$ power rails in Table: *Voltage Rails Group* . • Updated Table: *Power Management and VID Parameters* to include ISL682XX voltage regulator. • Updated the descriptions of the figures showing the temperature sensing diode locations to clarify that each figure shows the top view of the die. In the Intel Quartus Prime Chip Planner, the view is flipped.
2022.01.25	Updated the topic that shows the temperature sensor locations to clarify that the figures show the top view of the devices as shown in the Intel Quartus Prime Chip Planner.
2021.12.13	Updated the VCCRCORE pin name.
2021.10.29	• Added Table: *Power Rails Status for Intel Agilex Devices*. • Added Table: *Stage Flow for the External PMBus Master without the PWRMGT_ALERT Signal and STATUS_BYTE=0*. • Added Table: *Stage Flow for the External PMBus Master without the PWRMGT_ALERT Signal and STATUS_BYTE is not Equal to 0*. • Added Figure: *Handshake Flow between the External PMBus Master and FPGA in the PMBus Slave Mode with PWRMGT_ALERT*. • Added Figure: *Handshake between the External PMBus Master and FPGA in the PMBus Slave Mode Timing Diagram without the PWRMGT_ALERT Signal*.

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Document Version	Changes
	• Added Figure: *Handshake Flow between the External PMBus Master and FPGA in the PMBus Slave Mode without PWRMGT_ALERT*. • Updated Table: *Comparison of Intel FPGA Power and Thermal Calculator and Intel Quartus Prime Power Analyzer Capabilities*. • Updated Table: *Supported Commands for the PMBus Master Mode*. • Updated Table: *Stage Flow for the External PMBus Master when the PWRMGT_ALERT Signal is Asserted and STATUS_BYTE=0*. • Updated Table: *Stage Flow for the External PMBus Master when the PWRMGT_ALERT Signal is Asserted and STATUS_BYTE is not equals to 0*. • Updated Table: *Configuration Pin Parameters*. • Updated Table: *Power Management and VID Parameters*. • Updated Table: *Local Temperature Sensor Locations and Equivalent Remote TSD Pin Names*. • Updated Figure: *PMBus Slave Mode*. • Updated Figure: *Temperature Sensing Diode Locations—Intel Agilex AGF 006 and AGF 008*. • Updated Figure: *Temperature Sensing Diode Locations—Intel Agilex AGF 012, AGF 014, AGF019, AGF 022, AGF023, AGF 027, AGI019, AGI 022, AGI023, and AGI 027*. • Updated the *Intel Agilex Power Management Overview* section. • Updated the *Catastrophic Trip Signal* section. • Updated the *Guidelines for I/O Pins in GPIO, HPS, and SDM Banks During Power Sequencing* section. • Updated the *Power-Down Sequence Requirements for Intel Agilex Devices with E-Tile* section. • Updated the *SmartVID Standard Power Devices* section. • Updated the *PMBus Master Mode* section. • Updated the *PMBus Slave Mode* section. • Updated the *Specifying Power Management and VID Parameters and Options* section. • Removed the *Intel Agilex Power Management and VID Interface Getting Started* section and merged the content into the *Intel Agilex Power Management and VID Implementation Guide* section. • Removed Figure: *External PMBus Master Software Flow*.
2021.07.02	• Updated the *SmartVID Standard Power Devices* section. • Updated the *SmartVID Feature Implementation in Intel Agilex Devices* section. • Updated the *SDM Power Manager* section. • Updated the *Temperature Compensation* section. • Updated Figure: *Handshake between the External PMBus Master and FPGA in the PMBus Slave Mode Timing Diagram*. • Updated Figure: *Temperature Compensation for SmartVID for Intel Agilex Devices*.
2021.06.09	• Updated the catastrophic trip signal information. The signal now drives low when the temperature is higher than 120°C.
2021.04.13	• Added information for temperature sensors in R-tile and F-tile transceivers. • Added the *Multi-Master Mode* section. • Added reference to the *Intel Stratix® 10 and Intel Agilex SmartVID Debug Checklist*. • Added reference to the *Intel FPGA Power and Thermal Calculator Standalone* and *Intel FPGA Power and Thermal Calculator User Guide*. • Updated the *Intel FPGA Power and Thermal Calculator*. • Updated the *SmartVID Standard Power Devices* section to include the –X power option. • Updated Table: *Supported Voltage Output Format for Intel Agilex Devices with the –V, –E, and –X Power Options*. • Updated the description of the slave device type and voltage output format parameters in Table: *Power Management and VID Parameters*. • Updated Figure: *Handshake between the External PMBus Master and FPGA in the PMBus Slave Mode Timing Diagram*. • Updated Figure: *External PMBus Master Software Flow*. • Removed VCCBAT from Table: *Voltage Rails Group*. • Removed the H-tile support.

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Document Version	Changes
2021.02.08	• Updated the topic about the voltage monitoring system to clarify about internal high-voltage rails. • Added VCCR_CORE (channel 5) to the figure showing the Intel Agilex voltage sensor. • Corrected the TSD location numbers for reading the temperatures of the HPS and SDM blocks. • Updated the footnotes to the table that lists the local temperature sensor locations to clarify that channel 0 returns the highest temperature in a location for any location that has more than one TSD. • Added the temperature sensor error codes. • Added the Temperature Reading design example section.
2020.11.11	Updated the footnote for V_{CCA_PLL} and V_{CCR_CORE} in Table: *Voltage Rails Group*.
2020.10.19	• Updated the SmartVID value and SmartVID programmed value terms to VID-fused value. • Added the *Power-Down Sequence Requirements for Intel Agilex Devices with E-Tile or H-Tile* section. • Updated the *Power-Up Sequence Requirements* section to include details about the power-down sequence for E-tile and H-tile devices. • Updated the *SDM Power Manager* section. • Updated the *PMBus Slave Mode* section. • Updated the *Temperature Compensation* section. • Updated Table: *Voltage Rails Group*. • Updated Table: *Power Management and VID Parameters* to update the description of the *Slave device type* and *Enable PAGE command* parameters. • Added Figure: *Handshake between the External PMBus Master and FPGA in the PMBus Slave Mode Timing Diagram*. • Added Figure: *Power-Down Sequence for Intel Agilex Devices with H-Tile*. • Added Figure: *Power-Down Sequence for Intel Agilex Devices with E-Tile*. • Updated Figure: *Temperature Compensation for SmartVID for Intel Agilex Devices*. • Removed note (2) from Figure: *External PMBus Master Software Flow*. • Updated *Example 1—Specifying the Power Management and VID Parameters through QSF Constraints*. • Updated the voltage monitor range to up to 1.10 V. • Updated the figure showing the voltage monitor 7-bit unipolar transfer function. • Updated the table that provides an overview of the local and remote temperature sensors. • Updated the topic about the local temperature sensors. • Updated the figures showing the TSD locations. • Updated the table listing the temperature sensor locations, channels, and remote TSD pin names. • Updated the topic about retrieving the local temperature sensor reading. • Added guidelines topic about calibrating the external temperature sensing chip. • Renamed "Mailbox Avalon ST Client Intel FPGA IP" to "Mailbox Client with Avalon Streaming Interface Intel FPGA IP".
2020.04.22	• Added the *Guidelines for I/O Pins in GPIO, HPS, and SDM Banks During Power Sequencing* section. • Added the F-tile and R-tile power rails in the *Voltage Rails Group* table. • Added V_{CCR_CORE} power supply to the *Power Supplies Monitored by the POR Circuitry* section. • Added the *Supported Voltage Output Format for Intel Agilex Devices with the –V and –E Power Options* table. • Updated the table that provides an overview of the local and remote temperature sensors to clarify that the local temperature sensor operates only in user mode. • Updated the topic about the temperature sensor channels and locations: — Updated the description from using "channels" to "locations". — Updated the diagram showing the sensor locations. — Updated the table listing the sensor locations and equivalent remote TSD pins. • Added topic about retrieving the local temperature sensor reading. • Updated the voltage monitor design guidelines to add VSIGP and VSIGN pins guideline. • Added the E-tile transceiver local temperature sensor design guidelines.

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Document Version	Changes
2020.02.06	• Updated the *PMBus Slave Mode* section. • Added $V_{CC\_HSSI\_GXE}$, $V_{CCRTPLL\_GXE}$, V_{CCR_CORE}, $V_{CCIO\_PIO\_SDM}$, and V_{CCBAT} power rails to the *Voltage Rails Group* table. • Removed $V_{CCRTPLL\_CR3\_GXE}$ and V_{CCM_WORD} power rails from the *Voltage Rails Group* table. • Removed the *Power Distribution* section.
2019.10.04	• Changed the Early Power Estimator (EPE) tool name to Intel FPGA Power and Thermal Calculator. • Added the *Intel Agilex Power Management and VID Interface QSF Constraint Guide* section. • Added ED8401, EM21XX, and EM22XX device selection in the slave device type parameters in the *Power Management and VID Parameters* table. • Updated the power optimization information in the *Intel Agilex Power Management Overview* section. • Updated the *Early Power Estimator (EPE)* section. • Updated the *Power Supplies Monitored by the POR Circuitry* section to remove the note on powering up V_{CCBAT} when not using the volatile key. • Updated the *SmartVID Standard Power Devices* section to update the voltage value for V_{CC} and V_{CCP} during power up. • Updated the V_{CCA_PLL} power rail from Group 2 to Group 3 in the *Voltage Rails Group* table. • Updated the *Stage Flow for the External Power Management Controller in the PMBus Slave Mode* figure. • Changed the voltage and temperature sensors IP support from Temperature Sensor and Voltage Sensor IPs to Mailbox Client and Mailbox Avalon ST IPs. • Updated the *Local Temperature Sensor* topic to add information about the catastrophic trip (nCATTRIP) signal. • Added reference to the *Intel Agilex Design Guideline Training: IBIS AMI Link Simulation, PDN, EMIF Layout Guidelines*. • Removed the *Power Dissipation and Thermal Considerations* section.
2019.04.02	Initial release.