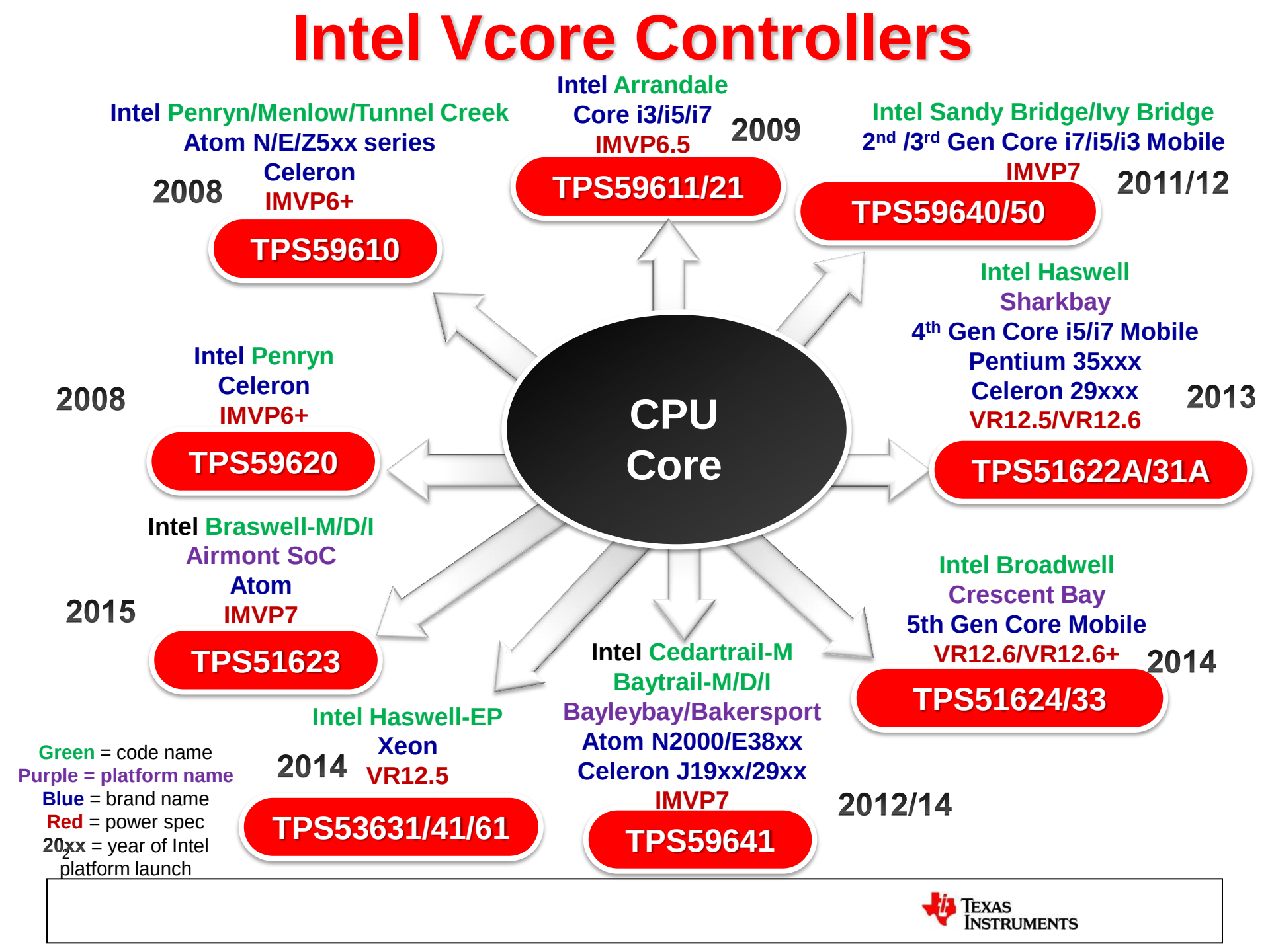
Intel Baytrail-I Atom E38xx Power Solutions

May 2016

Texas Instruments

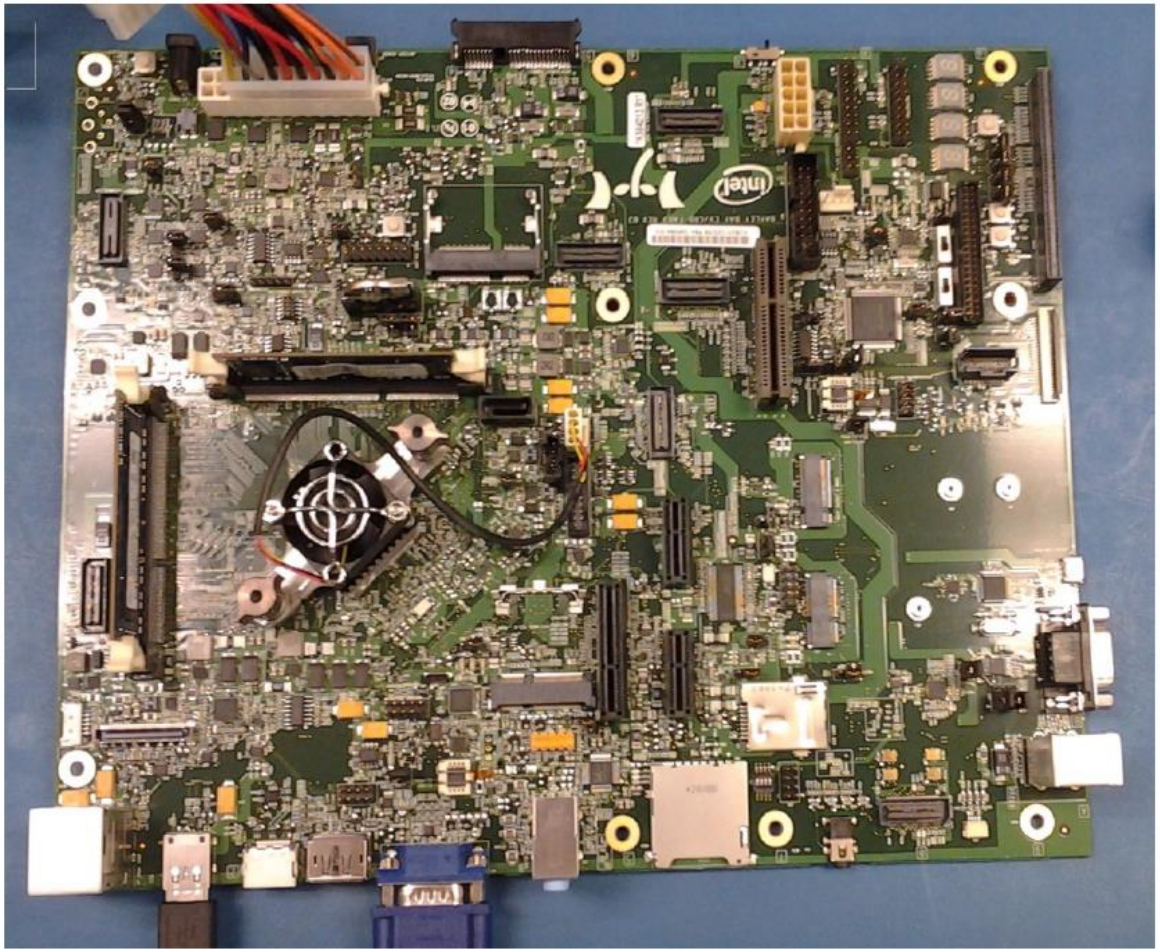
Intel Vcore Controllers



Intel's Bayley Bay-I CRB with TPS59641 and TI dc-dc power

TPS59641 + TPS51604 + CSD86330 x2 for Vcore
Can use TPS59641 + TPS51604 + CSD87381P x 2 (TI reference design)

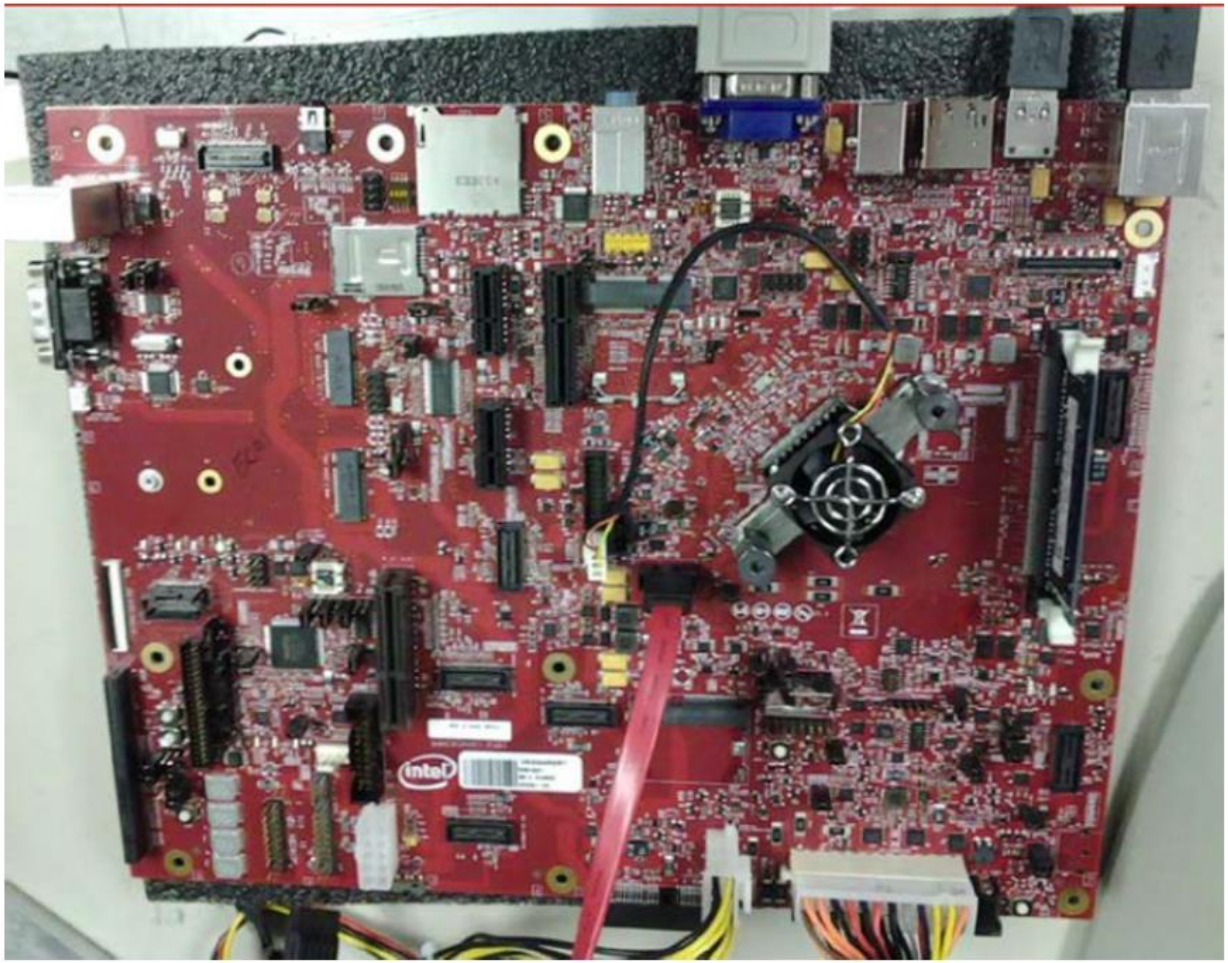
Bayley Bay-I - Board



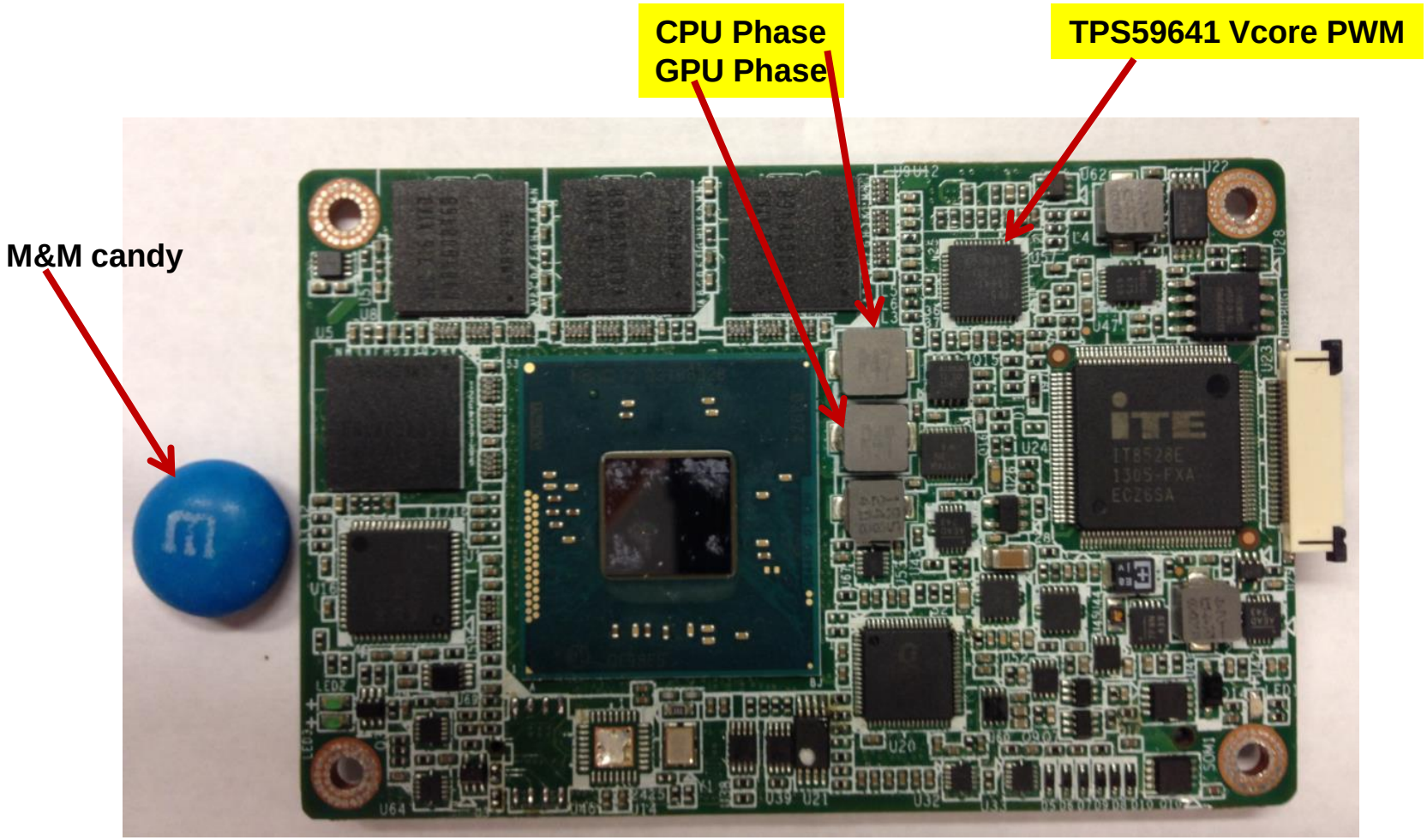
Intel's Bakersport CRB with TPS59641 and TI dc-dc power

TPS59641 + TPS51604 + CSD86330 x2 for Vcore
Can use TPS59641 + TPS51604 + CSD87381P x 2 (TI reference design)

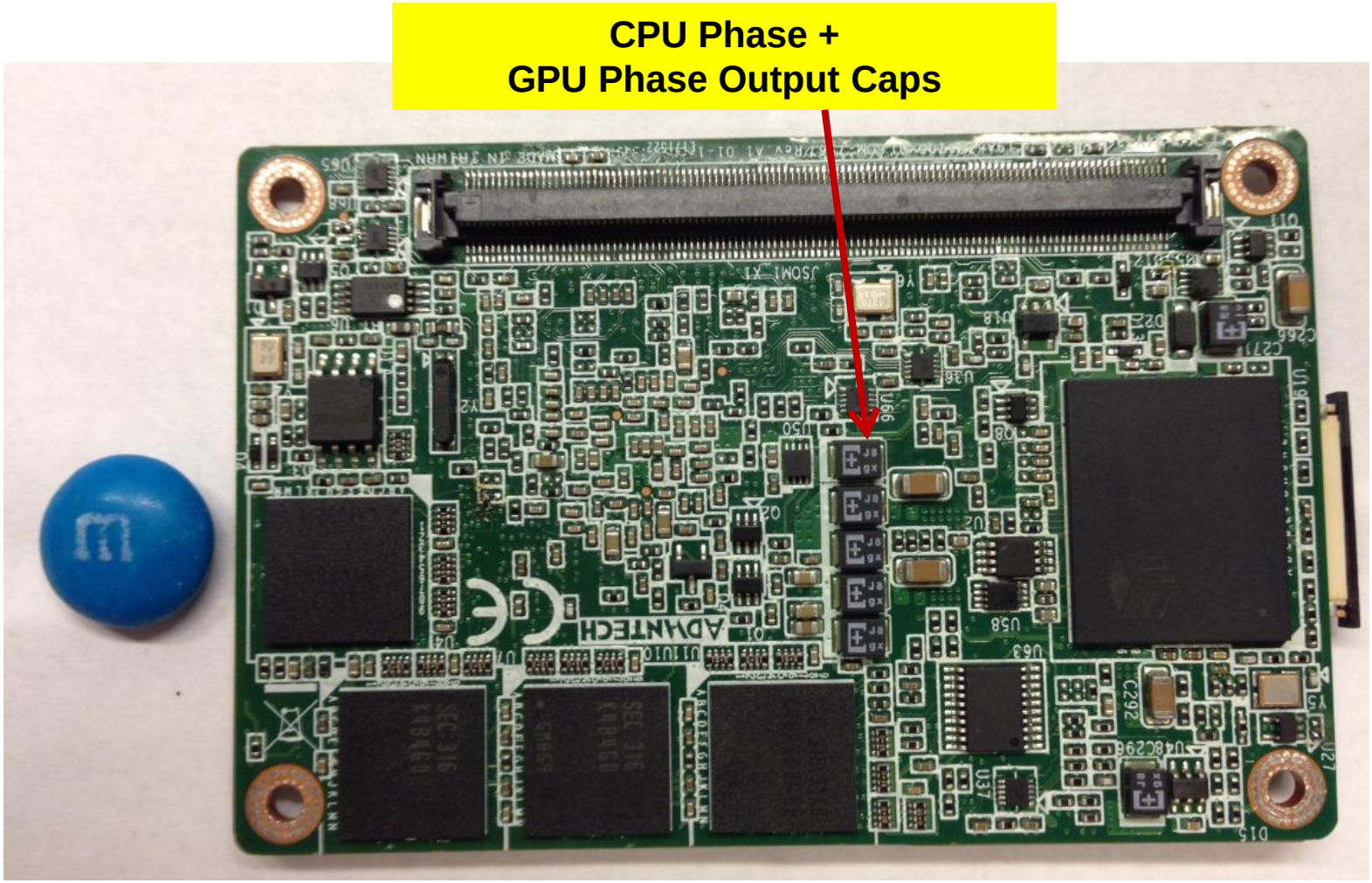
Bakersport - Board



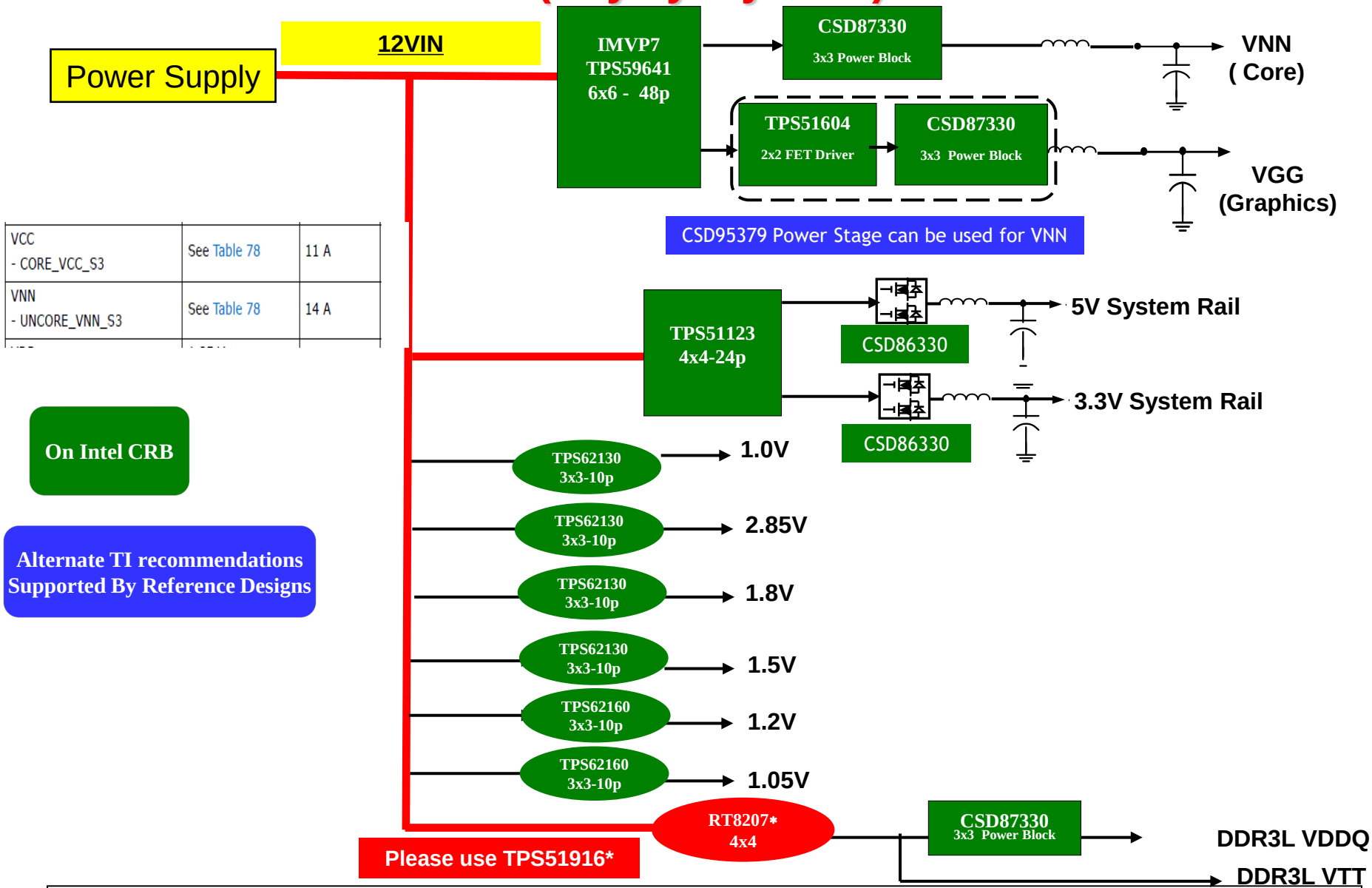
TPS59641 powering VR12.1 Baytrail-I CPU in a COM Express Module (55mm x 84mm)



TPS59641 powering VR12.1 Baytrail-I CPU in a COM Express Module – discrete solution fits in 55mm x 84mm module



Baytrail-I Embedded PC Solution (dual core) – 1-stage conversion (Bayleybay CRB)

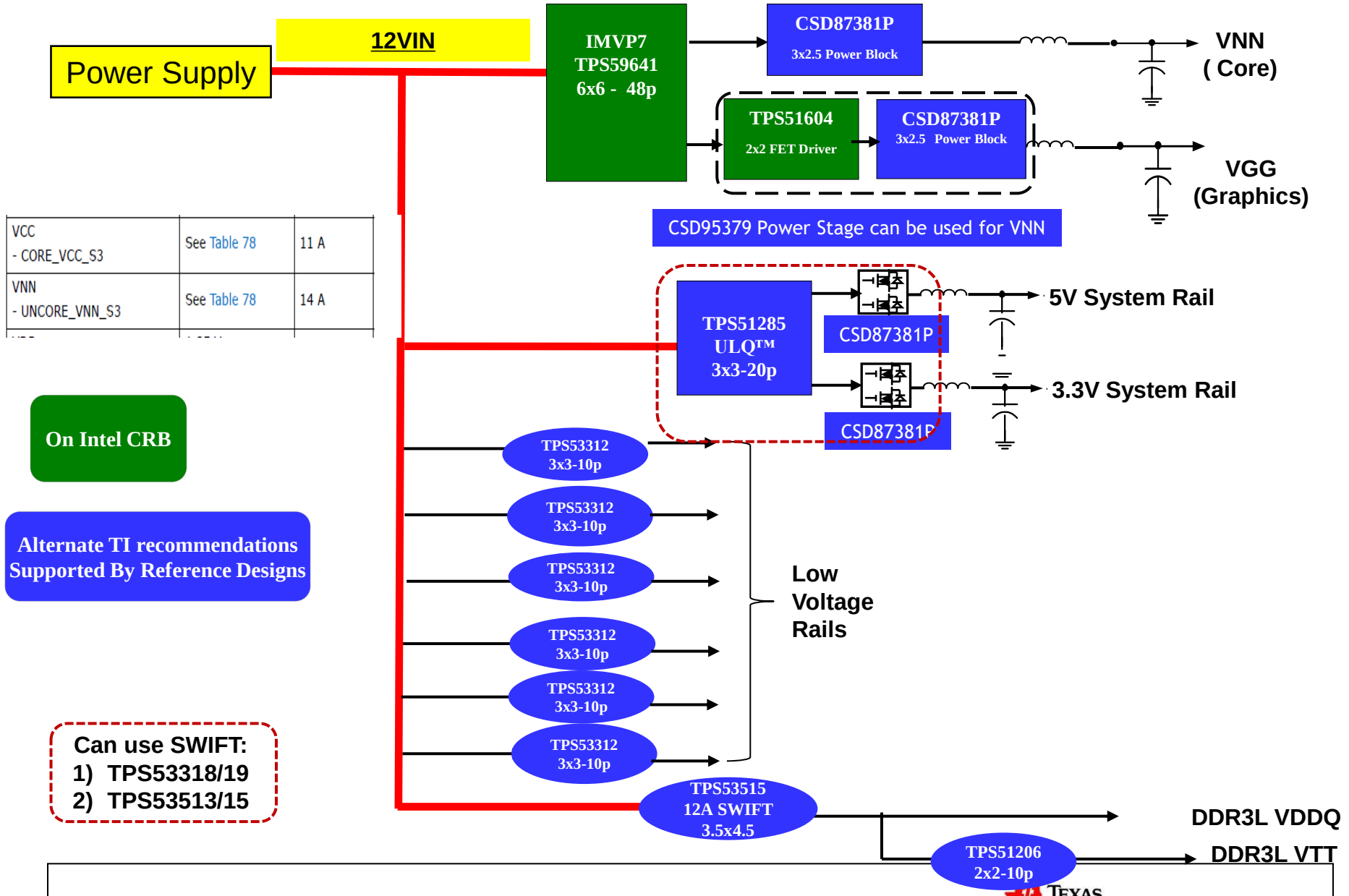


VCC - CORE_VCC_S3	See Table 78	11 A
VNN - UNCORE_VNN_S3	See Table 78	14 A

On Intel CRB

Alternate TI recommendations Supported By Reference Designs

Baytrail-I Embedded PC Solution (dual core) – 1-stage conversion



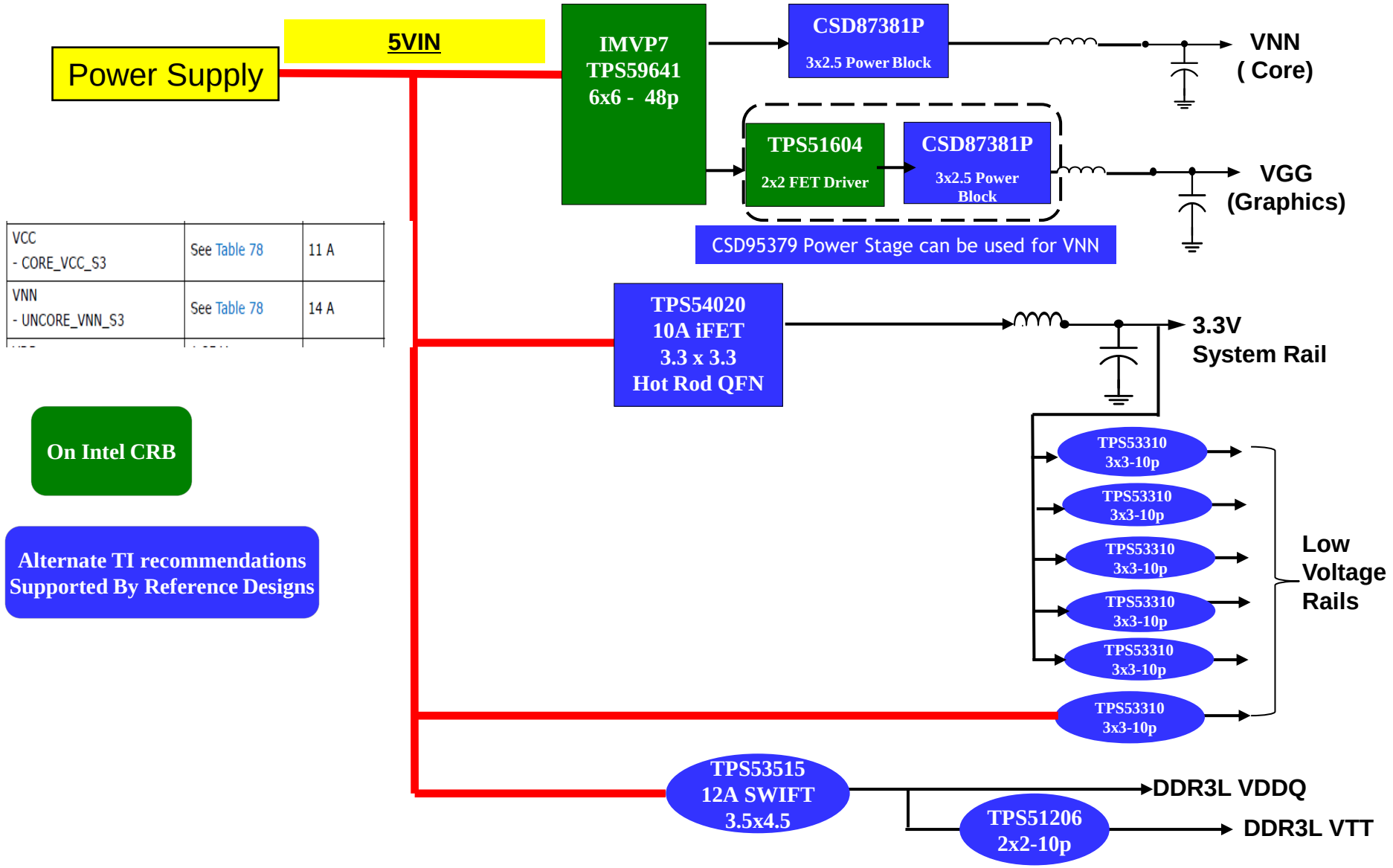
VCC - CORE_VCC_S3	See Table 78	11 A
VNN - UNCORE_VNN_S3	See Table 78	14 A

On Intel CRB

Alternate TI recommendations Supported By Reference Designs

Can use SWIFT:
1) TPS53318/19
2) TPS53513/15

Baytrail-I Embedded PC Solution (dual core) – 2-stage conversion



TPS59641
3V to 28V, 3+1-phase Step-Down PWM Controller for Intel Baytrail-M/D/I CPU

Features

- Input Voltage Range 3V to 28V
- IMVP7 SVID with VR12.1 VBOOT
- 2 integrated MOSFET drivers for CPU Core
- D-CAP+™ mode Architecture
- AutoBalance™ Phase-to-Phase Current Sharing
- Auto-Zero Comparator and Eco Mode™ operation
- V_{CORE} OSR™ Over Shoot Reduction
- All PWM Outputs can be configured as Driverless
- V_{CORE} USR™ Under Shoot Reduction
- 48L 6x6 QFN Package w/1mm Height

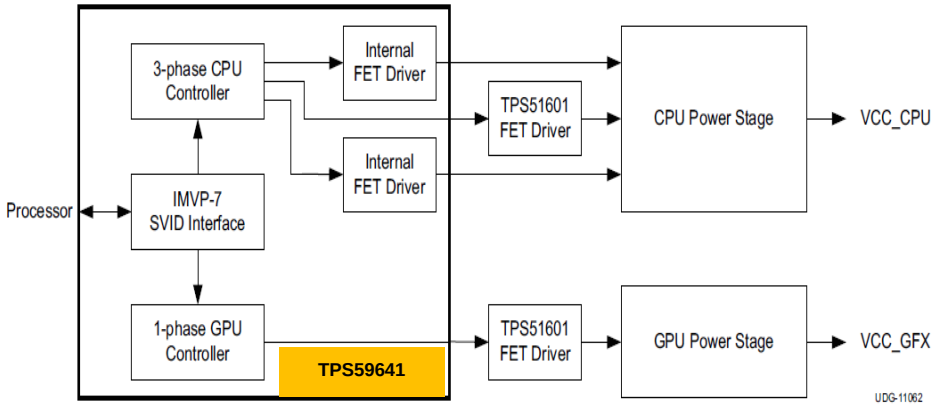
Benefits

- Conversion from 1-Cell Battery to AC/DC Adapter
- Fully Compliant to Baytrail CPU specification
- Lower noise vs. competition with 3 integr. drivers
- >70% smaller Vout deviation vs. CM
- 95% phase-to-phase current balance for high-rel
- Accurate Light Load Detection and High Efficiency Reduced Output Caps, Lower System Cost
- Use CSD97374 Power Stage for 3-chip 1+1 design
- Reduced Output Caps, Lower System Cost
- High power density, excellent thermal performance

Applications

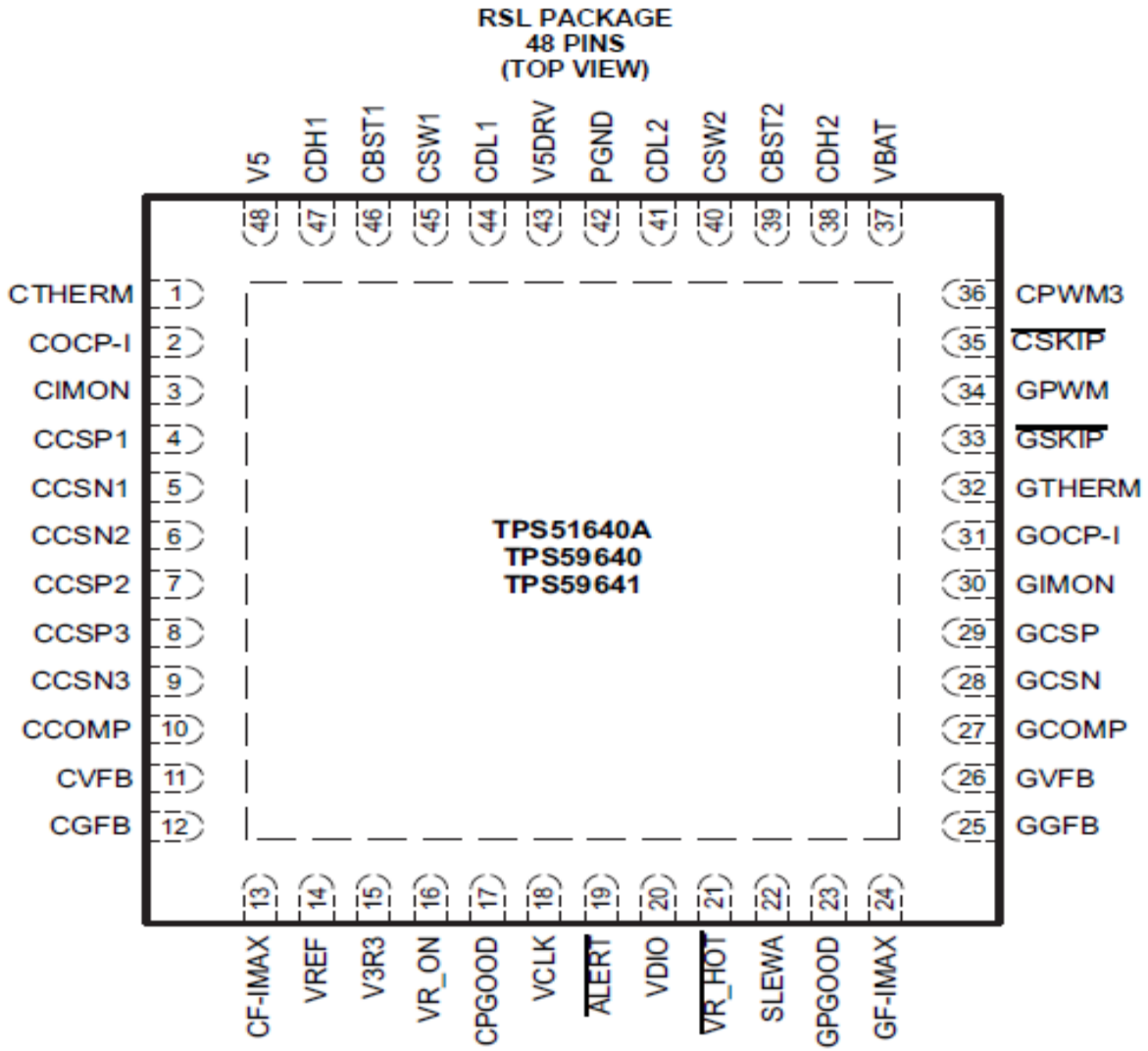
Intel Baytrail-M/D/I CPU Core Power

- Notebook Computers
- Desktop
- Tablet Computers
- Embedded Computers
- Aftermarket Car Infotainment



Texas Instruments

TPS59641 Pin Diagram



BAYTRAIL-I POWER SPECIFICATIONS

Conditions	VCC Rail (Core) CPU Spec	VNN Rail (Uncore) GPU Spec
Number of Phases	1	1
Input Voltage Range	5V-20V	5V-20V
VCC VID Max	1.0V	1.05V
VBOOT	1.0V or 1.1V	1.0V or 1.1V
Icc Max	9A	10A
Icc Dyn	7A	8A
Icc-Tdc	4A	7A
Load Line	5.9mOhm	5.9mOhm
Fast Slew rate	10mV/us	10mV/us

BAYTRAIL-I POWER SPECIFICATIONS (Intel EDS, DOC#538136

Table 65. VCC and VNN Currents

SKU	VCC Icc Max	VNN Icc Max
E3845	9	10
E3827	4	10
E3826	4	10
E3825	4	9
E3815	2	8

9.3.1 VCC and VNN Voltage Specifications

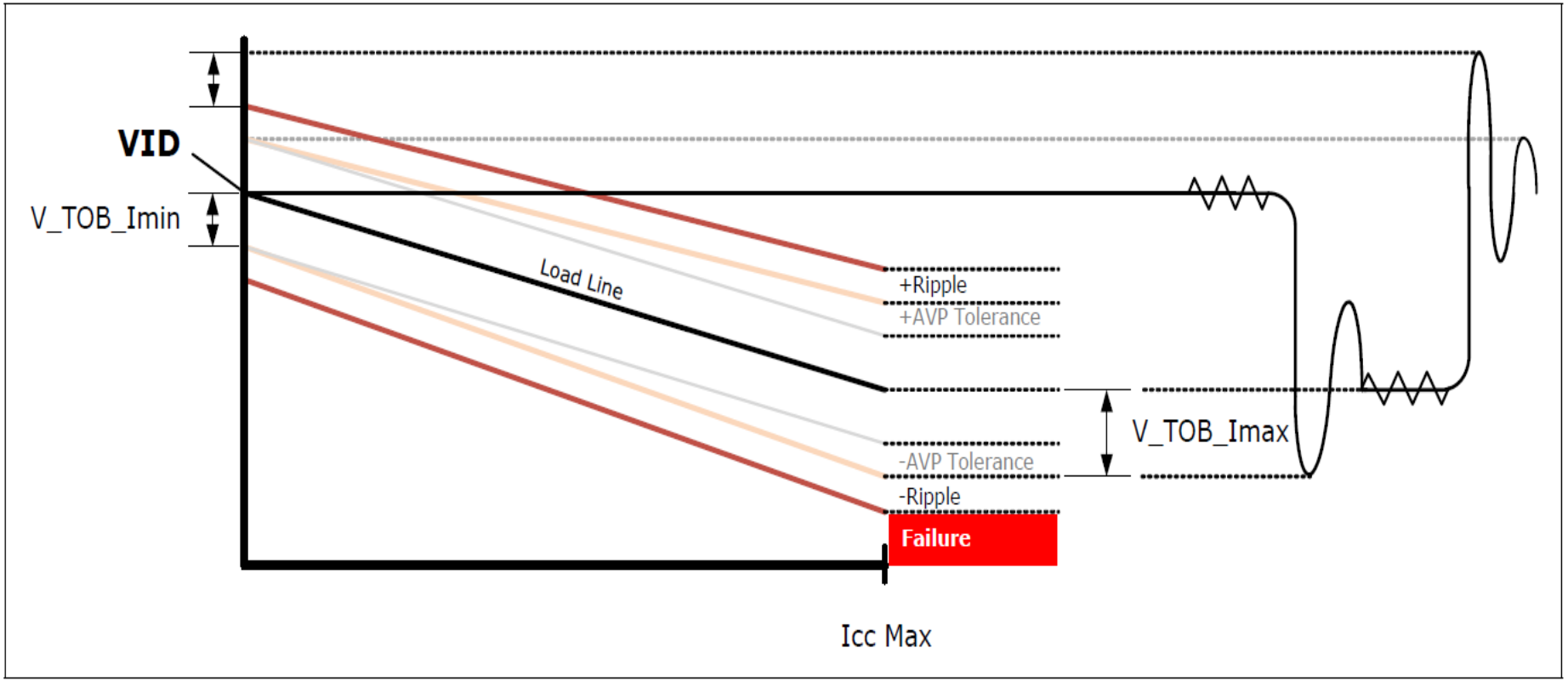
Table 66 and Table 82 list the DC specifications for the SoC power rails. They are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Care should be taken to read all notes associated with each parameter.

Table 66. VCC and VNN DC Voltage Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Note
CORE_VCC VID	Core VID Target Range	0.40		1.0	V	
CORE_VCC_S3	V_{CC} for SoC Core	See VCC VID			V	2, 5
UNCORE_VNN VID	Uncore VID Target Range	0.50		1.05	V	
UNCORE_VNN_S3	V_{NN} for SoC Uncore	See VNN VID			V	2, 5
CORE_VCC/ UNCORE_VNN V_{BOOT}	Default target V_{CC}/V_{NN} voltage for initial power up.		1.0 or 1.1		V	4
$SLOPE_{LL}$	Processor Core Supply DC Loadline		-5.9		mΩ	Figure 15

BAYTRAIL-I LOADLINE

Figure 15. CORE_VCC_S3 and UNCORE_VCC_S3 SoC Loadline



CPU POWER SPEC TESTING

Enter the name of the voltage rail being tested		CORE	
Normal Operating Mode			
Voltage Rail Parameters from Table in Design Guide	**Variables**	**Values**	**Units**
Loadline	R_DC_LL	5.9	mΩ
	R_AC_LL_MAX	8.0	mΩ
Test VID in Turbo Mode	VID1	1.15	V
Test VID in Low Frequency Mode	VID2	0.7	V
V_TOB_IMAX of a VID in PS0. It may be a % determined by the VID like 1.0 or 1.5, or fixed value in mV, like 16mV.	V_TOB_IMAX in PS0	17.0	mV
TOB in PS2	V_TOB_Imax_PS2	8.0	mV
Peak +/- Ripple in PS0 below TDC	PS0 Ripple	10	mV peak
Peak +/- Ripple in PS0 at currents above TDC+30% (may be the same as below TDC)	PS0_TDP Ripple	10	mV peak
+ Ripple in PS2	+ PS2 Ripple	15	mV peak
-Ripple in PS2	- PS2 Ripple	10	mV peak
Thermal Design Current	I_TDC	5	A
Max Current for the rail	IccMax	8	A
Dynamic step size in of VID1 in PS0	Icc_Dyn_VID1	7	A
Maximum Overshoot Above VID	VOvS_MAX	50	mV
Maximum Overshoot Time Above VID	tOvS_MAX	25	µs

VR Design Dependant Test Parameters	**Variables**	**Values**	**Units**
V_TOB_IMin for VID of 1.15 volts	V_TOB_Imin_VID1	5.75	mV
V_TOB_IMin for VID of 0.7 volts	V_TOB_Imin_VID2	8	mV
V_VR_TOB_IMax for VID of 1.15 volts	V_VR_TOB_Istep_VID1	17	mV
VID1 Efficiency Target at TDC	Eff	85%	%

Typical Test Parameters	**Variables**	**Values**	**Units**
Max Dynamic Current in PS0	IccMax_PS0	8	A
Max Dynamic Current in PS2	IccMax_PS2	0	A
TOB at ICCMax VID of 1.15 in PS0	V_TOB_Imax	17	mV
Transient Slew Time	didt	200	ns
dVID Settling Time	dVID_Settle	5	µs
SetVID_Fast Value is either 10mV/us or 20mV/us. Verify in VR controller datasheet	SetVID_FAST	10	mV/us

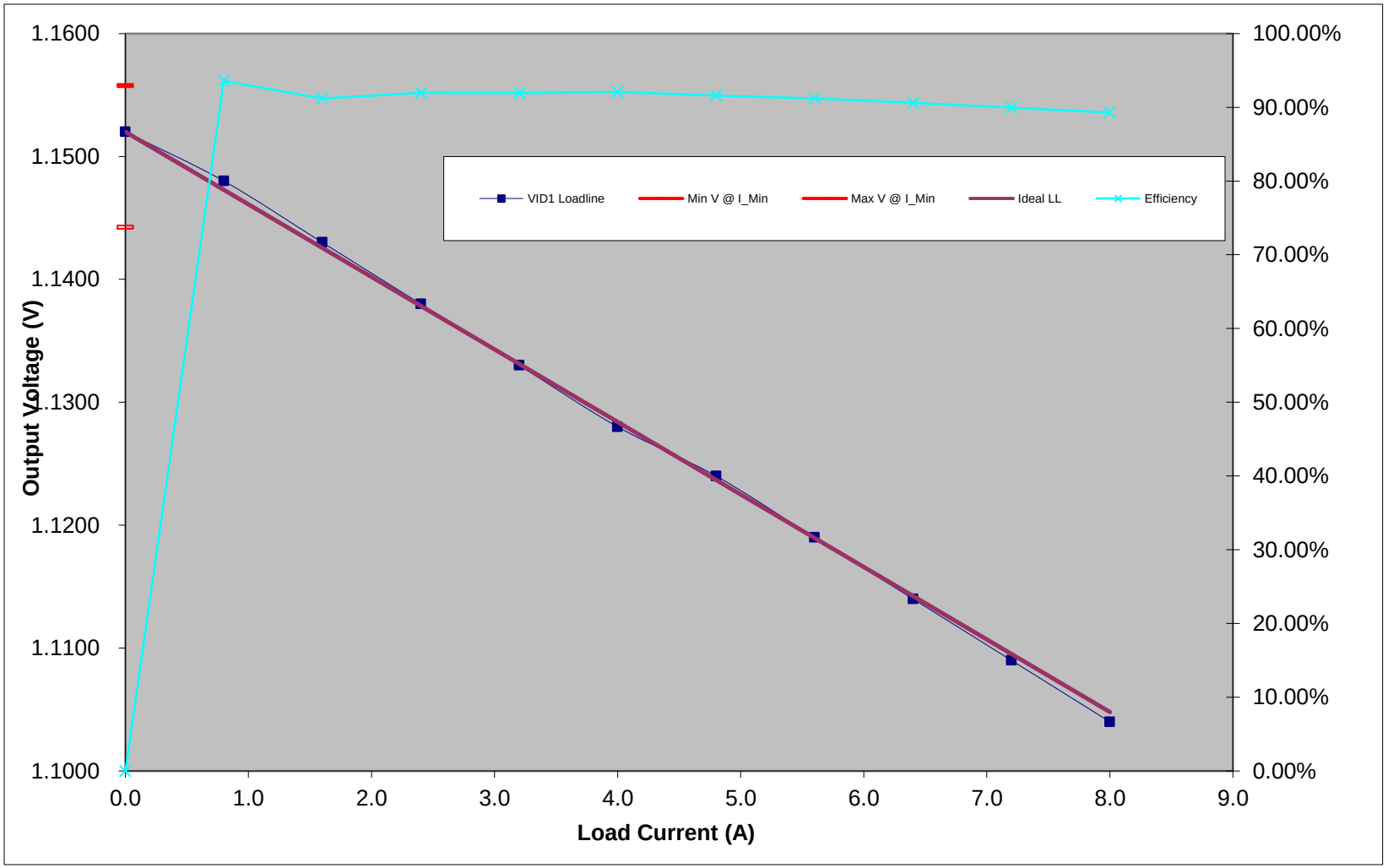
GPU POWER SPEC TESTING

Enter the name of the voltage rail being tested		GFX	
Normal Operating Mode			
Voltage Rail Parameters from Table in Design Guide	**Variables**	**Values**	**Units**
Loadline	R_DC_LL	5.9	mΩ
	R_AC_LL_MAX	5.9	mΩ
Test VID in Turbo Mode	VID1	1.05	V
Test VID in Low Frequency Mode and PS2	VID2	0.7	V
V_TOB_IMAX of a VID in PS0. It may be a % determined by the VID like 1.0 or 1.5, or fixed value in mV, like 16mV.	V_TOB_IMAX in PS0	15.0	mV
TOB in PS2	V_TOB_Imax_PS2	8.0	mV
Peak +/- Ripple in PS0 below TDC	PS0 Ripple	10	mV peak
Peak +/- Ripple in PS0 at currents above TDC+30% (may be the same as below TDC)	PS0_TDP Ripple	10	mV peak
+ Ripple in PS2	+ PS2 Ripple	15	mV peak
-Ripple in PS2	- PS2 Ripple	10	mV peak
Thermal Design Current	I_TDC	7	A
Max Current for the rail	IccMax	14	A
Dynamic step size in of VID1 in PS0	Icc_Dyn_VID1	3	A
Maximum Overshoot Above VID	VOvS_MAX	50	mV
Maximum Overshoot Time Above VID	tOvS_MAX	25	µs

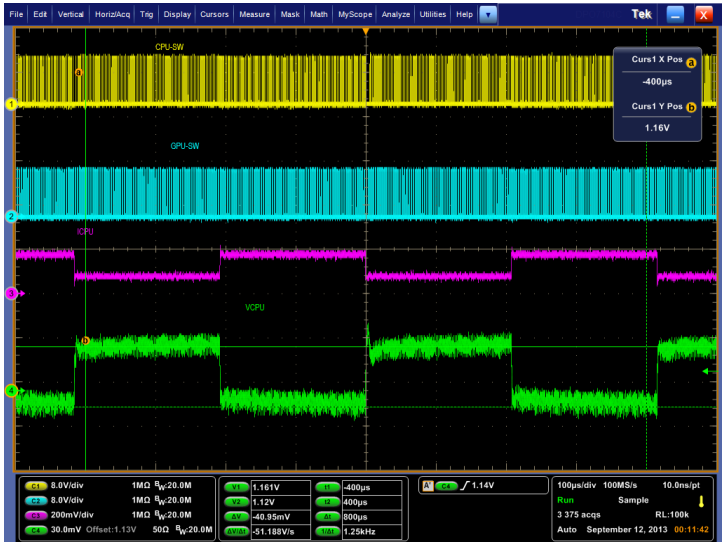
VR Design Dependant Test Parameters	**Variables**	**Values**	**Units**
V_TOB_IMin for VID of 1.05 volts	V_TOB_Imin_VID1	5.25	mV
V_TOB_IMin for VID of 0.7 volts	V_TOB_Imin_VID2	8	mV
V_VR_TOB_IMax for VID of 1.05 volts	V_VR_TOB_Istep_VID1	15	mV
VID1 Efficiency Target at TDC	Eff	85%	%

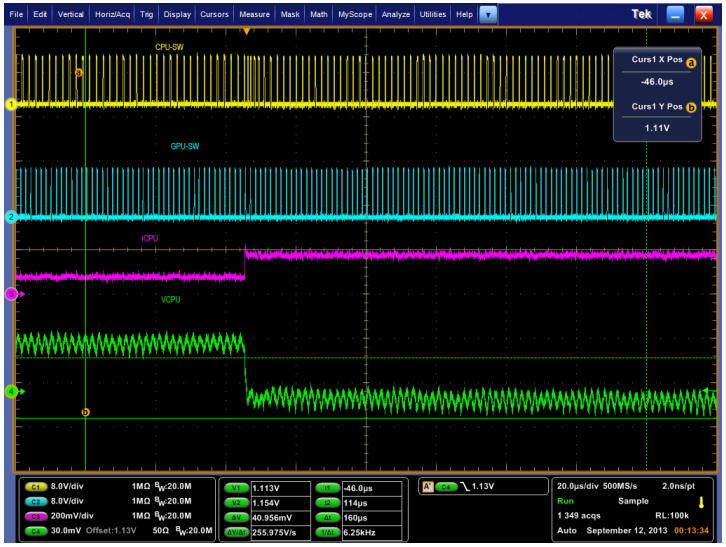
Typical Test Parameters	**Variables**	**Values**	**Units**
Max Dynamic Current in PS0	IccMax_PS0	7	A
Max Dynamic Current in PS2	IccMax_PS2	0	A
TOB at ICCMax VID of 1.05 in PS0	V_TOB_Imax	15	mV
Transient Slew Time	didt	200	ns
dVID Settling Time	dVID_Settle	5	µs
SetVID_Fast Value is either 10mV/us or 20mV/us. Verify in VR controller datasheet	SetVID_FAST	10	mV/us

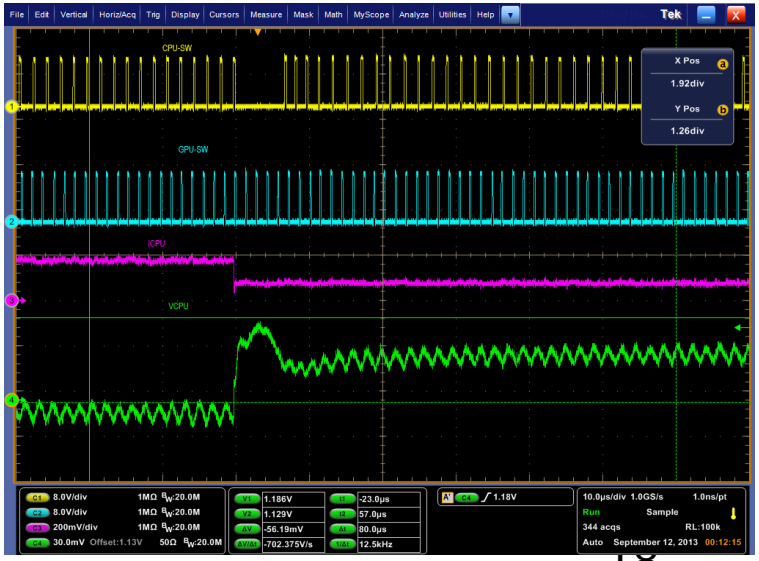
Efficiency and load line



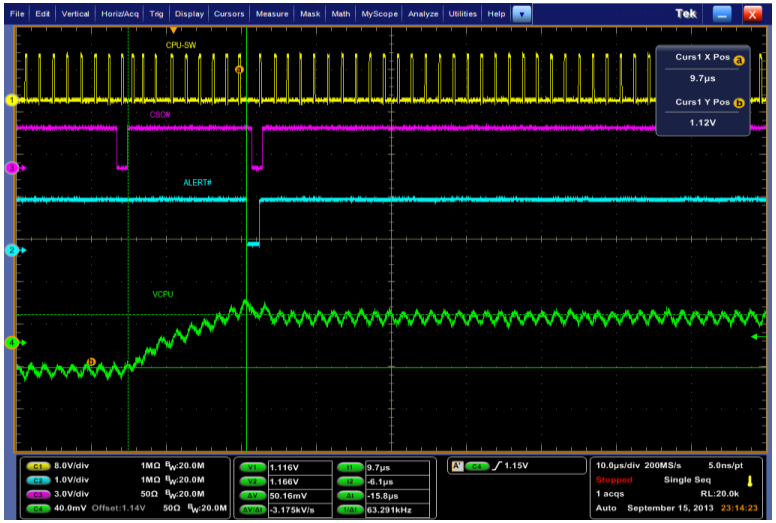
Load transient (PS0 -1A to 8A, 8A to 1A)

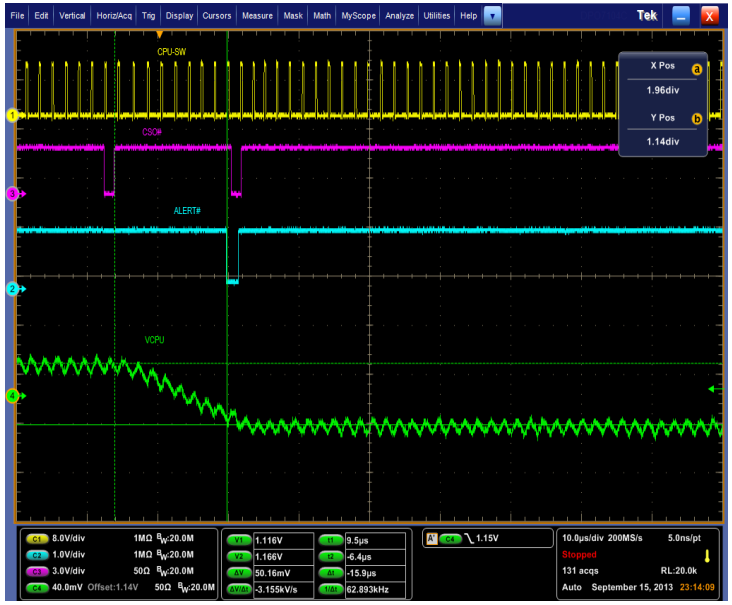






Dynamic VID in PS0





TPS59641 Design Calculator Tool

TPS59641(VR12.1 CPU and GPU Vcore) Design Procedure with DCR Sensing Temperature Compensation — GLMJR36 01A

Example: Baytrail-M CPU

INSTRUCTIONS

1. When you open this file Click on 'Enable Macros' when the prompt appears
2. This Program has a Macro to calculate an optimized set of DCR sense component values.
3. You need the Excel Add-in "Solver" to use this Program. Go to Tools -> Add-in. Check the box "Solver" and "Analysis Tool-pak'
4. Enter the parameters in Green Cells
5. DO NOT CHANGE ANY CELLS OTHER THAN GREEN CELLS
6. The Program automatically selects the TRIPSEL selection
7. Run the Macro (By pressing CTRL+q) for correct DCR sense values. The DCR sense and some of the results will update only after running the macro.
8. Use the 'PASS' / 'FAIL' criteria as a guideline only. Judgement should be made based on actual numbers.
9. When you get an 'ERROR!' in the results, the input parameters must be adjusted to get a correct result.
10. The Bode Plot at the end is based on Linearized model and is valid only << switching frequency.

If it is okay to switch the CPU at 450Khz, then for CPU NVDD you need only 4 ceramic

Enter the parameters in Green Cells

DO NOT CHANGE any other cells

Processor Requirements

	CPU	GFX	
Number of phases	1	1	
VID_Vcore_HFM (0 A)	0.9000	1.2800	V
R_Loadline	5.9	5.9	mV/A
Maximum Current (Icc_max)	8	7	A
Per phase Maximum Current	8.0	7.0	A
Thermal Design Current (LTDC_total)	4	3	A
Per phase Thermal Design Current	4.0	3.0	A
SetVID Fast Slew Rate (Typical)	12		mV/µs
Load Current for Bode Plot	8	10	A

System Requirements

Vin max	20		V
Vin_min	5		V
Freq	450	660	kHz

Inductor

Minimum Recommended Inductance	0.60	0.65	µH	
Maximum Recommended Inductance	1.13	1.30	µH	DO NOT CHANGE
Chosen Inductance, L	0.68	0.56	µH	PASS
Inductor DCR, L_DCR	4.200	3.400	mΩ	PASS

Bulk Capacitor

Output Capacitor, Bulk	330	330	µF
ESR of Bulk Output capacitor	6.0	6.0	mΩ
Total No. of Output Capacitors	2	1	
ESL of Bulk Capacitor	1	1	nH

DCR power loss

Max. allowed DCR power loss	0.11	0.08	W	DO NOT CHANGE
DCR Power loss (TDC)	0.09	0.04	W	

DCR Temperature Compensation

B value of DCR thermal compensation NTC	4250	4250	K	
Resistance of NTC at 25C	100	100	kΩ	
TCR_cu	0.0039		ppm/C	DO NOT CHANGE

Over Current Limit (TRIPSEL)

Min. Over Current Limit (OCL) Target	12	12	A

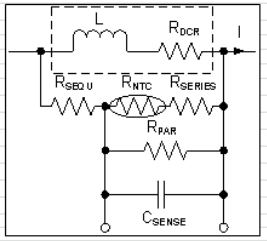
RUN MACRO (CTRL+q) for Correct DCR sense values

CPU

Rcsqu	17.15	kΩ
Rcseries	28.81	kΩ
Rpar	165.77	kΩ
Csense	11.57	nF
Divider Ratio	0.809	If Divide Ratio is lower than 0.75, try increasing OCL and run macro again.
TEMP COMPENSATI	PASS	

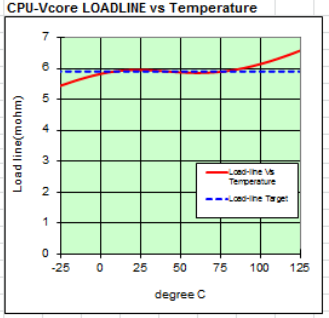
GFX

Rcsqu	17.36	kΩ
Rcseries	28.81	kΩ
Rpar	164.73	kΩ
Csense	11.77	nF
Divider Ratio	0.800	If Divide Ratio is lower than 0.75, try increasing OCL and run macro again.
TEMP COMPENSATI	PASS	

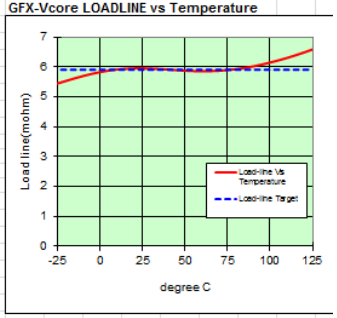


Pin 1 (CTHERM)to GND	100	kΩ	NTC for VR_HOT flag and Thermal Shutdown.
Pin 1 (CTHERM) to VREF	15.68	kΩ	Sets the IMVP Thermal Shutdown Level for CPU-Vcore
Pin 2 (COCP-I) to GND	100	kΩ	Selects the OCP level for CPU-Vcore
Pin 3 (CIMON) to COCP-I	4.21	kΩ	Sets IMON voltage for CPU-Vcore on CIMON pin
Pin 3 (CIMON) to GND	0.22	µF	CIMON Filter cap recommended
b			Sns DCR sensing for CPU
Pin 10 (CCOMP) to VREF	13.82	kΩ	Sets the DROOP for CPU-Vcore
Pin 11, Pin 12			Voltage sense Feedback, CPU
Pin 13 (CF-IMAX) to GND	56	kΩ	Selects the Frequency for CPU-Vcore
Pin 13 (CF-IMAX) to VRE	1723.0	kΩ	Sets the Icc_max for CPU-Vcore
Pin 14 (VREF) to GND	0.33	µF	VREF to Analog Ground By-pass capacitor
Pin 15 (V3R3V) to GND	1	µF	3.3V supply by-pass capacitor
Pin 16			VR_ON logic
Pin 17, Pin 23			CPGOOD and GPGOOD need external pull-up
Pin 18-Pin 21			SVID lines. Pull-up per Intel Spec
Pin 22 (SLEWA) to GND	150	kΩ	DO NOT CHANGE THIS VALUE at present
Pin 22 (SLEWA) to VREF	169	kΩ	This resistor sets the SLEW rate
Pin 24 (GF-IMAX) to GND	150	kΩ	Selects the Frequency for GFX-Vcore
Pin 24 (GF-IMAX) to VRE	5314.3	kΩ	Sets the Icc_max for GFX-Vcore
Pin 25, Pin 26			Voltage sense Feedback, GFX
Pin 27 (GCOMP to VREF)	11.06	kΩ	Sets the DROOP for GFX-Vcore
Pin 28, Pin 29 (GCSP-N)			Sns DCR sensing for GFX
Pin 30 (GIMON) to GND	0.22	µF	GIMON Filter cap recommended
Pin 30 (GIMON) to GOCP-	483	kΩ	Sets IMON voltage for GFX-Vcore on GIMON pin
Pin 31 (GOCP-I)	75	kΩ	Selects the OCP level for GFX-Vcore
Pin 32 (GTHERM) to GND	100	kΩ	NTC for VR_HOT flag and Thermal Shutdown.
Pin 32 (GTHERM) to VRE	15.68	kΩ	Sets the IMVP Thermal Shutdown Level for GFX-Vcore
Pin 33 (GSKIP) to GND	>=150	kΩ	Resistor to GND sets OSR/USR level
Pin 33 (GSKIP) to VREF	open	kΩ	Program this resistor to turn OSR off
Pin 34, 36 (GPWM, CPWM3)			PWM outputs.
Pin 35 (CSKIP) to GND	>=150		Resistor to GND sets OSR/USR level
Pin 35 (CSKIP) to VREF	open	kΩ	Program this resistor to turn OSR off
Pin 38-48			Gate-drive outputs
Pin 37	10	kΩ	Optional Resistor from Input voltage to VBAT pin
Pin 48 (V5) to 5VDRV	10	ohm	External Filter Resistor for 5V Analog Supply voltage
Pin 10 (CCOMP) to VREF	100	pF	Noise Filter at CCOMP-VREF (CPU-Vcore)
Pin 27 (GCOMP to VREF)	100	pF	Noise Filter at GCOMP-VREF (GFX-Vcore)
Pin 43 (V5DRV) to GND	4.7	µF	5V Driver Supply By-pass cap
Pin 48 (V5) to GND	2.2	µF	V5 to Analog Ground by-pass cap

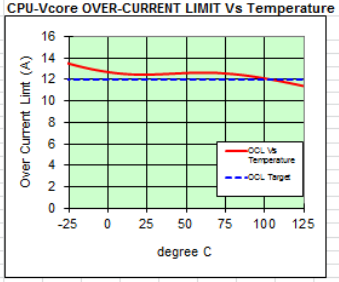
CPU-Vcore LOADLINE vs Temperature



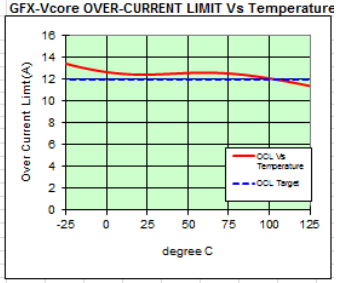
GFX-Vcore LOADLINE vs Temperature



CPU-Vcore OVER-CURRENT LIMIT Vs Temperature



GFX-Vcore OVER-CURRENT LIMIT Vs Temperature

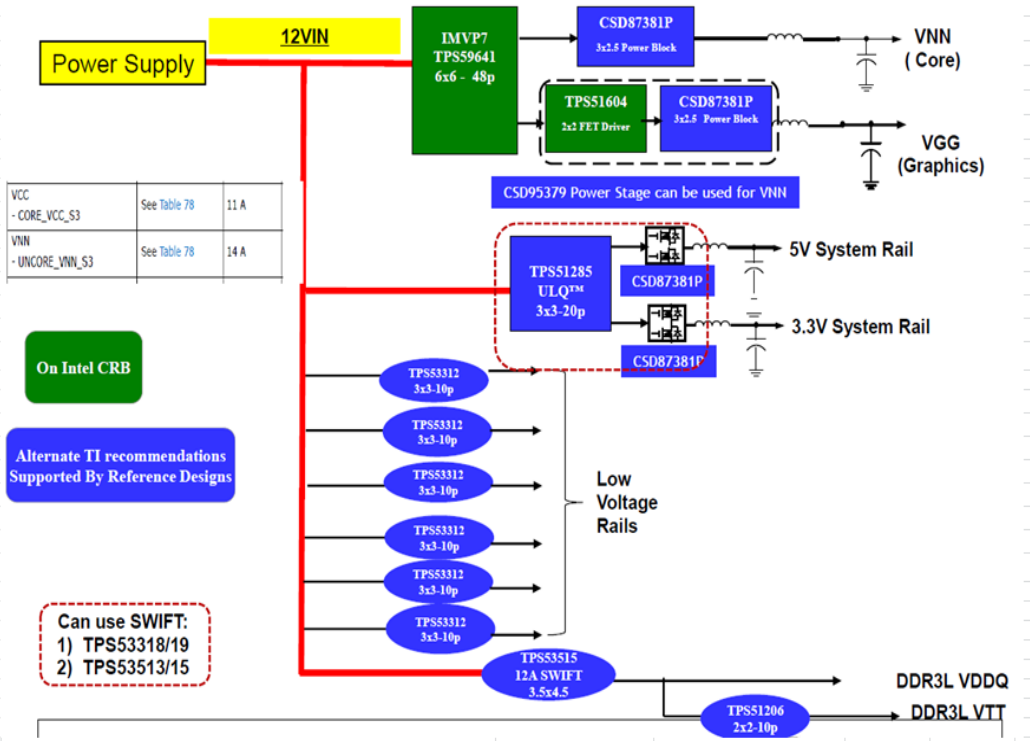


- ***Enables you to plug in your own design specifications and obtain component values, and the estimated loadline (voltage regulation) and current limit variation over temperature***

TPS59641 CPU and GPU core PCB area and BOM cost (MU+ component pricing)

12VIn Baytrail-I Discrete VR Solution w/TPS51285 and CSD87381P		
	Cost	Area mm^2
Vcore (VR12.1) - TPS59641 + TPS51604 + CSD87381P x 2	$0.66	288
5V and 3.3V - TPS51285 + CSD87381P x 2	$0.46	300
DDR3L VDDQ and VTT - TPS53515 + TPS51206	$0.36	280
Low Voltage Rails (x6 total) - TPS53312	$0.65	424
Total	**$2.13**	**1,292**

Baytrail-I Embedded PC Solution (dual core) – 1-stage conversion



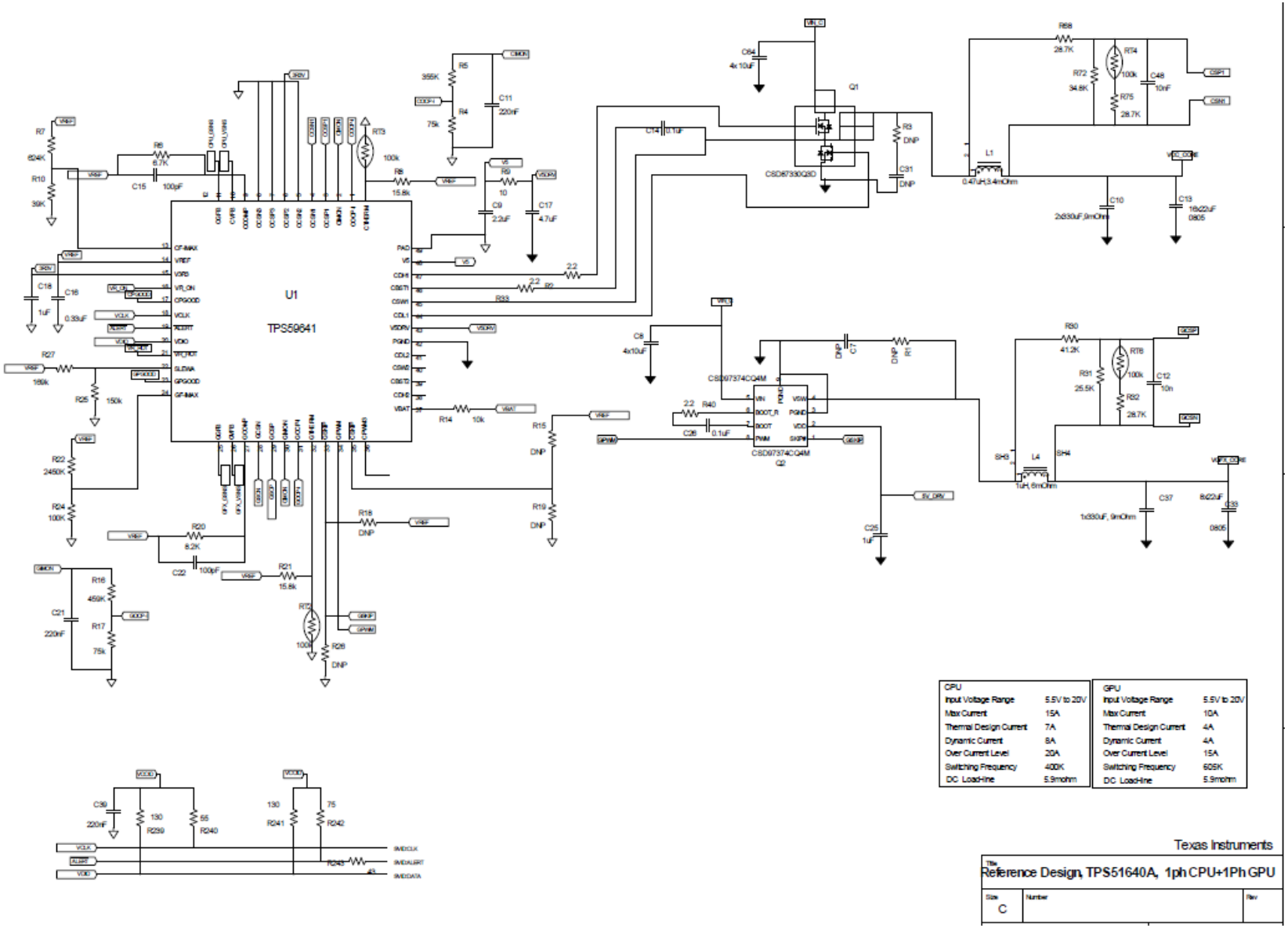
Baytrail-I Vcore BOM and PCB Area - TPS59641 + TPS51604 + CSD87381P x2

VR12.1 1+1-phase
TDC (CPU) = 7A, VNN (GPU) = 4A,
ImaxCPU = 15A, ImaxGPU = 10A
Idyn = 8A/8A,
VBOOT = 1.1V
DC Loadline = -5.9mOhm
VIN = 20V

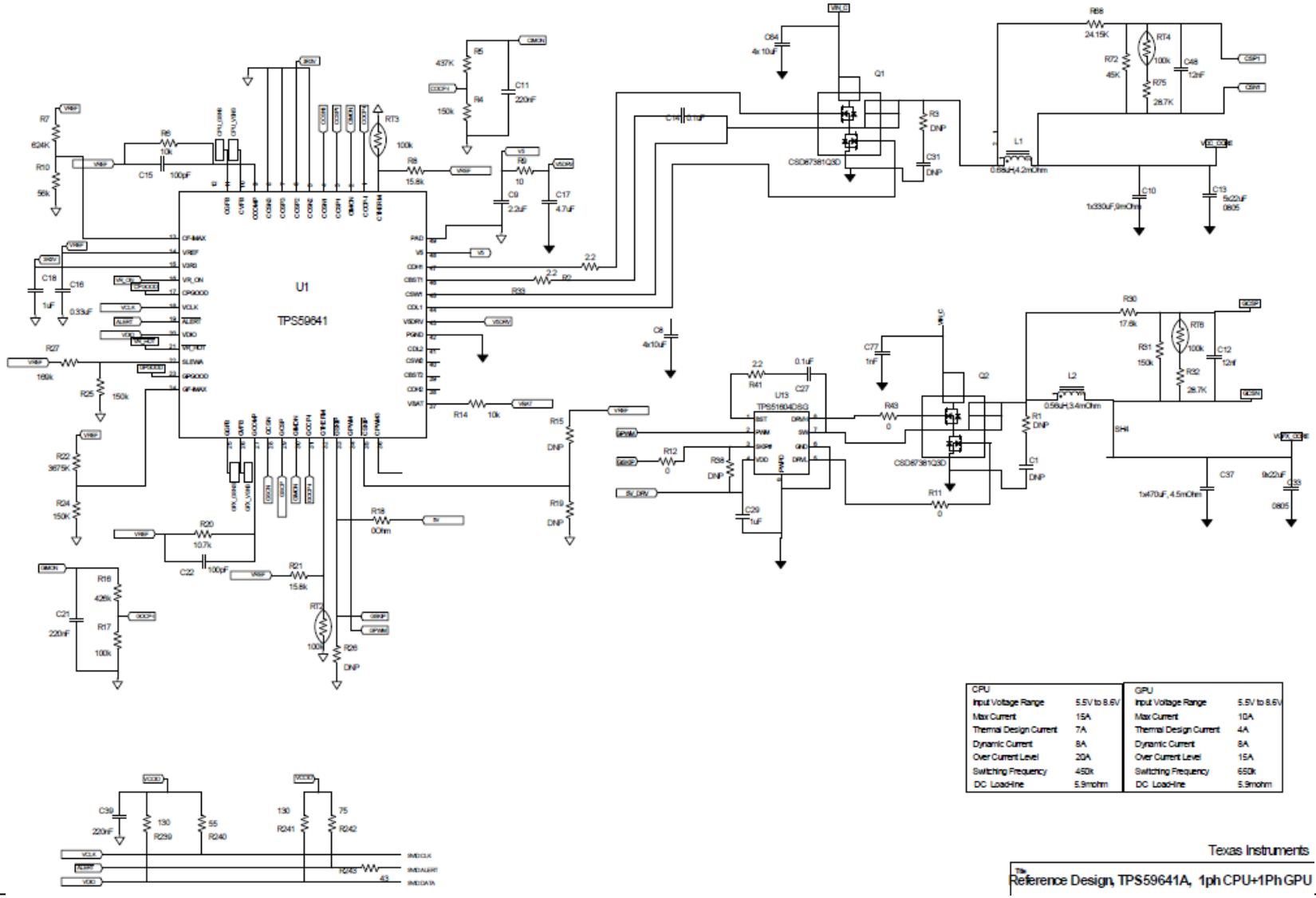
450KHz/650KHz
TPS59641 + TPS51604
CSD87381P/450KHz/0.68uH for CPU
CSD87381P/650KHz/0.56uH for GPU

	Component area (mm2)	Total Area (mm2)	AUP	Qty	Cost
Controller - TPS59641	36	36		1	$0.000
Driver - TPS51604	4	4		1	$0.00
FET (H&L) - CSD87381P	7.5	7.5		1	$0.00
FET (H&L) - CSD87381P	7.5	7.5		1	$0.000
Bulk Cap 330u(9mohm)	31.4	31.4	$0.120	1	$0.120
Bulk Cap 470u	31.4	31.4	$0.130	1	$0.130
Cap MLCC 22uF	2	30	$0.009	15	$0.135
Cap MLCC 10uF	2	0	$0.008	0	$0.000
Cap MLCC 2.2uF	1	0	$0.008	0	$0.000
Cap MLCC 1uF	1	0	$0.005	0	$0.000
Inductor	49	98	$0.090	2	$0.180
R and Cs	1	38	$0.001	38	$0.038
NTC (Thermistor)	1	4	$0.015	4	$0.06
Total		288		65	$0.663

TPS59641 Baytrail-M/D/I reference design w/CSD97374 PS



TPS59641 Baytrail-M/D/I reference design with CSD87381P PowerBlock II



Texas Instruments

Reference Design, TPS59641A, 1ph CPU+1Ph GPU

TEXAS INSTRUMENTS

5V/3.3V System Rail

TPS51285A/B

5-24Vin/ Dual CH Controller for 5V/ 3.3V rails with ULQ™

Sample	
Samples	**Production**
Now	Apr'13

Features

- Innovative ULQ™ (Ultra-Low Quiescent current) achieves very high efficiency at light load operation, supports Connected Standby mode of Windows 8
- Iq=75uA (25uA/ch+25uA / 2x LDO)
- Input voltage range: 5V to 24V
- Output voltages: 5V (CH1) and 3.3V (CH2)
- Switching frequency: 400kHz (5V-rail) and 475kHz (3.3V-rail)
- Auto-skip light load operation
- Built-in 100mA 5V/3.3V LDOs
- Clock Output for Charge-pump
- Power Good indicator
- Separate Enable inputs for switchers
- 20pin 3x3(mm) QFN Package

Applications

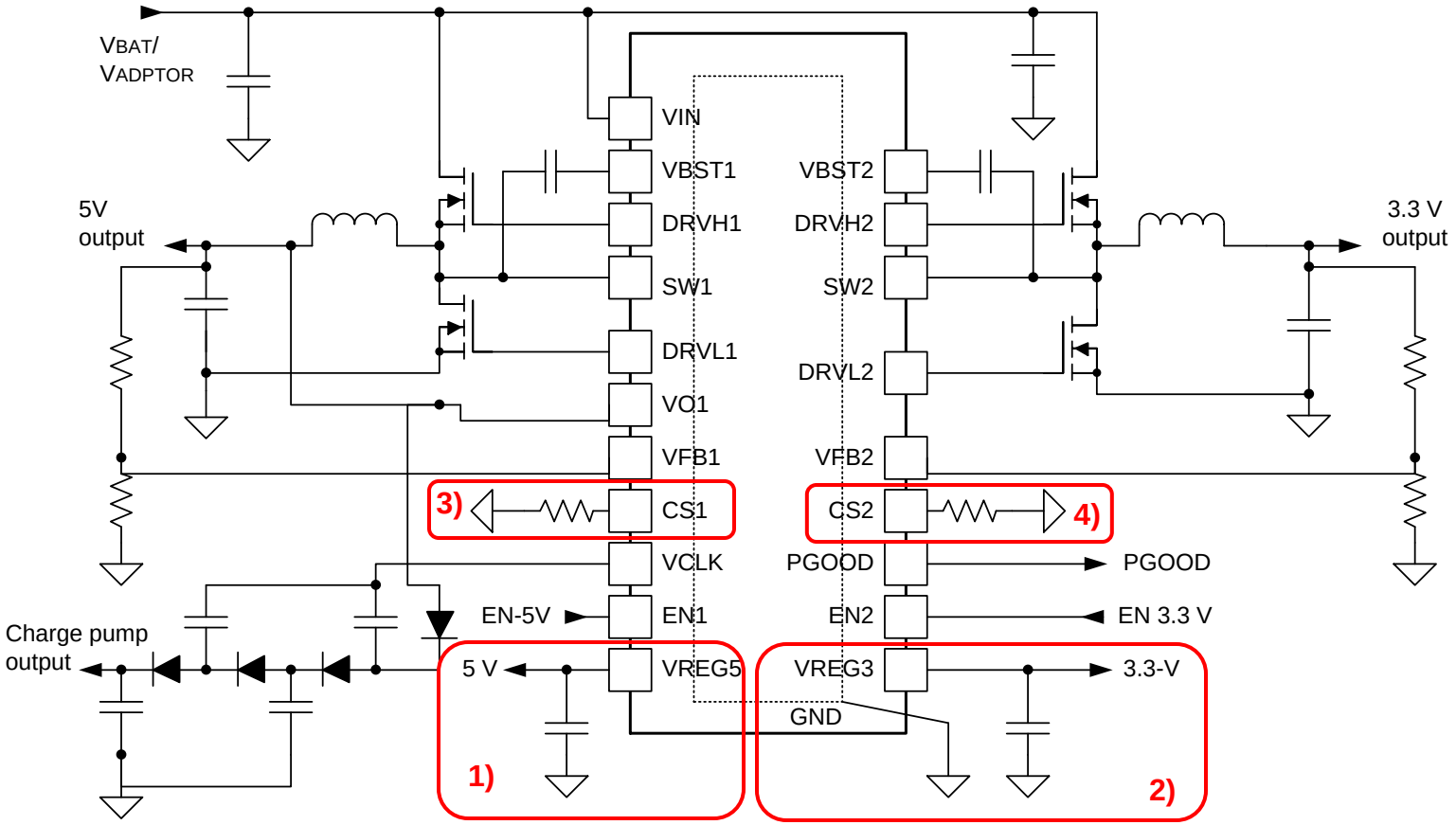
- Ultrabooks
- Notebook Computers
- Tablet Computers
- Embedded Computers

Benefits

- Supports severe power loss requirement of Intel Ultrabook/ Microsoft Connected Standby mode with Auto ULQ function
- Support wide input voltage range including 2-cell battery and 20V adaptor
- Fully integrated 5V/ 3.3V rails solution in Small 3.0x3.0mm QFN Package
  - 100mA 5V/3.3V LDOs
  - Clock Output for Charge-pump
  - Power Good indicator
  - Full protections (UVLO, OVP, UVP, OCL & OTP)
- Easy to use, no external compensation circuit
- Co-layout with TPS51225x and TPS51275x family
- High power density, excellent thermal performance

Version	Always-on LDO
TPS51285A	3.3V LDO
TPS51285B	3.3V & 5V LDOs

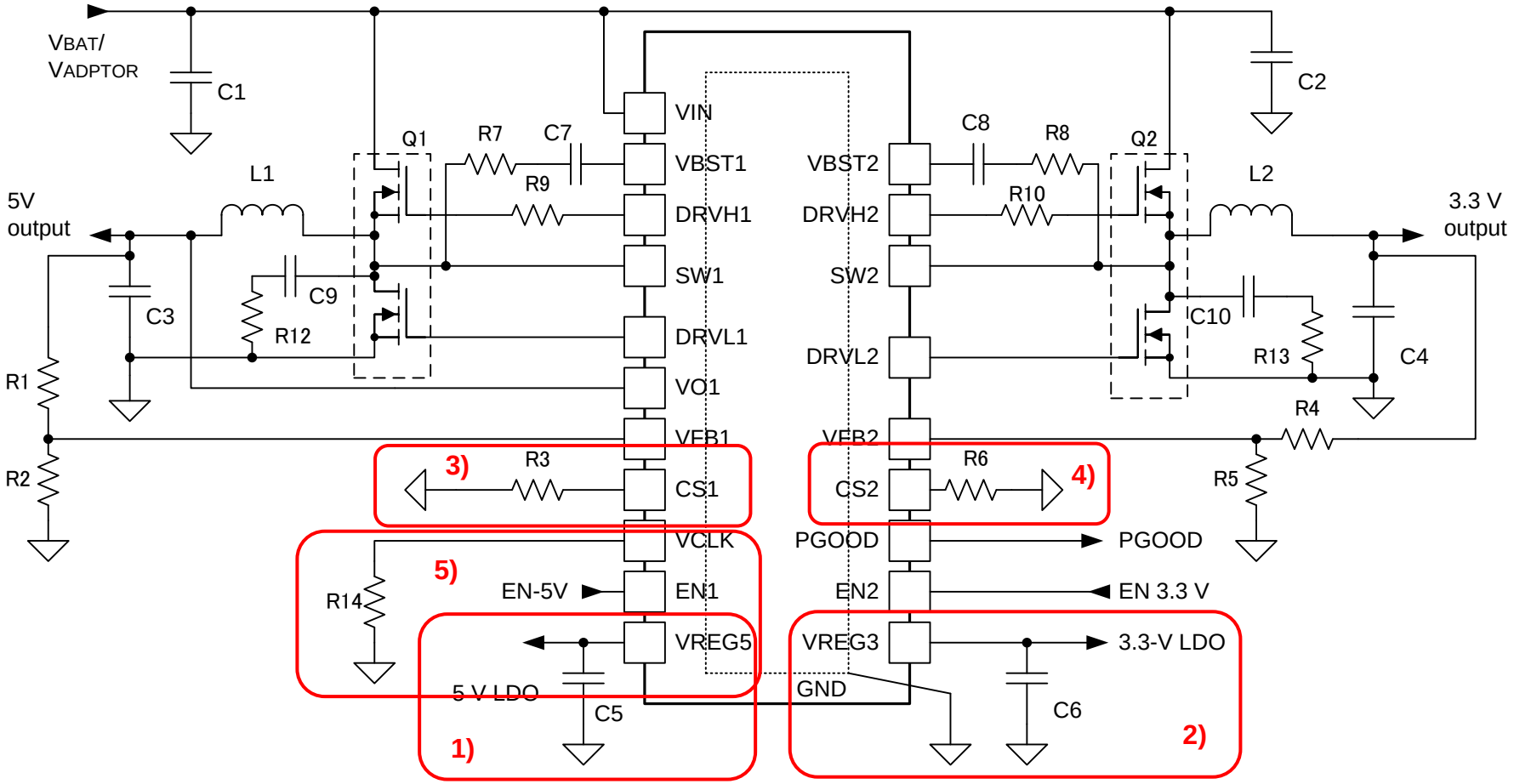
TPS51225/ 51275/ 51285 Co-layout (w/ CP)



When TPS51285A/B is used, please update the below four components.

1) VREG5 cap to 4.7uF
2) VREG3 cap to 4.7uF
3) CS1 resistor to 1/5 of the Tps51225/275 value
4) CS2 resistor to 1/5 of the Tps51225/275 value

TPS51225/ 51275/ 51285 Co-layout (w/o CP)

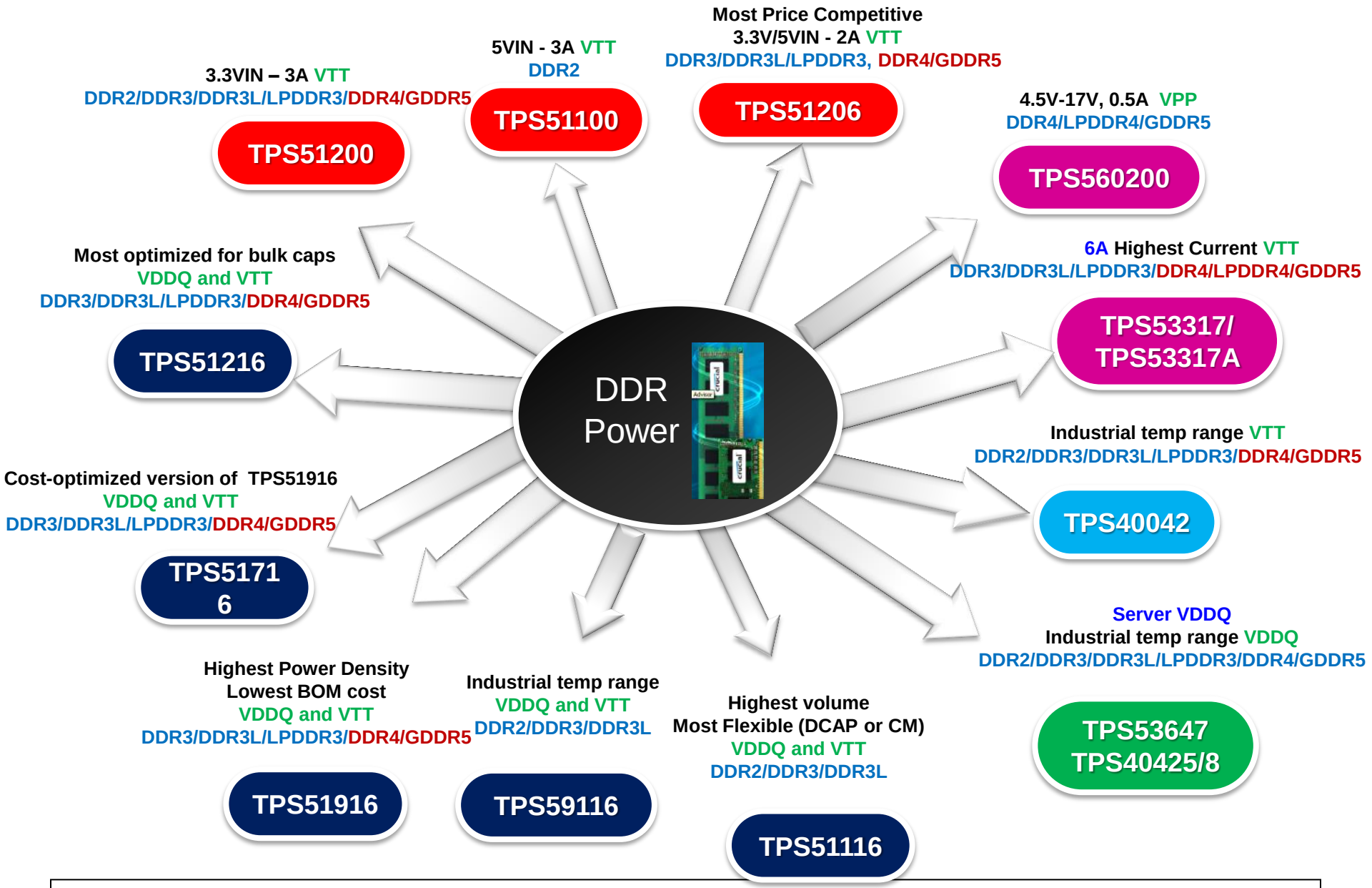


When TPS51285A/B is used, please update the below five components.

1) VREG5 cap to 4.7uF
2) VREG3 cap to 4.7uF
3) CS1 resistor to 1/5 of the Tps51225/275 value
4) CS2 resistor to 1/5 of the Tps51225/275 value
5) Add R14 (200-ohm) (Be open for Tps51225/275)

DDR Power Solutions

DDR Power Solutions Portfolio



DDR Power Supplies & Terminators

	TPS51916	TPS51216	TPS51116	TPS51206	TPS51100	TPS51200	TPS53317	TPS53317A
General Description	**Complete DDR2, DDR3 and DDR3L Power Solution**	**Complete DDR2, DDR3 and DDR3L Power Solution**	**Complete DDR2, DDR3 Power Solution**	**2-A Peak Sink/Source DDR Termination Regulator**	**Source-Sink DDR Termination Regulator 3A Source, 3.5A Sink**	**Source-Sink DDR Termination Regulator**	**Source-Sink 6A Integrated FET Switching DDR Termination Regulator**	**Source-Sink 6A Integrated FET Switching DDR Termination Regulator**
VIN	3V to 28V	3V to 28V	3V to 28V	3.3V to 5V	4.75V to 5.25V	0.3V to 3.6V	1V to 6V	0.9V to 6V
# outputs	4, VDDQ, VTT, VTTREF and 1P8VREF	4, VDDQ, VTT, VTTREF and 1P8VREF	3, VDDQ, VTT and VTTREF	2, VTT and VTTREF	1 VTT	1 VTT	1 VTT	1 VTT
Fsw (kHz)	300/400/500/670	300/400	400	N/A	N/A	N/A	600kHz and 1MHz	600kHz and 1MHz
Control topology	D-CAP and D-CAP2	D-CAP	D-CAP and D-CAP+	LDO	LDO	LDO	D-CAP+	D-CAP
Compensation	No comp is required.	No comp is required.	Internal and external comp	N/A	N/A	N/A	No comp is required.	No comp is required.
DDR compatibility	DDR2, DDR3 and LPDDR3	DDR2, DDR3 and LPDDR3	DDR1, DDR2, DDR3	DDR, DDR2, DDR3, and low-power DDR3/DDR4 VTT Memory Termination	DDR, DDR2 VTT Memory Termination	DDR, DDR2, DDR3, and low-power DDR3/DDR4 VTT Memory Termination	DDR, DDR2, DDR3, and DDR4 VTT Memory Termination	DDR, DDR2, DDR3, and DDR4 /LPDDR4 VTT Memory Termination
VTT referencing scheme	Reference to VTTREF and trim option to 1/2*VDDQ	Reference to VTTREF and trim option to 1/2*VDDQ	Fixed reference to VTTREF		Integrated Divider Tracks 0.5 VDDQSNS for VTT and VTTREF	REFIN Input Allows for Flexible Input Tracking Either Directly or Through Resistor Divider	2R Divider from Vddq to form 1/2*VDDQ	2R Divider from Vddq to form 1/2*VDDQ
VTT output cap	1 x 10uF or 2 x 10uF	1 x 10uF or 2 x 10uF	2 x 10uF	N/A	N/A	N/A	3 x 47uF	11x22uF for DDR4
VTT current	+/-1A TDC and +/-2A for OCL	+/-1A TDC and +/-2A for OCL	+/-2A TDC and +/-3A for OCL	N/A	N/A	N/A	-/-6A	-/-6A
VTT accruacy	0A, +/-15mV to VTTREF; +/1A, +/-20mV to VTTREF	0A, +/-15mV to VTTREF; +/1A, +/-20mV to VTTREF	0A, +/-20mV to VTTREF; +/1A, +/-30mV to VTTREF; +/-2A, +/-40mV to VTTREF	N/A	N/A	N/A	+/- 1%	+/- 1%
S3/S5 support	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
PGOOD	Yes	Yes	Yes	No	No	Yes	Yes	Yes
FCCM	Yes	Yes	No	N/A	N/A	N/A	Yes	Yes
Power save	Auto skip	Auto skip	Auto skip	N/A	N/A	N/A	Yes	Yes
Support all ceramic	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes
SS method	REFIN control	REFIN control	Two step OCL limit	N/A	N/A	N/A	Internally Set 1.6ms	Internally Set 1.6ms
Bootstrap support	10ohm Internal switch	10ohm Internal switch	Internal diode	N/A	N/A	N/A		
OVP/UVP	Yes	Yes	Yes	N/A	N/A	N/A	Yes	Yes
Package	20pin 3x3mm RUK, 0.4mm pitch and 0.75mm height	20pin 3x3mm RUK, 0.4mm pitch and 0.75mm height	20pin TSSOP	2mm x 2mm SON10 PowerPAD	MSOP 10 with PowerPad	3mm x 3mm SON10	3.5mm x 4mm 20 pin QFN	3.5mm x 4mm 20 pin QFN

TPS51916

Complete DDR2, DDR3, DDR3L, and DDR4 Power Solution

Features

Synchronous Buck Controller (VDDQ)

- Conversion Voltage Range: 3 V to 28 V
- Selectable D-CAP™or D-CAP2™Mode
- Selectable 300 kHz/400 kHz/ 500kHz or 670kHz
- Auto-Skip Mode at Light loads
- Supports Soft-Off in S4/S5 States
- OCL/OVP/UVP/UVLO Protections

2A LDO(VTT), Buffered Reference(VTTREF)

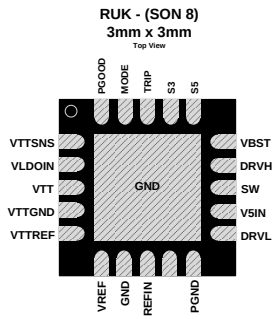
- 2-A (Peak) Sink and Source Current
- Thermal Shutdown
- 20-Pin, 3 mm × 3 mm, QFN Package

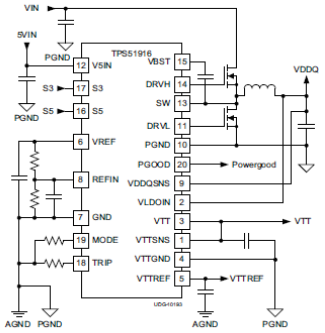
Benefits

- Wide range of input voltages for multiple rails
- Fast Transient Response, No loop compensation.. saves 4 resistors 2 Capacitors compared to VM controller. Fewer Output Capacitors Reduces BOM cost by 20%
- Flexible form factor, 30% smaller at 670kHz
- 90%+ Efficiency at Light Load with Higher Average Efficiency Over Entire Load Range
- Eliminates Pre-Bias issues
- Full suite of protection
- Compatible with both DDR2, DDR3 and DDR3L
- Built in protection
- Thermally enhanced packaging

Applications

- DDR2/DDR3/DDR3L Memory Power Supplies
- SSTL_18, SSTL_15, SSTL_135 and HSTL Termination





TPS51206

2A- peak Sink/ Source DDR Termination Regulator with Buffered Reference

Features

- Supports DDR2 (0.9V), DDR3 (0.75V), DDR3L (0.675V), LPDDR3 (0.6V) and DDR4 (0.6V)
- Supply Input Voltage: down to 3.1V
- VLDOIN Input Voltage Range: VTT+0.4V to 3.5V
- VTT Termination regulator
  - Output Voltage range: 0.5V to 0.9V
  - 2A peak Sink/ Source current
- VTTREF Buffered Reference
  - VDDQ/2 +/-1% Accuracy
  - 10mA Sink/ Source current
- Fully supports S3 (high-Z) and S4/S5 (soft-off) mode (S3&S5)
- 10-pin 2x2 SON Package w/0.8mm Height

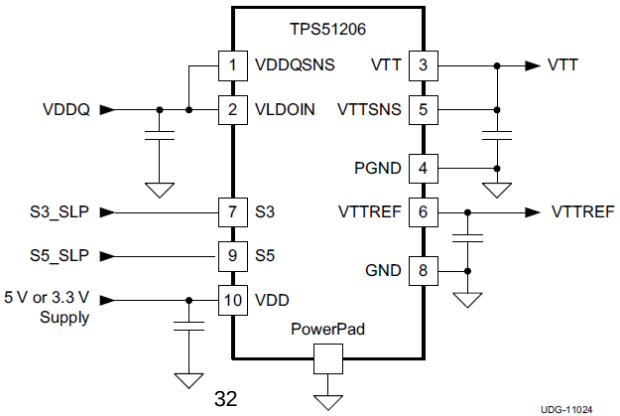
Benefits

- Reduce board area and total BOM cost
  - Only 1x10uF VTT output capacitance is required
  - No external voltage divider resistors, implements VDDQ voltage sensing input (VDDQSNS)
  - External components are Only 4 caps
  - Small 2.0x2.0mm SON Package
- Easy to use, supports 5V or 3.3V supply input voltage (VDD)
- S3/S5 enables support S3 (high-Z) and S4/S5 (soft-off) mode
- High power density, excellent thermal performance

Applications

- Ultrabooks
- Notebook Computers
- Tablet Computers
- Embedded Computers

STATE	S3	S5	VTTREF	VTT
S0	H	H	ON	ON
S3	L	H	ON	OFF (high-Z)
S4/S5	L	L	OFF (discharge)	OFF (discharge)



3A iFET Converters

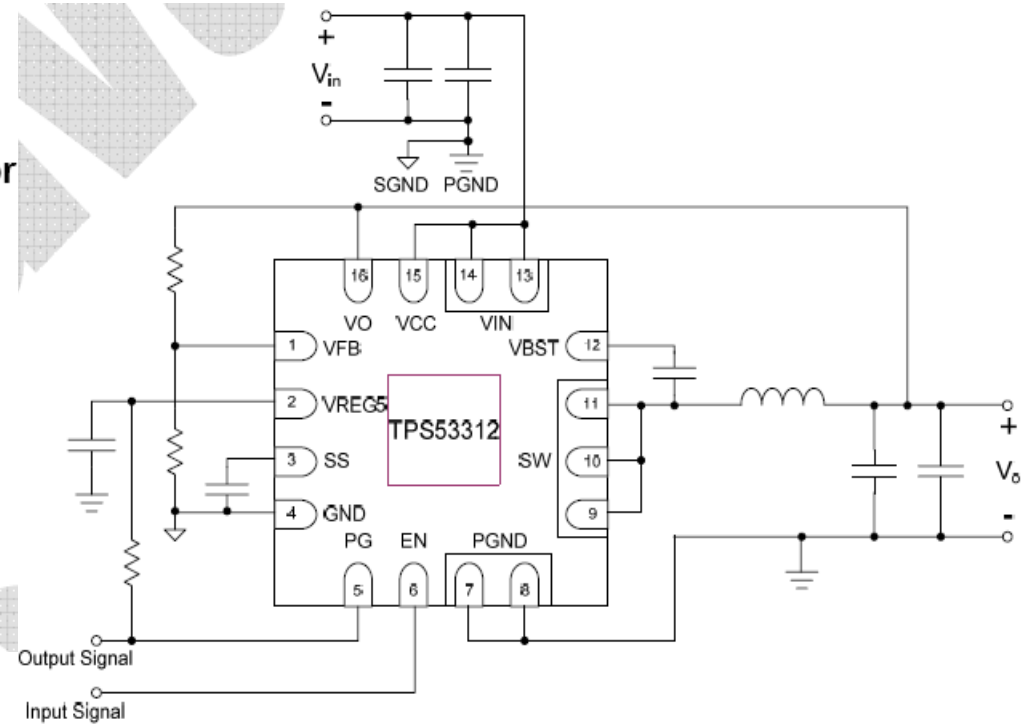
TPS53312 – 18V, 3A SINGLE CHANNEL SYNCHRONOUS STEP-DOWN CONVERTER WITH ECO MODE IN 3x3 QFN

Features

- Continuous 3A Output Current
- 4.5V – 18V Vcc Voltage Range
- 2V – 18V Conversion Voltage Range
- Adjustable Output Voltage Ranging from 0.76V to 5.5V
- DCAP2™ Mode Control Enables Fast Transient Response
- Low Output Ripple and Support all MLCC Output Capacitor
- Skip Mode for Light Load Control
- Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications
- High Efficiency, less than 10µA Supply Current at Shutdown
- Adjustable Soft Start Time
- Support Pre-Biased Soft Start
- 700kHz Switching Frequency
- Cycle-By-Cycle Over-Current Limit
- Open Drain Power Good Indication
- Internal Boot Strap Switch
- Small 3 x 3 - 16 Pin QFN Package

Benefits

- Fast Transient Response, No Compensation
- Lowest external component count to optimize board space / cost effective solution
- Easy to design with no effort in external compensation adjustment



TPS6213x/4x/5x:

3 .. 17V V_{IN}, 1-3A, 3MHz Step-Down Converters in 3x3mm QFN

Features

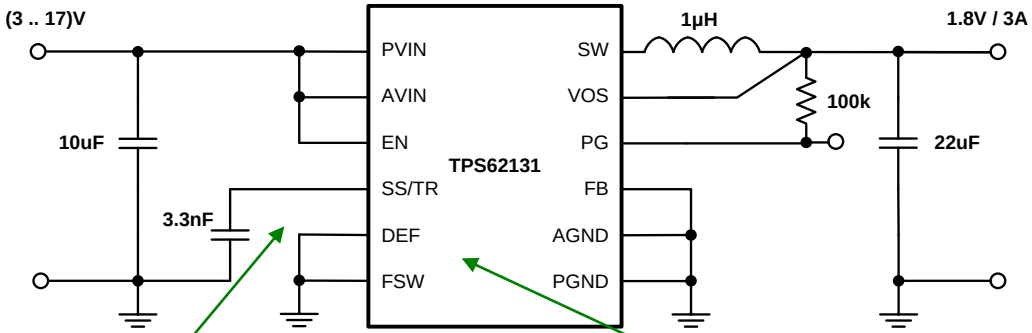
- High Efficiency Step Down Converter with DCS-Control™
- VIN range from 3 to 17V
- Adjustable VOUT from 0.9 to 6.0V
- Fixed VOUT options: 1.8V, 3.3V, 5.0V
- Output current up to: 3A (TPS62130)
  2A (TPS62140)
  1A (TPS62150)
- Seamless transition to Power Save Mode
- Pin-selectable switching frequency
- 100% Duty Cycle Mode
- Programmable Soft Start and Tracking
- Quiescent current of 17uA (typ.)
- Power Good

Benefits

- High VIN step down converter with small solution size
- 12V → 3.3V / 3A utilizing a 1uH inductor
- DCS-Control™ regulation is fast and accurate
- Low quiescent current and selectable switching frequency for high efficiency
- VFB control allows current source applications

Applications

- Solid State Disk Drives
- Embedded and mobile Computing
- Industrial applications



Cstart	Adjustable Startup
TR	FB Voltage Control

DEF	Pin Selectable Output Voltage
FSW	Pin Selectable Switching Frequency

CONCLUSION

- TPS59641 optimized IMVP7 controller for Intel 2014 Essential Client PCs and Embedded PCs using Valleyview CPU – on three (3) Intel CRBs!
- TI has the complete power solution
- High Switching Frequency for High Power Density
  - Complete Discrete Solution fit on 55x85 COME Module
- High Feature Integration for Low Component Count
  - DCAP+ Control Mode for Lowest Output Cap Count
- Higher Efficiency through out the load current range