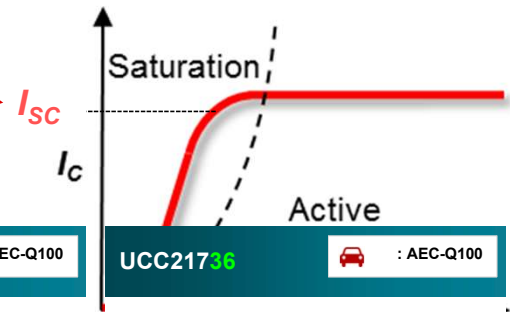
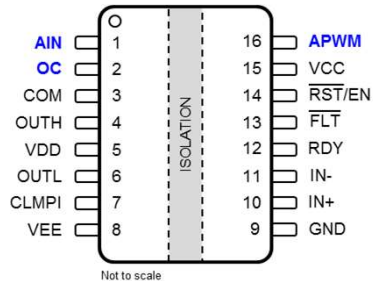


## How can we detect SC/OC?

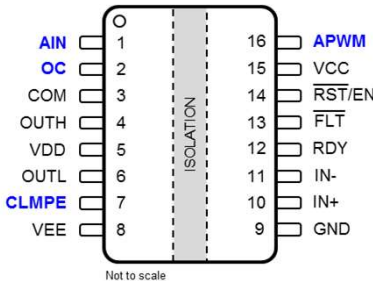
- Directly measure current
- UCC217xx with OC pin!



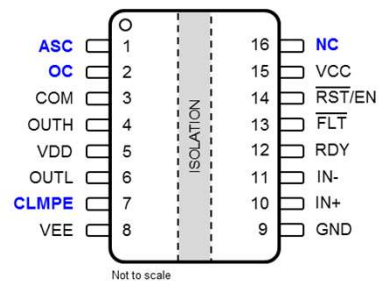
**UCC21710** : AEC-Q100



**UCC21732/39** : AEC-Q100



**UCC21736** : AEC-Q100

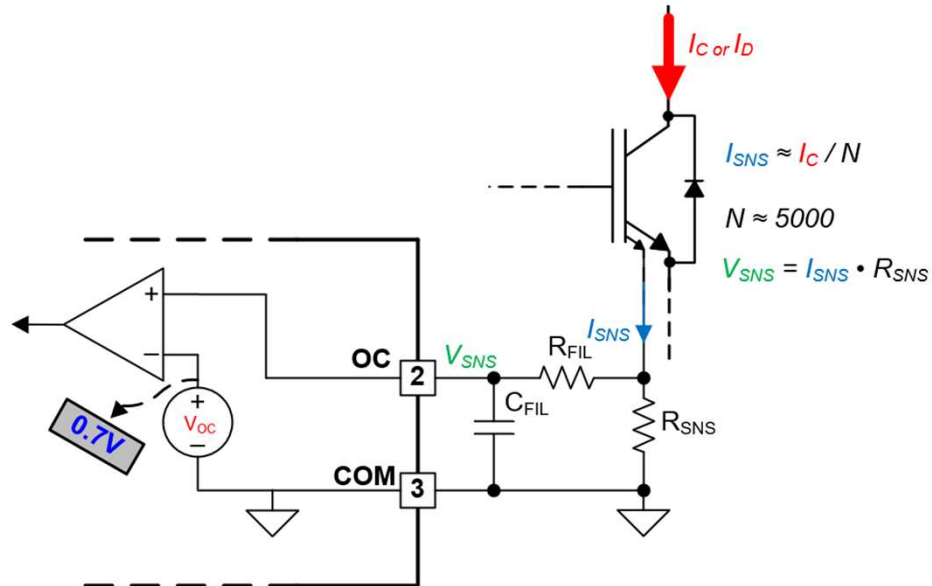


TI Information – Selective Disclosure



UCC21710,32,39, and 36 all have an "OC" pin, which roughly speaking, is a comparator with 0.7V threshold, which is used for current-based detection schemes.

# Current-based Detection – sense-FET / sense-IGBT



TI Information – Selective Disclosure



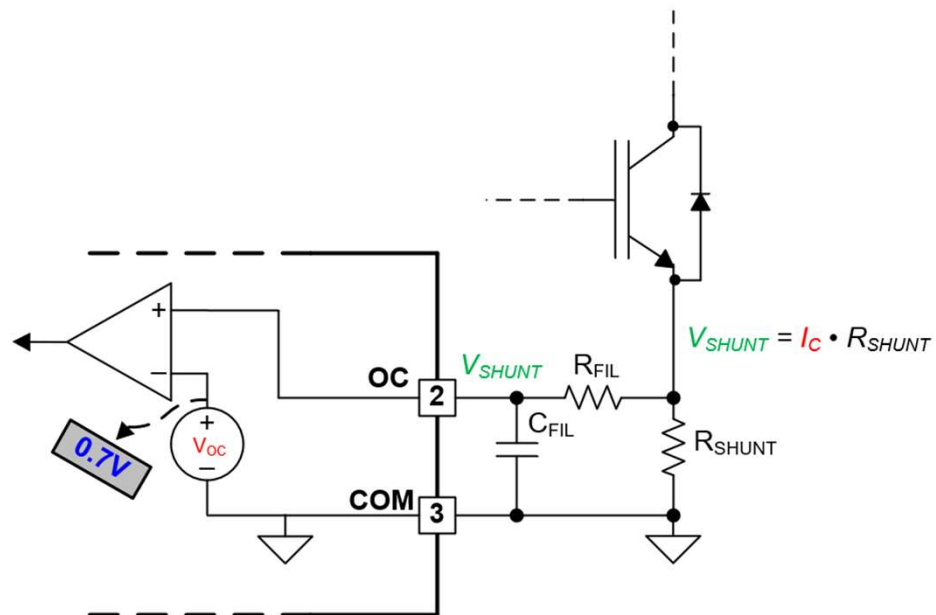
Here we see the block diagram of UCC217xx's OC system, configured for current-detection with a sense FET, using a sense resistor to do IV conversion, and a simple RC filter. At the comparators output there is also a 120ns glitch filter.

Sense-FET and sense IGBTs have an additional "current-sense" terminal which sources a small, small fraction of the collector or drain current, often at a ratio of 5000:1-10000:1

We can see the design process is straightforward. Once we set a collector current, we only need to choose  $R_{SNS}$  based on ohms law so that  $V_{SNS} >$  the internal 0.7V OC threshold triggers OC detection and shuts down the device.

Though it is not a true current mirror, this detection method is fast and accurate.

## Current-based Detection – Shunt Resistor



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TEXAS INSTRUMENTS

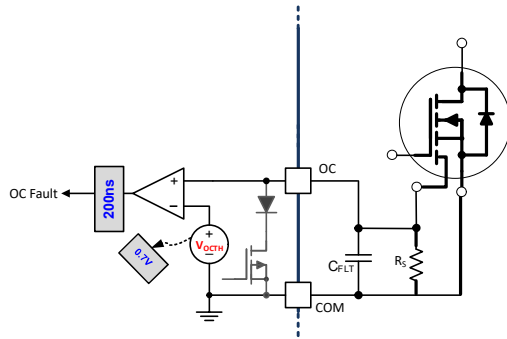
Even if we don't have a device with current-sense, we still have the option of doing direct current measurement using a very small-valued, precise shunt resistor, such as nichrome or wire-wound resistor which can handle the large collector current.

# UCC217xx: fast SC detection – Current Sensing

## OC for SenseFET: UCC21710/32/36/39

- OC Detection Time: 200ns
- OC Detection Threshold: 0.7V

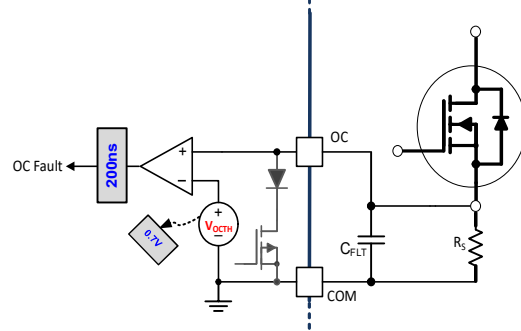
⇒ **Fast & Accurate Detection**



## OC for Shunt Resistor: UCC21710/32/36/39

- OC Detection Time: 200ns
- OC Detection Threshold: 0.7V

⇒ **High power loss**



TI Information – Selective Disclosure

TEXAS INSTRUMENTS

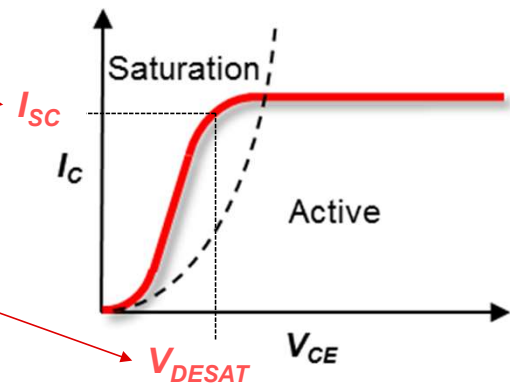
To summarize our current sensing OC/SC detection methods using OC with its low 0.7V threshold, both offer very fast detection of up to 200ns which gives us plenty of headroom below the typical SC withstand time for SiC. Current-sense methods are also equally appropriate for both SiC and IGBTs.

sense-FETs and sense-IGBTs are not exceedingly common, compared to their sense-less counterparts, so we do not see this detection method employed as often.

The shunt resistor method is equally fast and accurate, and can be used with any discrete IGBT or SiC fet. The main drawback is it suffers from large  $I^2R$  losses due to the high collector currents, hampering efficiency which is a contradiction to designing with SiC.

## How can we detect SC/OC?

- Set a current threshold
- Set a voltage threshold
  - We need an early threshold for SiC!



TI Information – Selective Disclosure

 TEXAS INSTRUMENTS

Our methods to detect short circuit and overcurrent are largely grouped into 2 categories.

We've already gone over current-based short-circuit & overcurrent detection, but is that the only way?

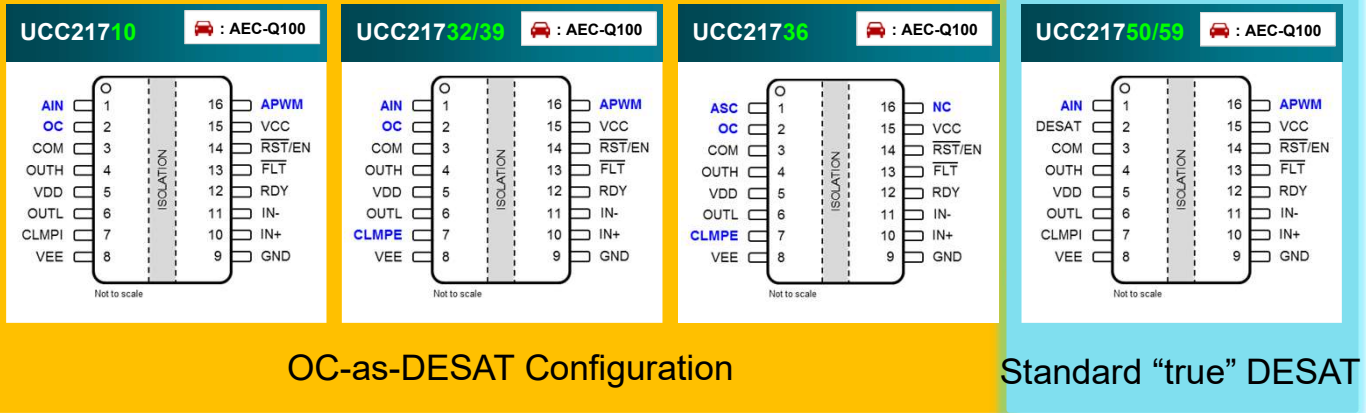
The answer is NO! We can use a purely-voltage based detection method as well, and as we saw previously, for IGBT, voltage based detection can be very effective due to its IV characteristics.

This, in effect, uses the power-switch itself as a sort of I-V converter, loosely extrapolating  $I_C$  or  $I_D$  current based on the drain or collector voltage.

# How can we detect SC/OC?

- Set a current threshold

↑ Saturation!



TI Information – Selective Disclosure



Our methods to detect short circuit and overcurrent are largely grouped into 2 categories.

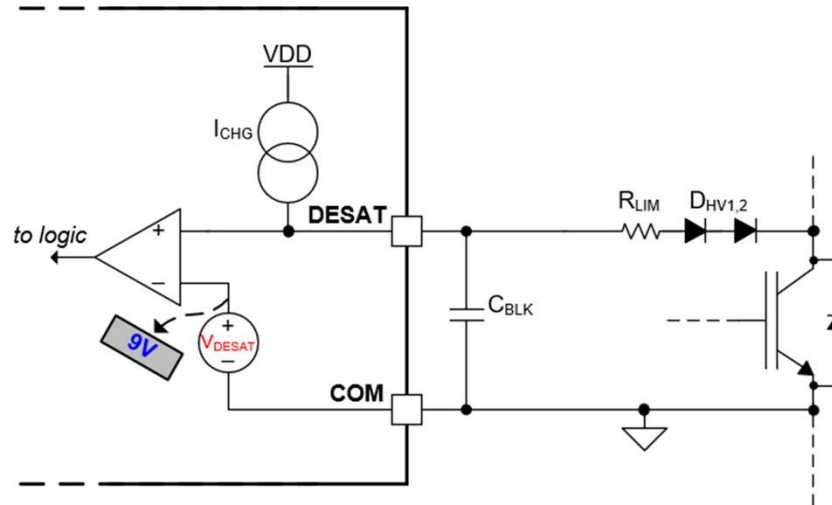
We've already gone over current-based short-circuit & overcurrent detection, but is that the only way?

The answer is NO! We can use a purely-voltage based detection method as well, and as we saw previously, for IGBT, voltage based detection can be very effective due to its IV characteristics.

This, in effect, uses the power-switch itself as a sort of I-V converter, loosely extrapolating IC or ID current based on the drain or collector voltage.

# Voltage-based Detection – DESAT

- DESAT has high, 9V internal threshold, and 500uA charging current



TI Information – Selective Disclosure

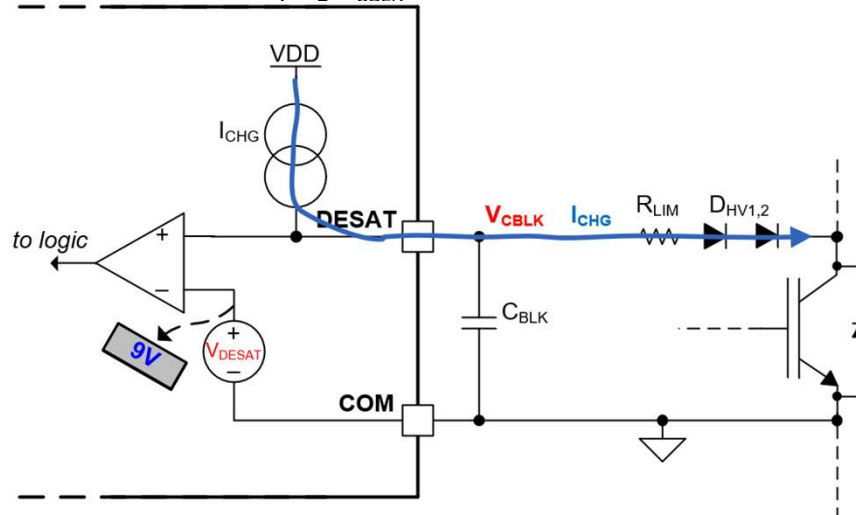
TEXAS INSTRUMENTS

Compared to OC, we see that DESAT circuit looks quite a bit different, with an internal current source, and high voltage diodes to the collector.

How does it work?

## Voltage-based Detection – DESAT

- **Normal operation**, collector/drain voltage is **low**, diodes are **forward biased**
- CHG current flows to drain/collector, keeping  $V_{\text{CBLK}}$  low



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TEXAS INSTRUMENTS

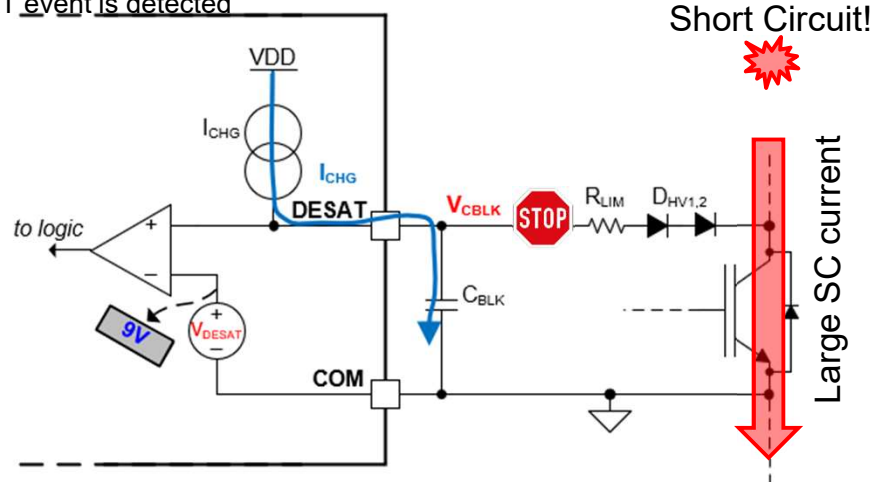
During normal operation of the power switch, its drain/collector voltage is low, and the charging current flows through the diodes and out to the sea.

This keeps the voltage at the pin low since the blanking cap is not being charged up.



# Voltage-based Detection – DESAT

- **Short-circuit/Overcurrent**, collector/drain voltage increases quickly, & diodes become **reverse biased**
- CHG current now charges blanking cap, increasing  $V_{CBLK}$ , and eventually beyond the 9V threshold.
- At that point, DESAT event is detected



TI Information – Selective Disclosure

TEXAS INSTRUMENTS

During an Short circuit even, or overcurrent, the IC / ID current is high and the drain current.

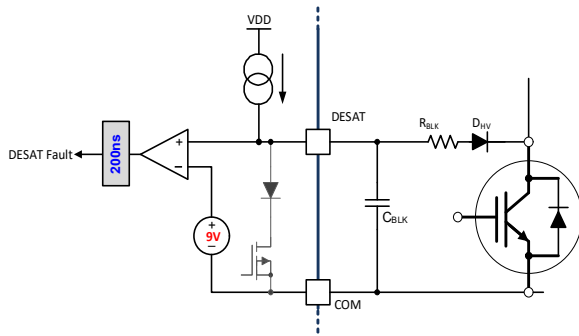
The collector / drain voltage rises and the diodes are no longer forward biased. All the current now charges the blanking cap. After its charged up above  $V_{DESAT}$ , the comparator will trip and short-circuit will be detected by the driver.

# UCC217xx: fast SC detection – Voltage Sensing

## DESAT (Standard) for IGBT: UCC21750/59

- Internal DESAT Threshold: 9V

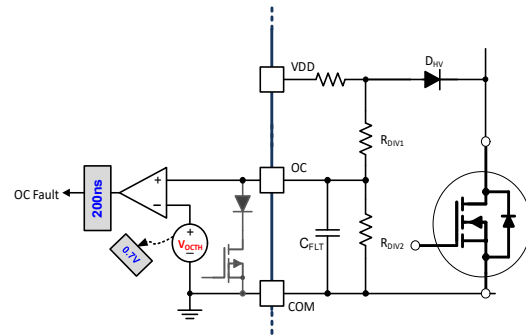
⇒ **Proven DESAT for IGBT**



## OC for DESAT: UCC21710/32/36/39

- OC Detection Time: 200ns
- OC Detection Threshold: 0.7V

⇒ **Flexible DESAT Threshold**



TI Information – Selective Disclosure



Now to summarize our voltage-detection methods.

UCC21750/59 has a “true” DESAT detection circuit with a internal 9V threshold, which is tuned for use with IGBTs. and built-in, fixed current source to charge the blanking cap.

This method is simple to implement, and highly effective for protecting IGBTs.

Because it is tailored for the majority of IGBTs, When it comes to SiC, using UCC21750’s “true” DESAT is not a silver-bullet solution,

For one, the 9V threshold is far too high for SiC owing to its I-V characteristics, though we can bring that down with discrete components to an appropriate level.

Secondly, the charging current is fixed internally, which charges the blanking cap slower. We can only reduce the blanking cap and thus the blanking time so much, so this is a limitation when protecting SiC.

For SiC we generally need to set this DESAT detection threshold to no more than a few volts. Without setting an lower threshold, the power dissipation becomes too high too quickly and swift failure of SiC fet follows.

The true DESAT system also has a “leading edge blanking time” which leaves far less headroom below SiC’s SC withstand time which is already much short than for IGBTs, further contributing to the need to set a lower DESAT threshold.

With SiC, even 100ns can be too long to spare.

To put it simply, while “true” DESAT can work for both SiC and IGBTs, it is best suited for IGBTs and requires careful design and consideration of timing to ensure detection to shutdown happens in <1us.

Though we just the OC-detection system used for direct over-current detection, we can actually configure it in a DESAT configuration, which I’ll call OC-DESAT.

The operation theory is the same as with “true” DESAT, so we don’t need to go over it in extreme detail.

We notice that the circuit basically adds just 2 resistors compared to true DESAT. The top replaces the internal current source, and the bottom sets our OC threshold as part of a resistor divider.

The blanking time can now be controlled on 2 fronts, we can change the cap value, and we now have control over the charging current, so we can control and shorten the blanking time for SiC

Compared with the current-detection methods, this option does not consume a lot of power and can work with any discrete, halfbridge, 6pack modules.

The low-threshold of the gate driver’s OC detection system allows us not only to set a low detection threshold, but to fine-tune it with a resistor divider.

Further-more we can adjust the

Though current-based detection has its advantages, the simplicity, low-cost, flexibility of using OC-DESAT means this is frequently used in SiC systems.

Current-based detection methods are somewhat easier to understand in terms of design , being essentially based on ohms law.  
True DESAT and OC-DESAT have a few more moving parts, so in the next part of our presentation we will discuss design of these DESAT systems in greater detail.

## Summary of SC detection methods.

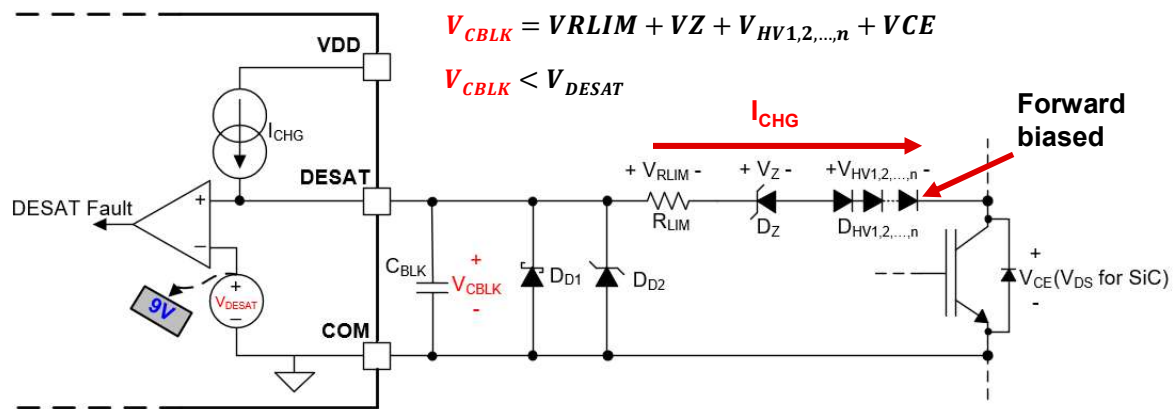
| Detection Method                   | Benefits                                      | Drawbacks  |
|------------------------------------|---|--|
| <b>DESAT</b><br><b>OC-as-DESAT</b> | Simple<br>Works with both Discretes & Modules | UCC21750 DESAT tuned for IGBTs<br>Timing                     |
| <b>Shunt Resistor (OC)</b>         | Most accurate                                 | High $I^2R$ losses<br>Can't be used with Half-bridge modules |
| <b>sense-FET/IGBT (OC)</b>         | More Accurate than DESAT                      | Limited IGBTs/SiC with current-sense feature                 |

TI Information – Selective Disclosure



## UCC217xx DESAT-pin (UCC21750/59) : Normal operation

- IGBT or SiC MOSFET is ON
- No short circuit condition
- Low  $V_{CE}/V_{DS}$
- $V_{CE}/V_{DS}$  must be lower than  $V_{DESAT}$  during normal operation



TI Information – Selective Disclosure

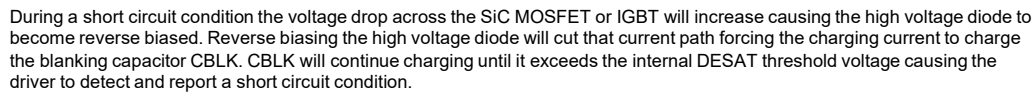
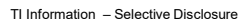


TEXAS INSTRUMENTS

During normal operation the SiC MOSFET or IGBT will have a low voltage drop. In order for the DESAT-pin function to work the voltage drop across the SiC MOSFET or IGBT must be lower than the internal DESAT threshold voltage during normal operation.

The blanking capacitor C\_BLK connected between the DESAT-pin and COM-pin will charge up to a voltage determined by the voltage drop across the current limiting resistor, Zener diode, high voltage diodes, and SiC MOSFET or IGBT. Once C\_BLK charges up to all of these voltage drops combined the high voltage diode will become forward biased keeping C\_BLK from charging to a higher voltage. The voltage that C\_BLK charges up to must be designed in such a way that it will be lower than the internal DESAT threshold voltage V\_DESAT. The difference between V\_DESAT and blanking capacitor voltage will prevent from having a false short circuit condition due to noise in the system.

- IGBT or SiC MOSFET is ON
- $V_{CE}/V_{DS}$  is high due to short circuit / overcurrent condition
- High voltage diode becomes reverse biased causing ICHG to charge CBLK

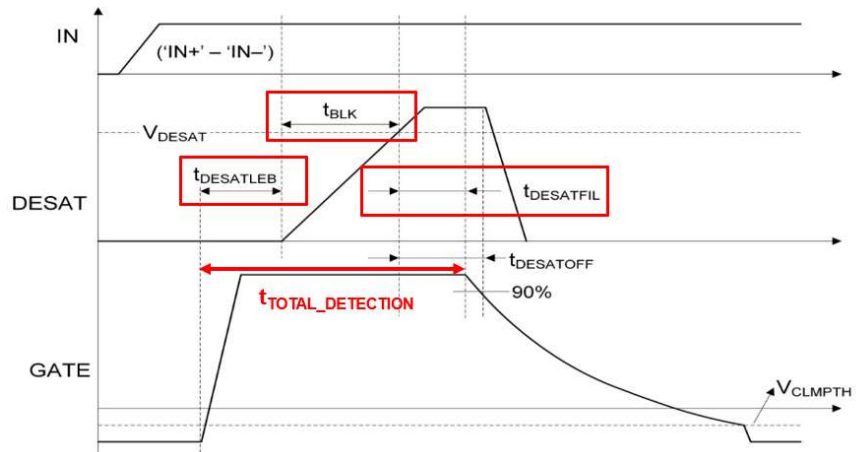


# UCC217xx DESAT-pin (UCC21750/59) : Short circuit / overcurrent detection timing

$$t_{TOTAL\_DETECTION} = t_{DESATLEB} + t_{BLK} + t_{DESATFIL}$$

$$t_{BLK} = \frac{C_{BLK} * V_{DESAT}}{I_{CHG}}$$

- Internal timing parameters
  - $t_{DESATLEB}$
  - $t_{DESATFIL}$
- Adjustable timing parameter
  - $t_{BLK}$
- Lower timing flexibility due to  $t_{DESATLEB}$  &  $t_{DESATFIL}$



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Looking into the detection timing, the longest it will take the gate driver to detect a short circuit condition and shutdown a SiC MOSFET or IGBT is when it turns ON into a short circuit condition. When turning ON into a short circuit condition the total detection time is broken down into three timers; the leading edge blanking time, the blanking time, and the desat deglitch filter.

The leading edge blanking time denoted as  $t_{DESATLEB}$  is the first timer in the detection timing. During the leading edge blanking time the blanking capacitor voltage will remain at 0V due to the internal current source being disabled.

The second timer is the blanking time which can be configured through proper sizing of the blanking capacitor. During the blanking time the internal current source will be ON and will charge the blanking capacitor up to the internal DESAT threshold voltage.

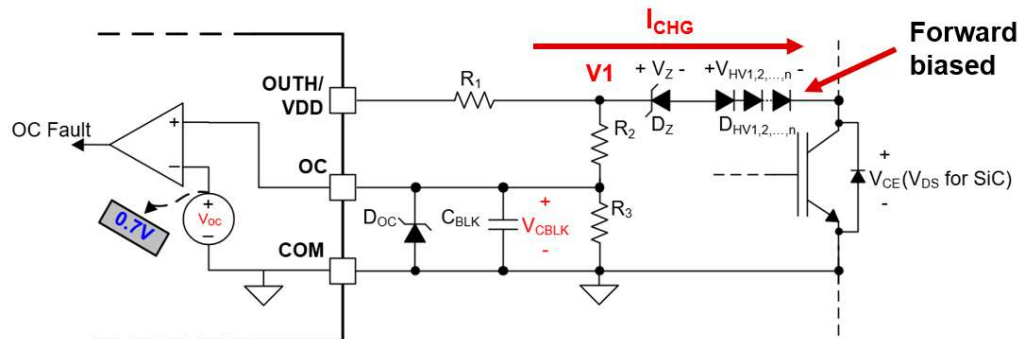
The last timer is the internal DESAT deglitch filter. The blanking capacitor voltage must be greater than the internal DESAT threshold voltage for longer than the DESAT deglitch filter for the gate driver to report a short circuit condition. This timer prevents the gate driver from reporting a short circuit condition in the case there are short voltage spikes on the DESAT-pin due to noise in the system.

The leading edge blanking time and DESAT deglitch filter are set internal timers that cannot be adjusted. This is a disadvantage for SiC MOSFETs since these devices typically need fast detection and shutdown timing to prevent damage.

## UCC217xx OC-pin for DESAT (UCC21710/32/36/39) : Normal Operation

- IGBT or SiC MOSFET is ON
- No short circuit condition
- Low  $V_{CE}/V_{DS}$
- $V_{CE}/V_{DS}$  can be higher than  $V_{OC}$  during normal operation

$$V_1 = V_Z + V_{HV1,2,\dots,n} + V_{CE} \quad V_{CBLK} = \frac{R_3}{(R_3 + R_2)} * V_1 \quad V_{CBLK} < V_{OC}$$



TI Information – Selective Disclosure



Similar to the DESAT-pin function during normal operation the SiC MOSFET or IGBT will have a low voltage drop. With the OC-pin function the voltage drop across the SiC MOSFET or IGBT doesn't have to be lower than the internal OC threshold voltage due to having more flexibility on the design with the voltage divider network created with R2 and R3.

With the OC-pin the blanking capacitor CBLK connected between the OC-pin and COM-pin will charge up to a voltage determined by the voltage drop across the Zener diode, high voltage diodes, SiC MOSFET or IGBT, and the voltage divider created by R2 and R3. Once V1 reaches the voltage drop across the Zener diode, high voltage diodes, and SiC MOSFET or IGBT combined the high voltage diode will become forward biased keeping CBLK from charging to a higher voltage. The voltage that CBLK charges up to must be designed in such a way that it will be lower than the internal OC threshold voltage  $V_{OC}$ . The difference between  $V_{OC}$  and blanking capacitor voltage will prevent from having a false short circuit condition due to noise in the system.

- During normal operation the high voltage diode will be forward biased
- $C_{BLK}$  will only charge up to a voltage determined by the external components
- $C_{BLK}$  voltage is given by equation 3

$$V_{CBLK} = \frac{R_3}{(R_3 + R_2)} * V_1 \quad (3)$$

Where

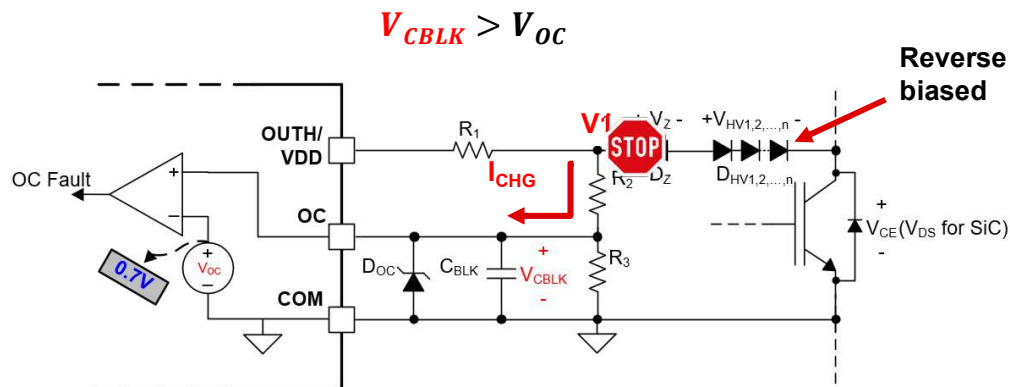
- $V_1 = V_Z + V_{HV1,2,\dots,n} + V_{CE}$ 
  - $V_Z$  is the voltage drop across the Zener diode
  - $V_{HV1,2,\dots,n}$  is the voltage drop across n number of high voltage diodes



- $V_{CE}$  is the voltage drop across the IGBT ( $V_{DS}$  in the case of SiC)
- R2 & R3 are the voltage divider network to adjust the  $V_{CE}/V_{DS}$  detection threshold

## UCC217xx OC-pin for DESAT (UCC21710/32/36/39) : Short circuit / overcurrent condition

- IGBT or SiC MOSFET is ON
- $V_{CE}/V_{DS}$  is high due to short circuit / overcurrent condition
- High voltage diode becomes reverse biased causing  $I_{CHG}$  to charge CBLK



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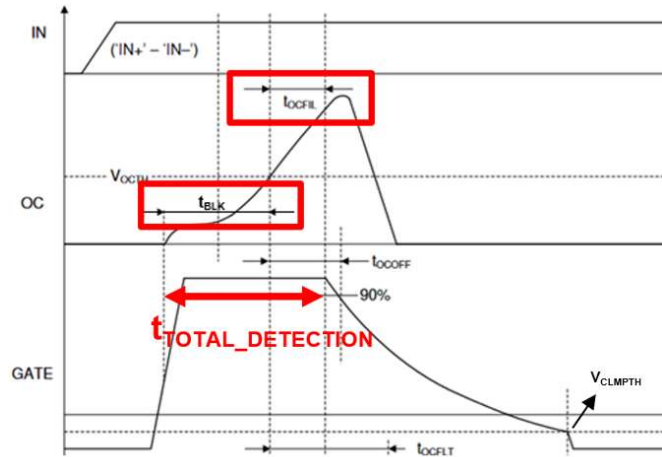
During a short circuit condition the voltage drop across the SiC MOSFET or IGBT will increase causing the high voltage diode to become reverse biased. Reverse biasing the high voltage diode will cut that current path forcing the current to charge the blanking capacitor CBLK. CBLK will continue charging until it exceeds the internal OC threshold voltage causing the driver to detect and report a short circuit condition.

## UCC217xx OC-pin (UCC21710/32/36/39): Short circuit / overcurrent detection timing

$$t_{TOTAL\ DETECTION} = t_{BLK} + t_{OC\_FIL}$$

$$t_{BLK} = -\frac{R1+R2}{R1+R2+R3} * R3 * CBLK * \ln(1 - \frac{R1+R2+R3}{R3} * \frac{V_{oc}}{VDD})$$

- **Internal timing parameter**
  - $t_{\text{OCFIL}}$
- **Adjustable timing parameter**
  - $t_{\text{BLK}}$
- **Higher timing flexibility with only  $t_{\text{OCFIL}}$  and adjustable  $t_{\text{BLK}}$**



### TI Information – Selective Disclosure



**TEXAS INSTRUMENTS**

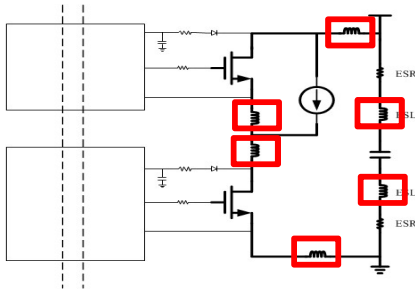
Looking into the detection timing, just like the previous example with the DESAT-pin the longest it will take the gate driver to detect a short circuit condition and shutdown a SiC MOSFET or IGBT is when it turns ON into a short circuit condition. With the OC-pin function when turning ON into a short circuit condition the total detection time is broken down into two timers; the blanking time, and the OC deglitch filter. There is no leading edge blanking time as the current source is generated from an external bias voltage.

Just like in the DESAT-pin function example, the blanking time can be configured through proper sizing of the blanking capacitor. During the blanking time the blanking capacitor will charge up to the internal OC threshold voltage.

The second timer is the internal OC deglitch filter. The blanking capacitor voltage must be greater than the internal OC threshold voltage for longer than the OC deglitch filter for the gate driver to report a short circuit condition. Just like for the DESAT-pin function the OC delight filter timer prevents the gate driver from reporting a short circuit condition in the case there are short voltage spikes on the OC-pin due to noise in the system.

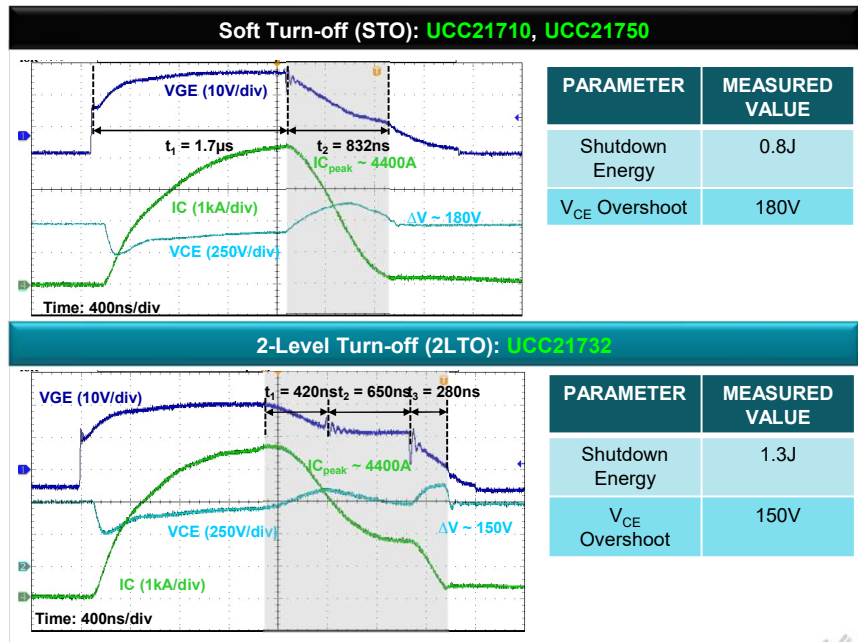
Due to not having the leading edge blanking time that the DESAT-pin function has the OC-pin function can be configured to have a faster detection time that can be beneficial when driving SiC MOSFETs.

## Soft turn-off (STO) & 2-level turn-Off



- Parasitic inductances in the power loop paired with  $di/dt$  cause voltage spikes
- $di/dt$  rate is much higher under short circuit fault
- There are two ways to slow down the turn-off process
  - Extend  $dt$ 
    - Soft turn-off
  - Reduce  $di$ 
    - 2-level turn-off

TI Information – Selective Disclosure



In any design there will be parasitic inductances in the power loop. Parasitic inductances in the power loop paired with  $di/dt$  cause voltage spikes. During a short circuit condition the  $di/dt$  rate can be very high that preventive measures must be taken to limit the overshoot voltage of the SiC MOSFET or IGBT to prevent damaging these components. Effectively, there are two ways to limit the overshoot during the turn-off process: reduce  $di$  or extend  $dt$ .

Soft turn off will extend the turn off time with a current source that is generated inside of the gate driver to slowly discharge the SiC MOSFET or IGBT to reduce the  $di/dt$ .

Two level turn off will reduce the change in current by distributing the turn off current between the first turn off and second turn off times.

# A design aid for DESAT / OC Detection

- Our [UCC217xx calculator](#) can accelerate and inform the design of SC protection!

## Functions include:

- Driver thermals
- Drive Current
- Shutdown time
- DESAT & OC-as-DESAT
- Soft turn-off



SUPPORT SOFTWARE

UCC217xx XL Calculator Tool

SLUC695.ZIP (1108 KB)

TI Information – Selective Disclosure

**TEXAS INSTRUMENTS** UCC217xx Calculator: Soft Turn-Off

**TEXAS INSTRUMENTS** UCC217xx Calculator: Switch Shutdown

**TEXAS INSTRUMENTS** UCC217xx Calculator: DESAT

**TEXAS INSTRUMENTS** UCC217xx Calculator: OC (Over-Current)

How to use this calculator:

- 1) Input system information in User Input (parameter descriptions are shown under Definitions).
- 2) Driver parameters from the datasheet are given in the Fixed Value section.
- 3) See Calculator Output for OC calculations based on the System and Driver Parameter values.

Note: OC configuration is only available with UCC21732 and UCC21710.

| User Inputs       |      |       |      |     |   |      |
|-------------------|------|-------|------|-----|---|------|
| System Parameters |      |       |      |     |   |      |
| VDD               | R1   | R2    | R3   | Vfw | n | CBLK |
| (V)               | (Ω)  | (Ω)   | (Ω)  | (V) |   | (nF) |
| 20                | 5600 | 15000 | 1650 | 2   | 1 | 0.22 |

| Parameter | Definition   |
|-----------|--|
| VDD       | Positive drive voltage                                       |
| RDESAT    | Resistor in series with HV blocking diode to limit current   |
| R1        | Resistor to set blanking capacitor charge current            |
| R2        | Part of resistor divider to control DESAT threshold voltage  |
| R3        | Part of resistor divider to control DESAT threshold voltage  |
| Vfw       | Forward voltage drop across HV blocking diode                |
| n         | Number of HV blocking diodes in series                       |
| CBLK      | Capacitor to set blanking time (C1 in equation)              |
| VOCTH     | Internal OC detection threshold voltage                      |
| VOCDT     | Actual detection voltage considering all external components |
| tBLK      | Blanking time before DESAT detection                         |

| Fixed Value | Driver Parameters |
|-------------|-------------------|
| VOCTH       | (V)               |
| 0.7         |                   |

| Calculate |
|-----------|
| VOCDT     |
| (V)       |
| 5.06      |

UCC21732/10



TEXAS INSTRUMENTS

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## Contact

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