PCB layout case study for automotive DC/DC

LM25141-Q1 5V, 15A, 2.1MHz buck regulator design with 93%+ efficiency

July 5, 2022

T. Hegarty, APP-BSR-WV

LM25141-Q1 controller layout design

Optimized for efficiency, EMI and thermal performance

LM25141-Q1 5V, 15A, 2.1MHz

Key Specs: 5.5V–36V input, 5V @ 15A output, 2.1MHz **Device: LM25141-Q1**

Features

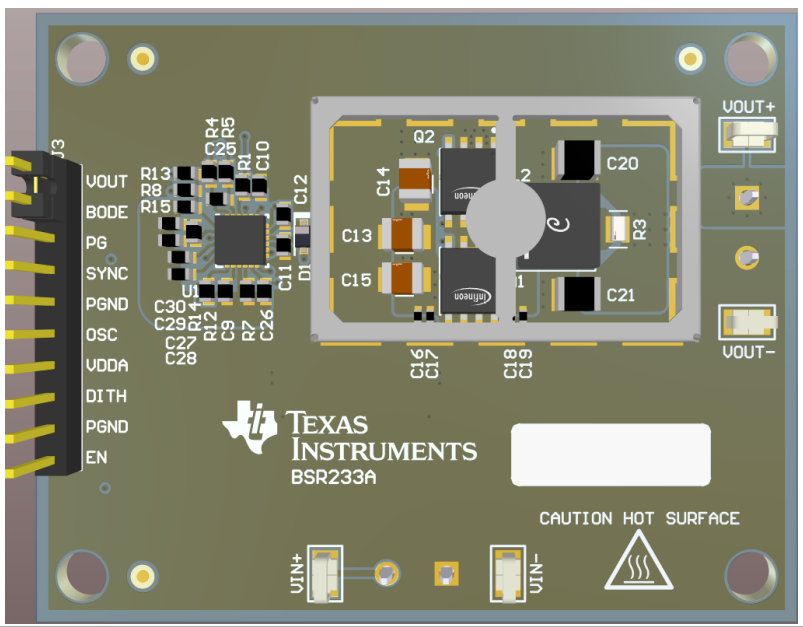
- **Wide 5.5V to 36V input range, 5V @ 15A single output**
- 15A output current with **93.3%** efficiency
- F_{SW} = **2.1MHz** (fixed), synchronizable –50% to +20%
- DITH pin for spread spectrum modulation
- 6-layer PCB; terminal blocks for VIN, VOUT, GND

Applications

- Down convert 12V automotive battery to high-current 5V / 3.3V rails
- Manage automotive input transients, including ISO 1675-2 and ISO 7637-2
- Meet **CISPR 25 Class 5** EMI requirements for conducted and radiated emissions
- Provide optimized thermal performance and high useable power at elevated ambient temperature operation

Supported Functions

- High conversion efficiency – 94% @ 12Vin, 10Aout
- 5V gate drive rail, up to 5.5V with external VCCX connected
- **SYNC IN** connections; choose CCM/DCM
- Almost **100% duty cycle** capability for low dropout
- Low $t_{ON(min)}$, $t_{OFF(min)}$ of **65ns, 60ns** for $0.6V \leq V_{OUT} < V_{IN}$

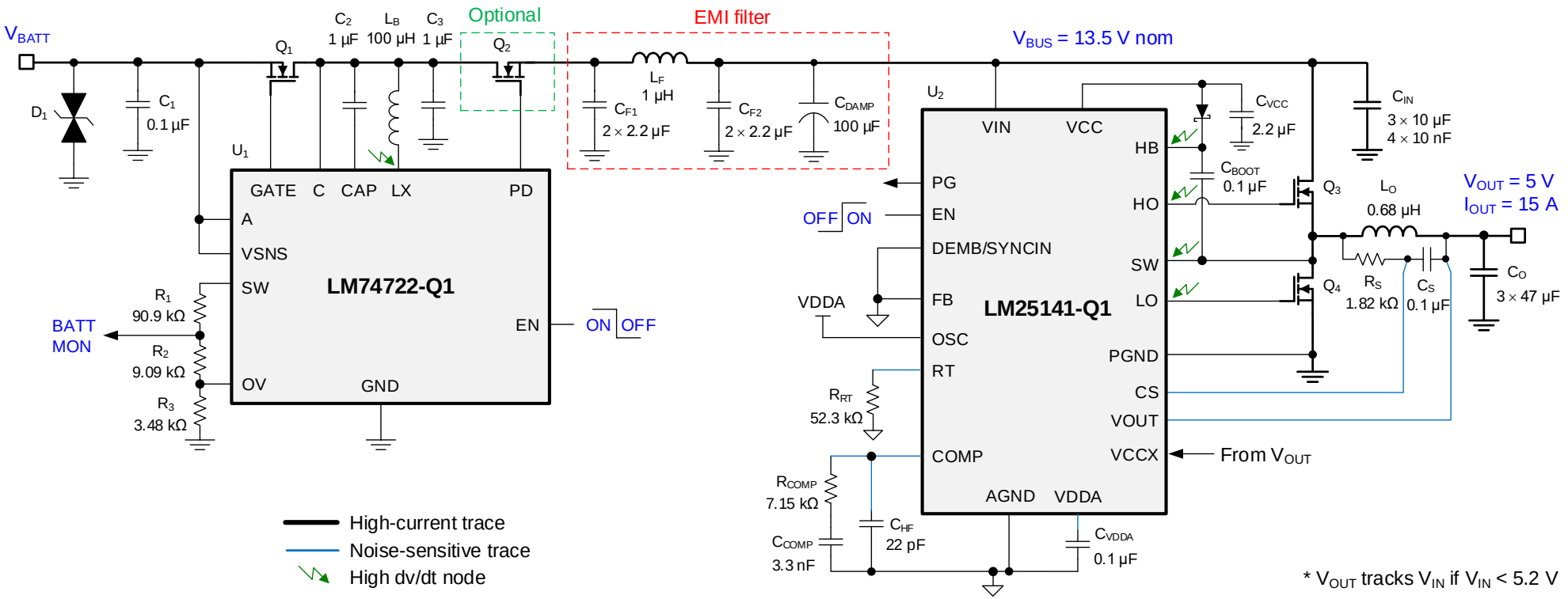


Available: Schematic, BOM, PCB source files, quickstart tool

TEXAS INSTRUMENTS

LM25141-Q1 42V single-phase sync buck controller

EMI mitigation features: SYNC In, FPWM/DEM, spread spectrum, adjustable gate drive

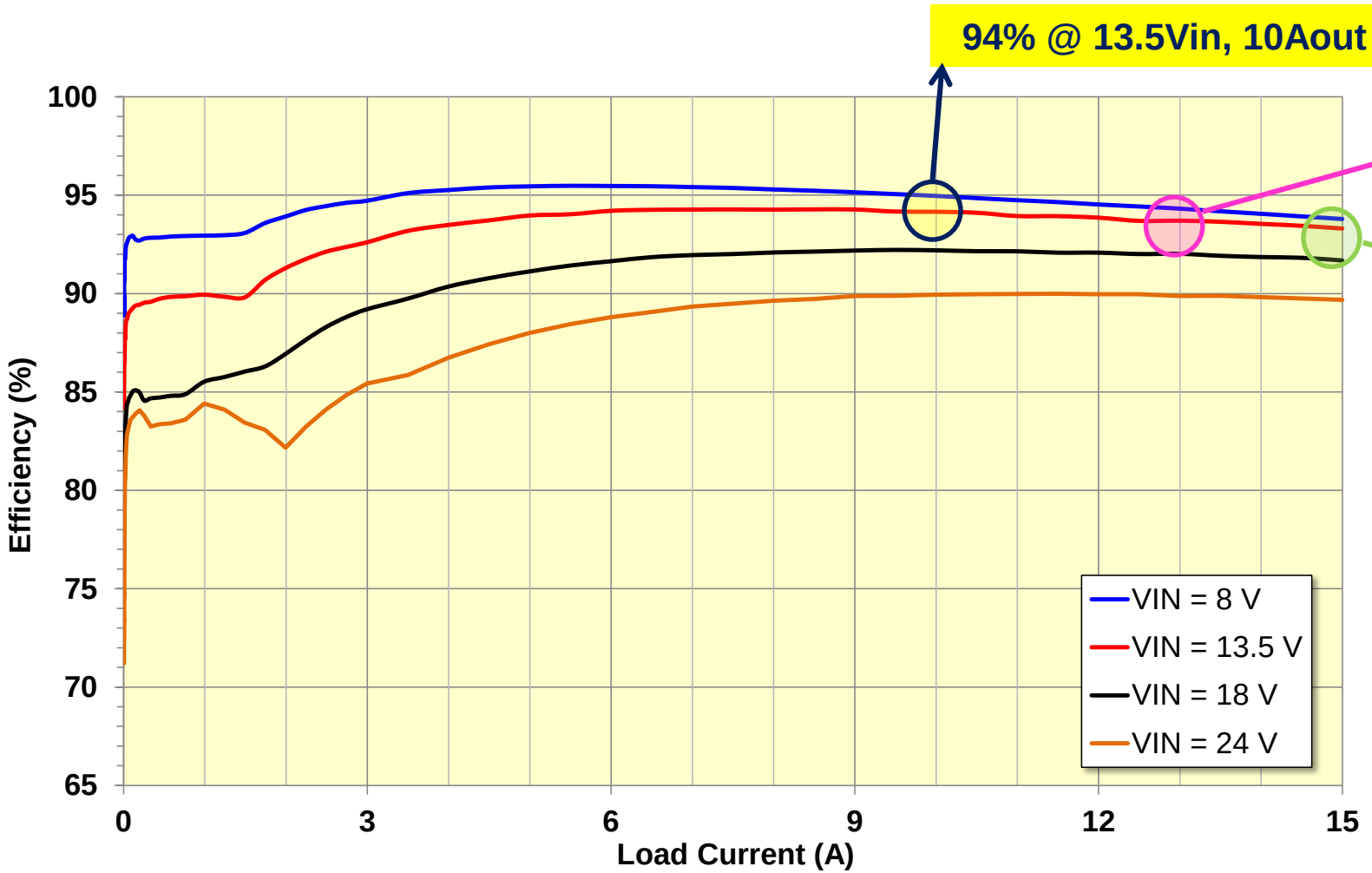


Identify:

High di/dt loops, high dv/dt surfaces, noise-sensitive traces

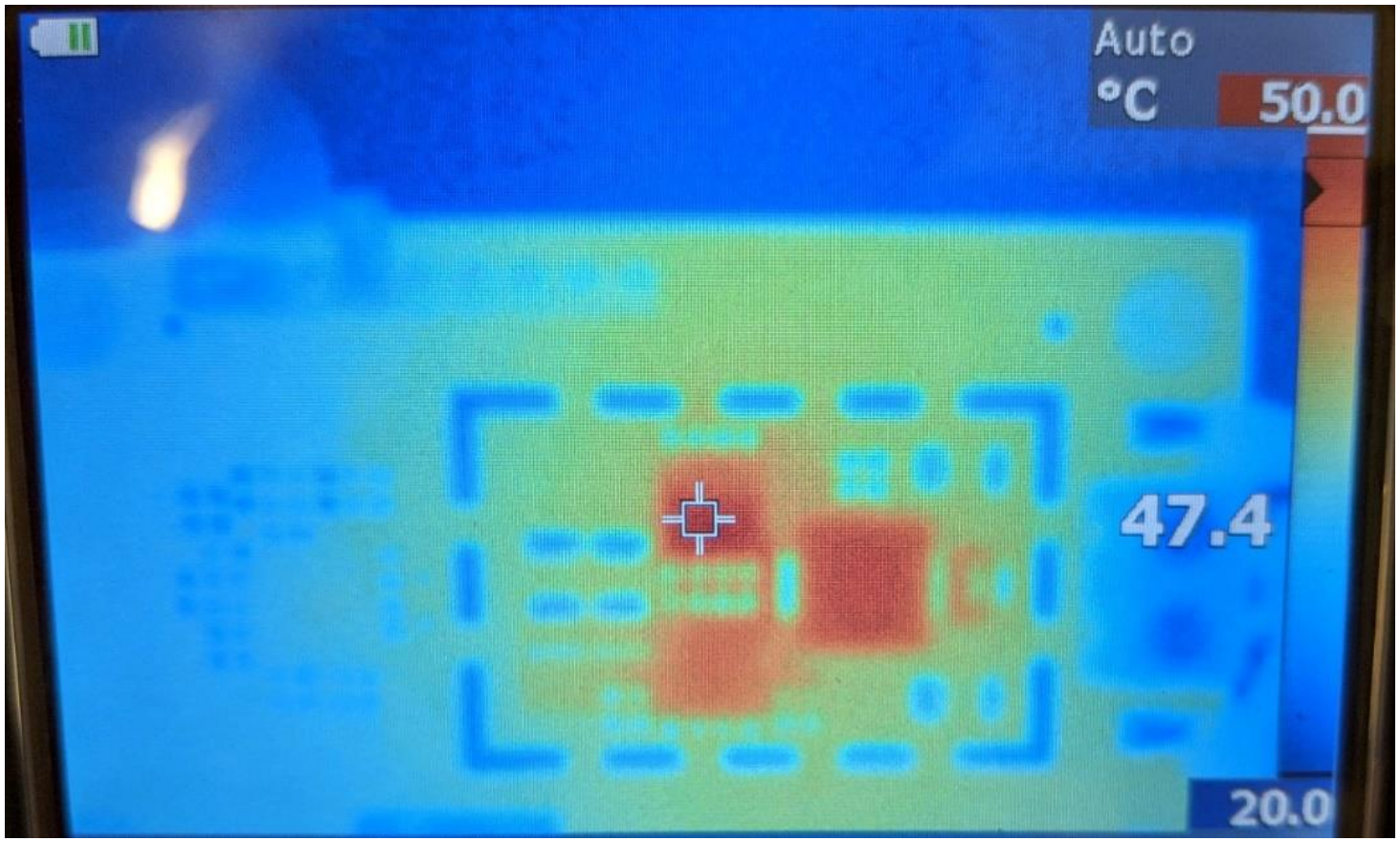
Note: LM74722-Q1 front-end protection circuit not included on PCB – shown here just for reference

Efficiency performance vs. I_{OUT} & V_{IN}, V_{OUT} = 5V (CCM)

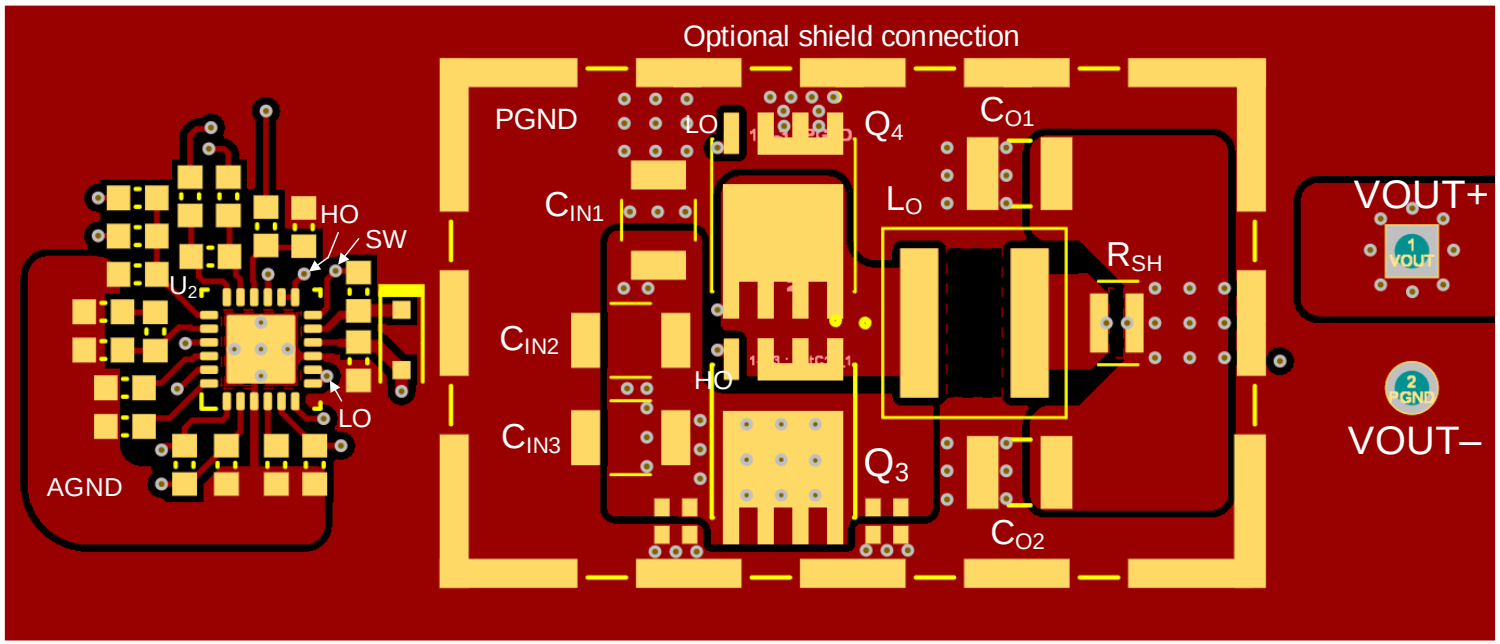


Note: efficiency increased by 0.7–1% by changing from Infineon OptiMOS5 to OptiMOS6 FETs. This data uses DCR current sensing

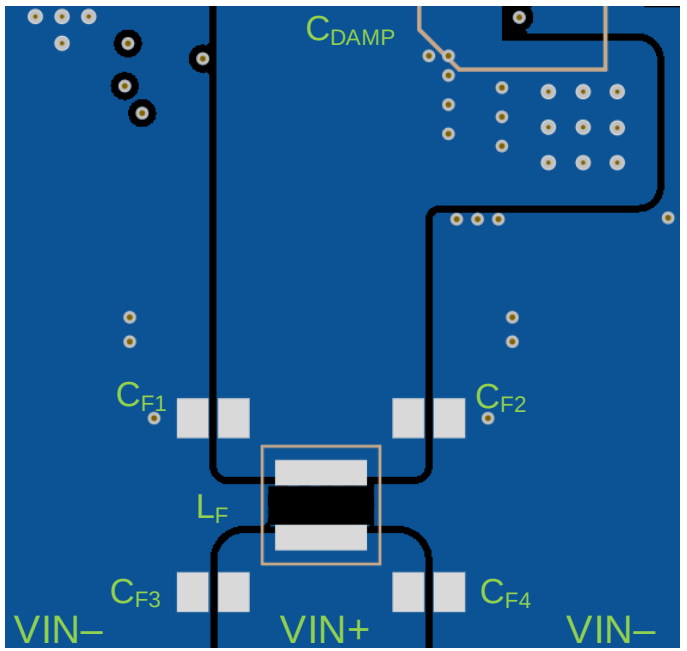
Thermal performance, V_{IN} = 12V, V_{OUT} = 5V, I_{OUT} = 8A



LM25141-Q1 layout – power stage (a), EMI filter (b)

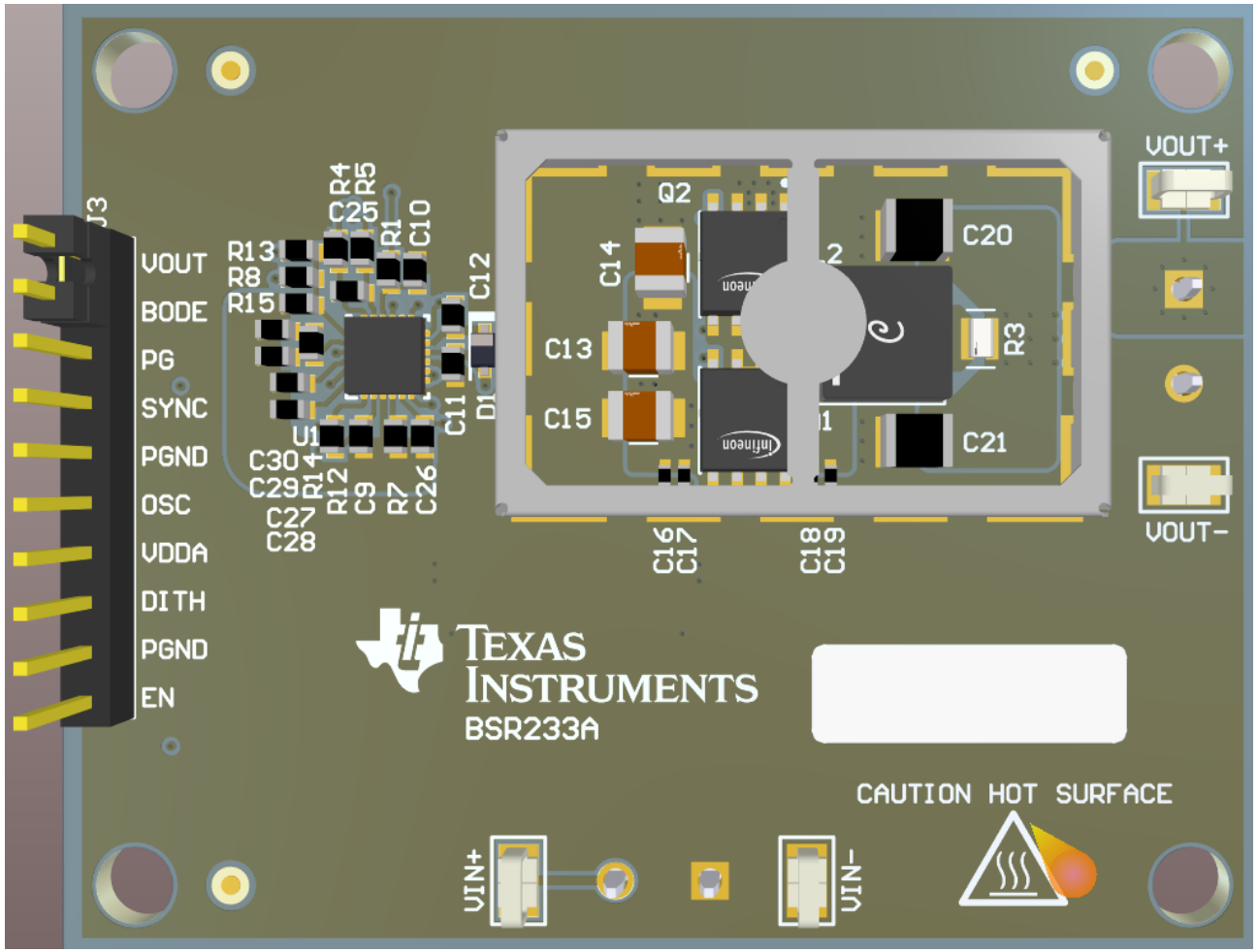


(a)



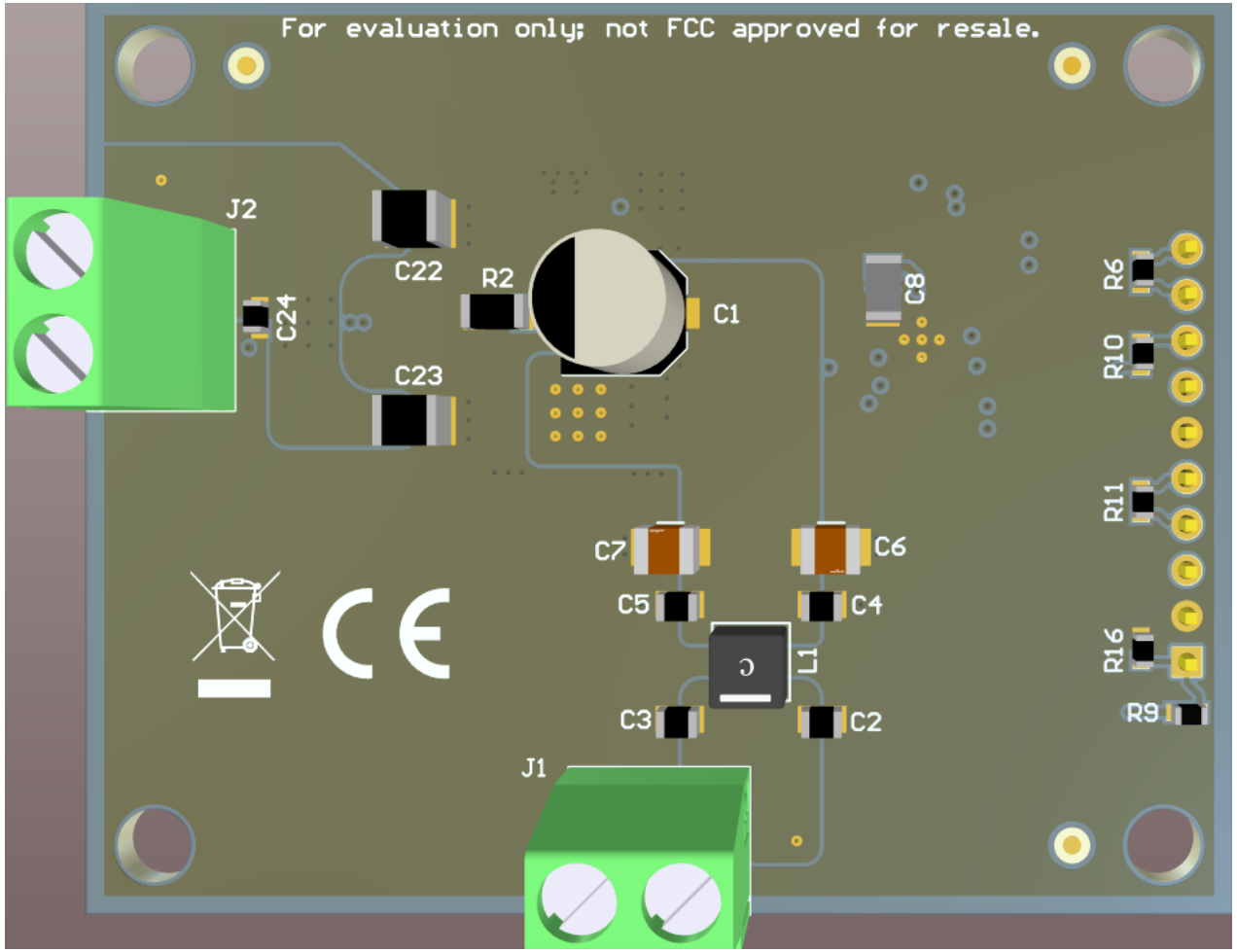
(b)

LM25141-Q1 layout – top 3D



1. High-density layout design
2. Power-stage EMI shield (6mm tall)
3. High-current input and output studs
4. 5 x 6mm FET packages, 6 × 6 × 3mm inductor, 0508 low-inductance shunt
5. Optional DCR current sensing eliminates shunt power loss
   - $P_{SHUNT} = 15A^2 \times 4m\Omega = 0.9W$
6. Multi-pin header connector for easy signal attachment and measurement

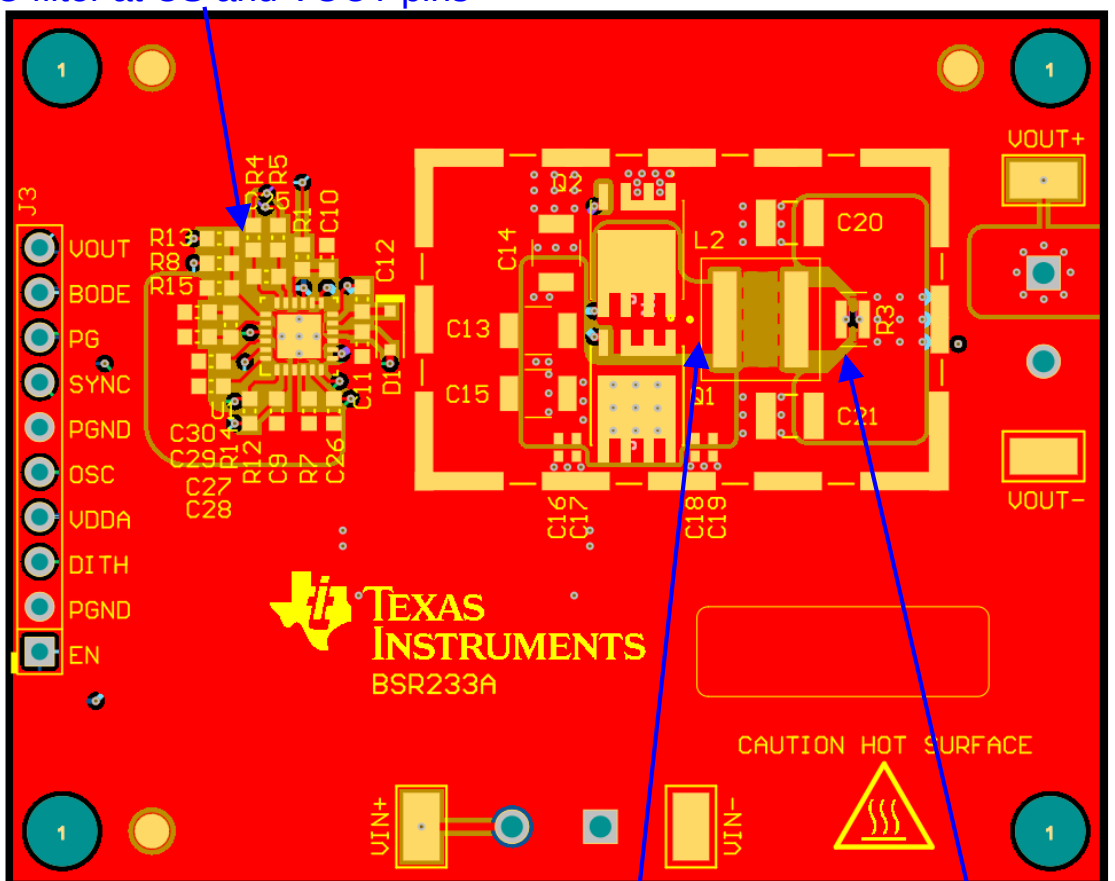
LM25141-Q1 layout – bottom 3D



1. EMI filter is a single-stage π-filter with electrolytic cap for parallel damping
2. No common-mode choke or ferrite beads
3. Small filter inductor (1µH) has high SRF
4. Filter caps C2-C5 laid out in butterfly arrangement around the filter inductor

LM25141-Q1 layout – top layer Cu

RC filter at CS and VOUT pins



Use min SW copper area

CS vias located at center of shunt pads

1. Ground pads included for optional EMI shield

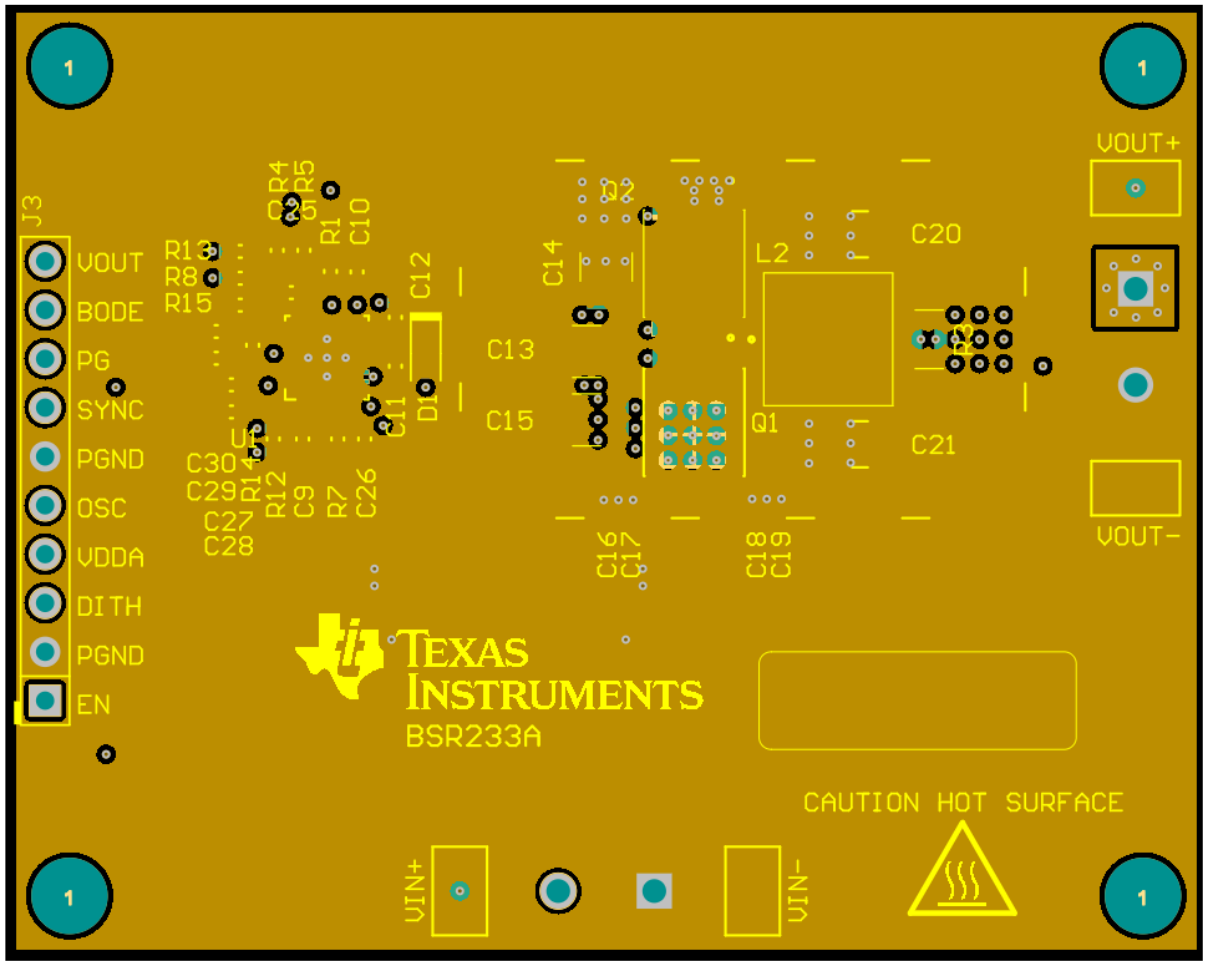
   ⇒ good for radiated EMI attenuation above 10MHz

2. Keep controller close to power MOSFETs

   ⇒ short gate drive traces for low parasitic inductance

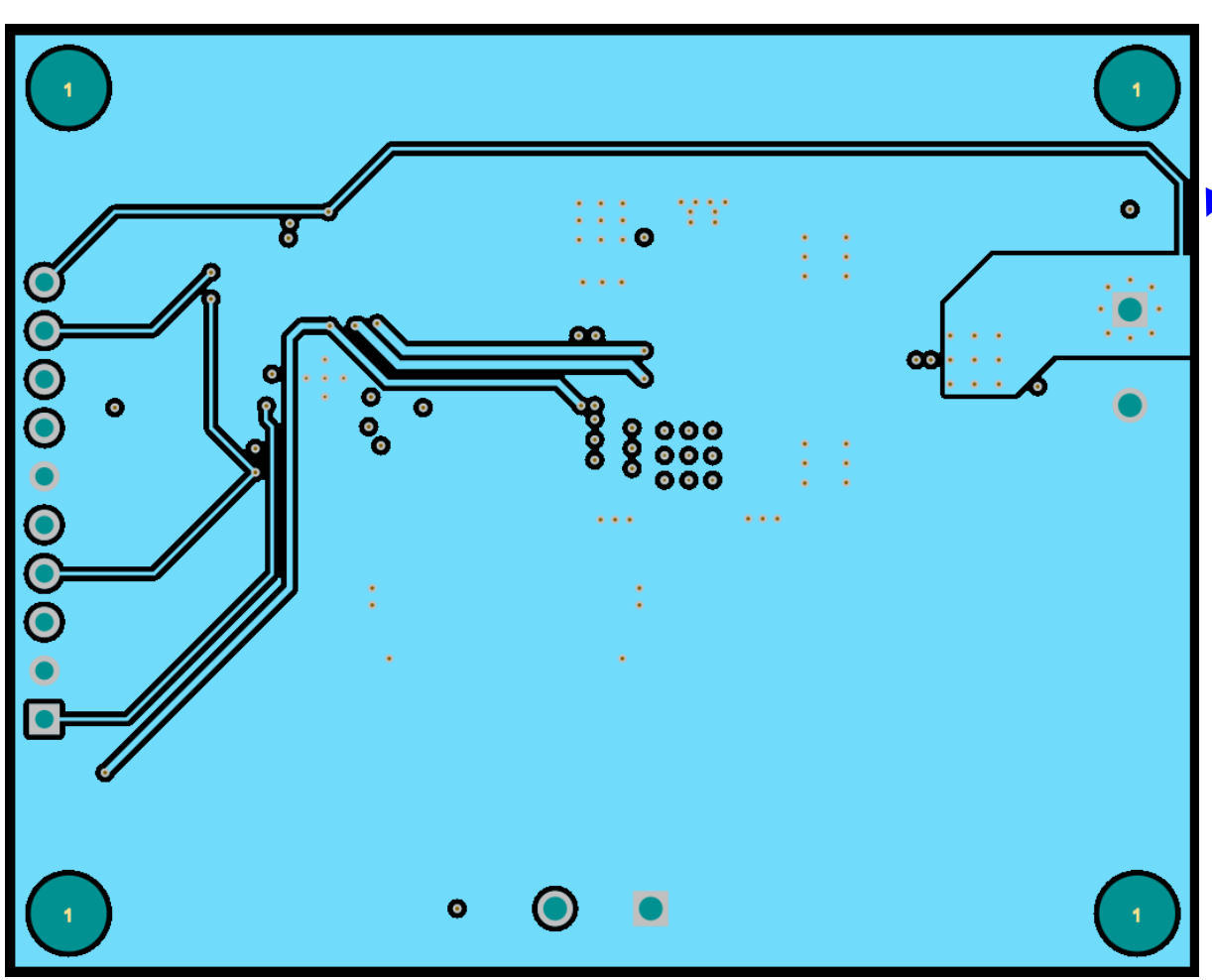
3. Consider soldering power connectors from the bottom side as they act like pick-up antennas on the top, bypassing the EMI filter

LM25141-Q1 layout – L2 copper



1. Solid GND plane provides EMI shielding and heatsinking
2. Keep L2 close to top layer (i.e. tight 6-mil spacing in the PCB stackup)

LM25141-Q1 layout – L3 copper



1. Minimize **conductive (capacitive)** and **radiative (inductive)** coupling

   ⇒ gate driver should be close to MOSFETs

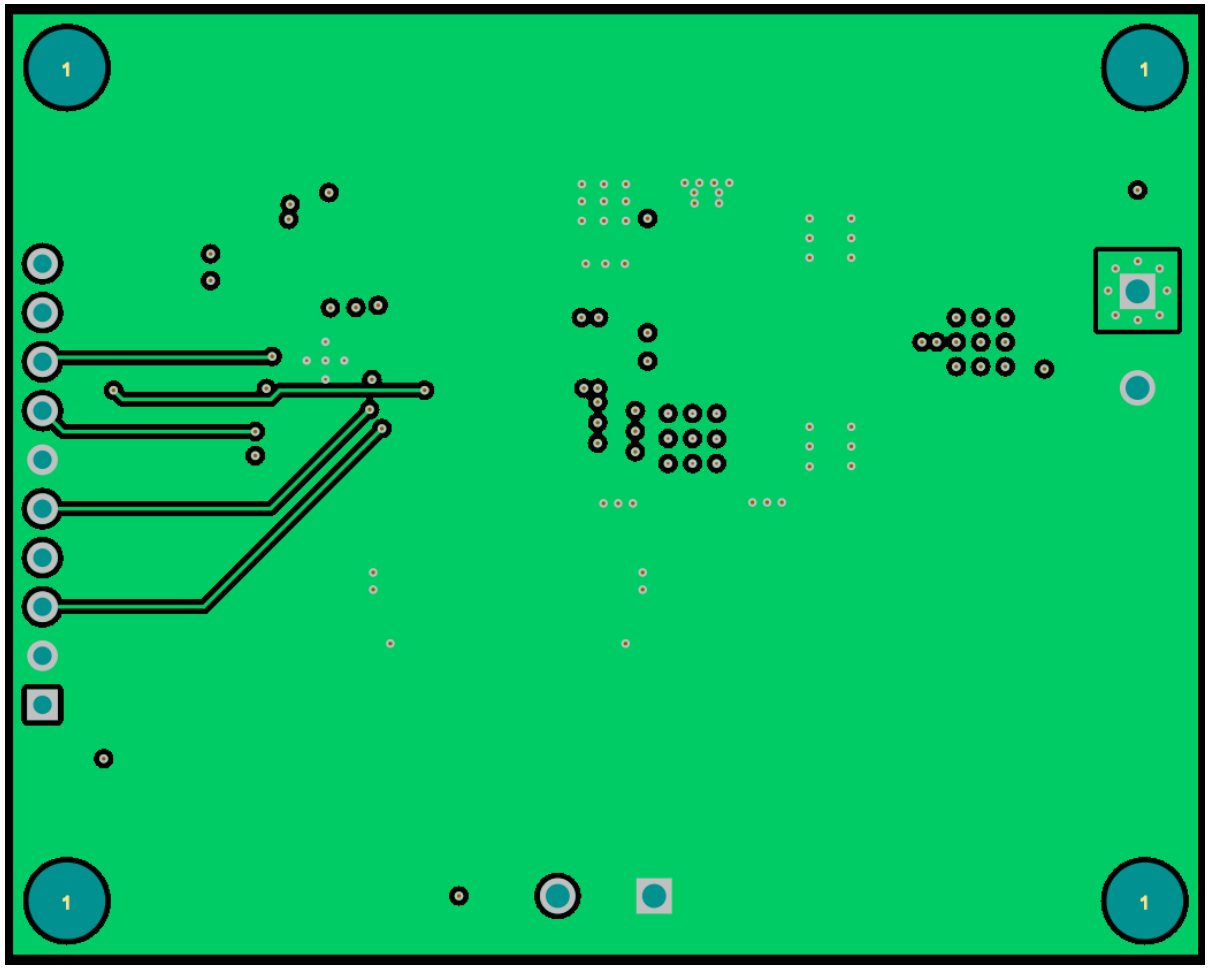
2. Route gate (HO) & source (SW) traces as a differential pair

   ⇒ minimizes gate loop inductance, giving faster switching & lower V_{GS} ringing

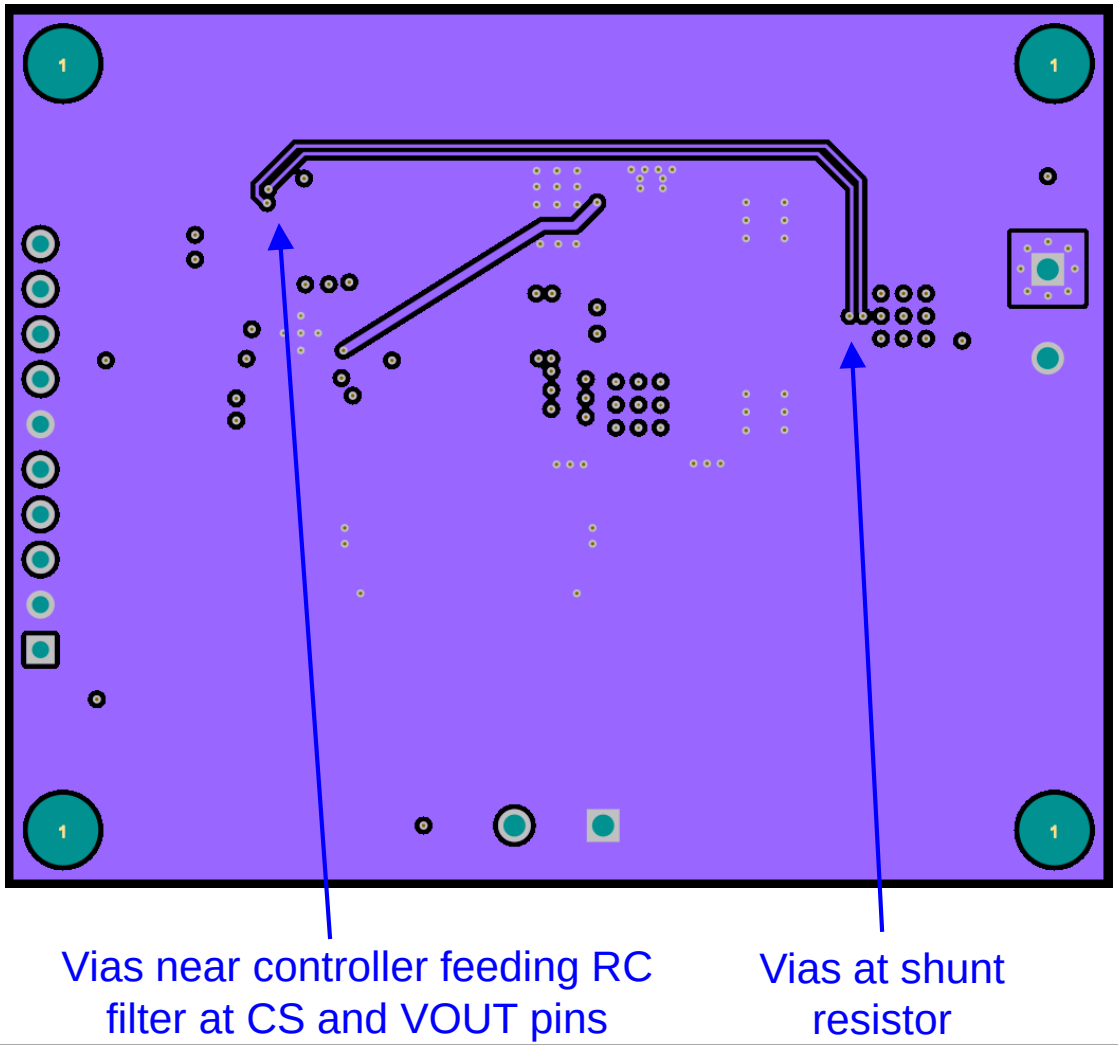
3. Orthogonal gate routing away from power loop reduces mutual coupling

4. VOUT connection is short and direct to the terminal block

LM25141-Q1 layout – L4 copper

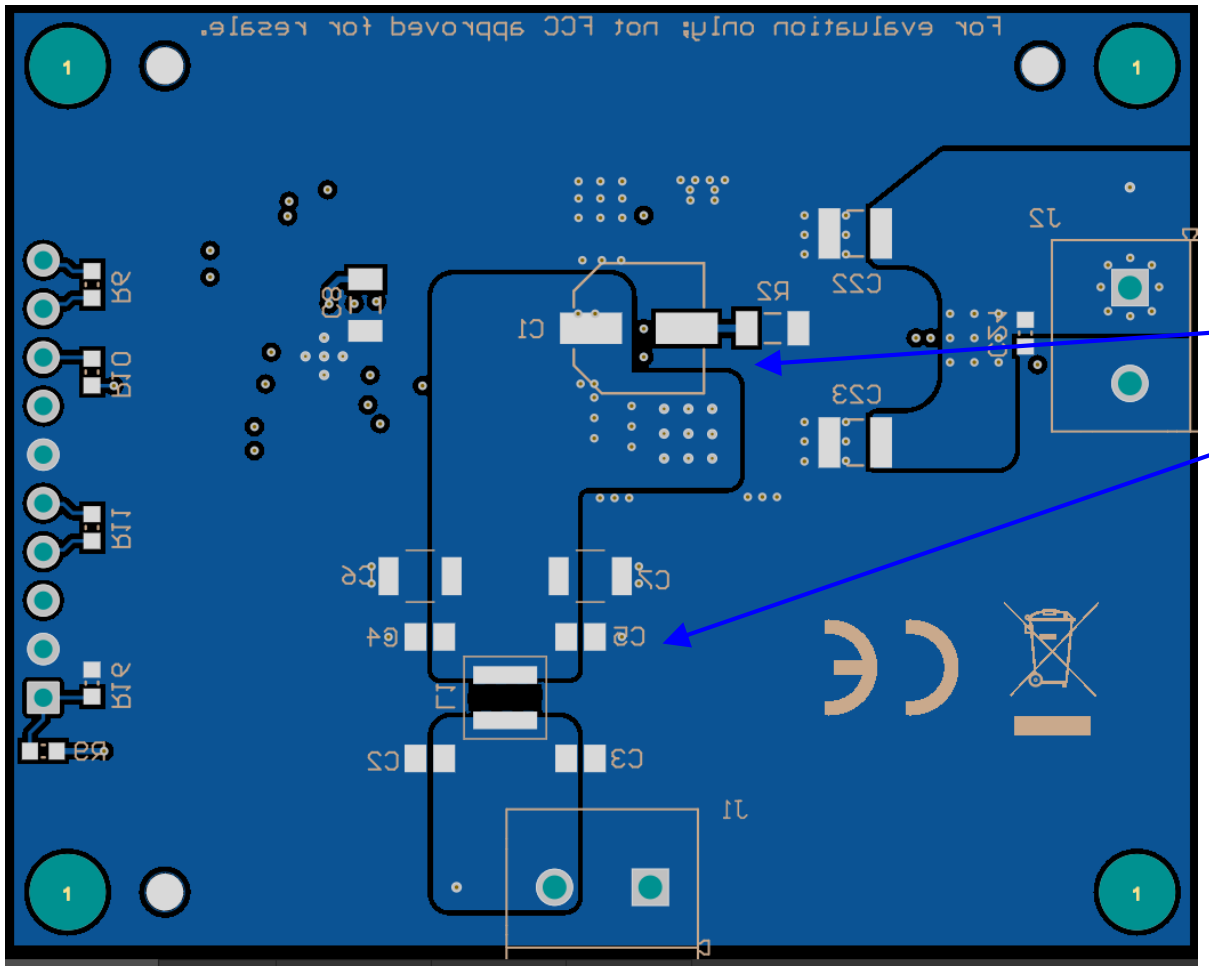


LM25141-Q1 layout – L5 copper



1. Current sense traces **routed differentially** from the shunt to the controller
2. Locate the CS filter at the IC pins (CS and VOUT)
3. **Keep CS traces away from SW copper and gate drive traces**
4. Narrow traces are mostly just connections to a terminal block for easy access

LM25141-Q1 layout – bottom layer copper



1. EMI filter on the bottom side avoids pick-up from SW node and inductor on the top
2. Use electrolytic cap for parallel damping
3. Butterfly layout of caps around the EMI filter inductor with GND plane keepout underneath

LM25141-Q1 layout – layer stack-up

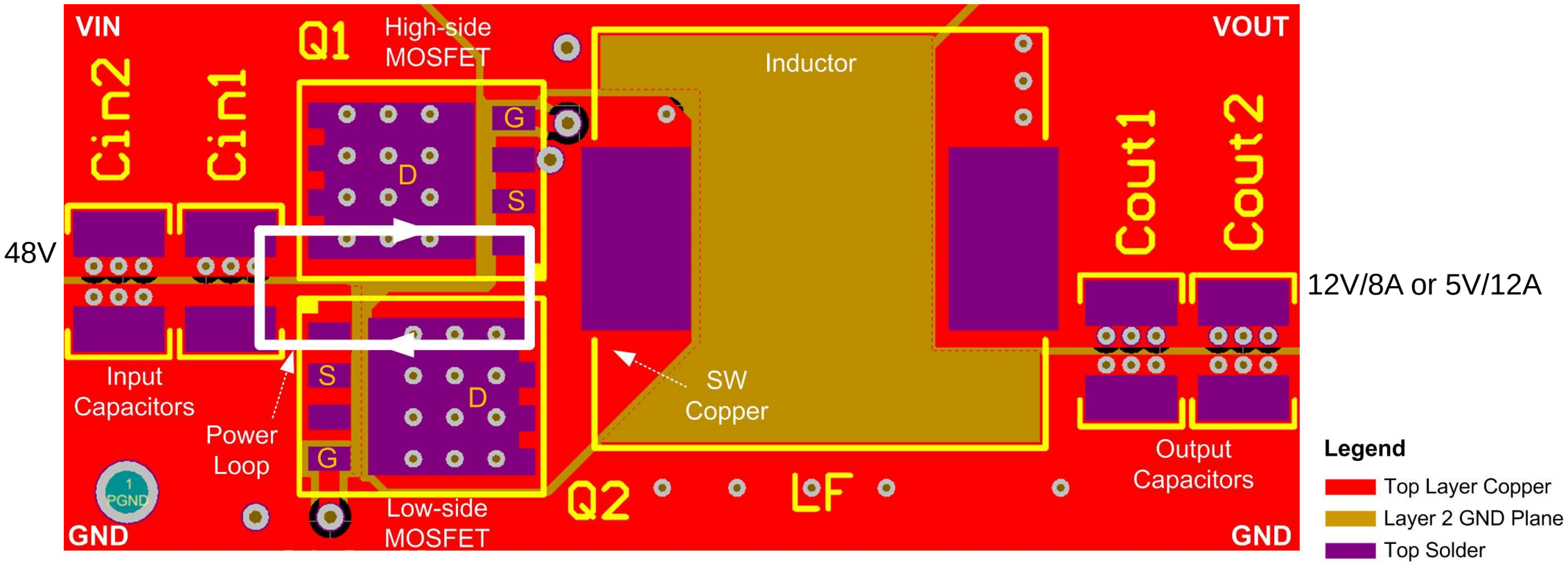
#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.4mil	3.5	
1	Top Layer		Signal	2oz	2.756mil		
	Dielectric1	FR-4 High Tg	Core		6mil	4.8	
2	Signal Layer 1		Signal	2oz	2.756mil		
	Dielectric2	FR-4 High Tg	Dielectric		10mil	4.8	
3	Signal Layer 2		Signal	2oz	2.756mil		
	Dielectric 3	FR-4 High Tg	Dielectric		12mil	4.8	
4	Signal Layer 3		Signal	2oz	2.756mil		
	Dielectric 4	FR-4 High Tg	Dielectric		10mil	4.8	
5	Signal Layer 4		Signal	2oz	2.756mil		
	Dielectric 5	FR-4 High Tg	Dielectric		6mil	4.8	
6	Bottom Layer		Signal	2oz	2.756mil		
	Bottom Solder	Solder Resist	Solder Mask		0.4mil	3.5	
	Bottom Overlay		Overlay				

Note: 2oz copper with 6-mil spacing from top layer (power stage components) to layer 2 GND plane

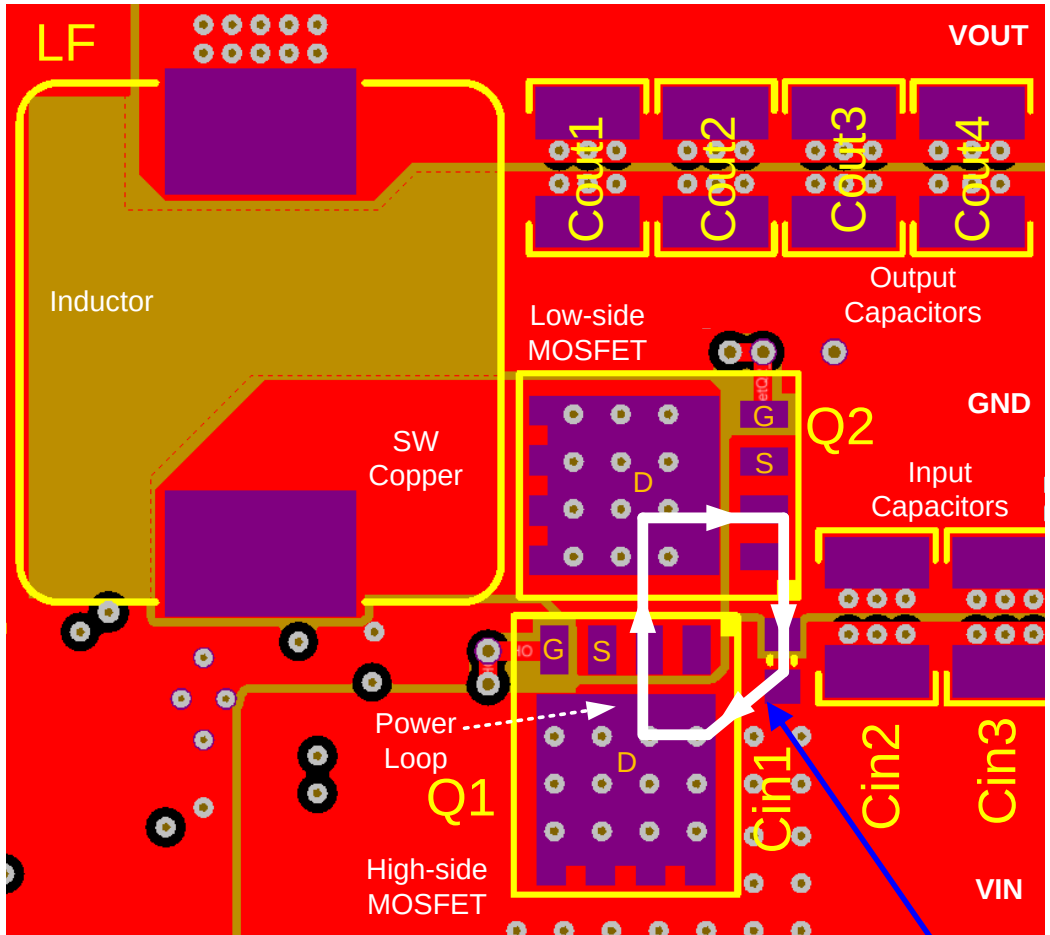
Buck controller layout and component selection theory

(Backup slides)

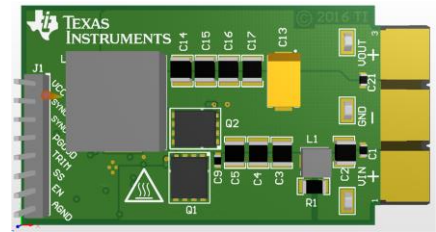
Buck controller PCB layout #1 (lateral loop)



Buck controller PCB layout #2 (lateral loop)



Layout modification

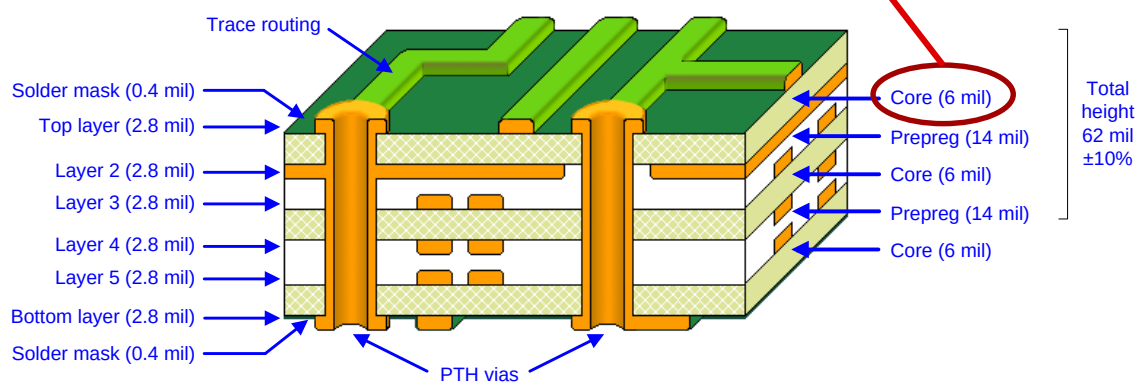


Rotate high-side MOSFET Q1 90°

Add **0603 input cap**, Cin1

- ✓ 10nF, 100V, 0603, X7R
- ✓ 77MHz SRF (self-resonant frequency)
- ✓ Smaller high-frequency power loop area

Specify PCB stack-up with **6-mil spacing** top layer to L2 GND plane

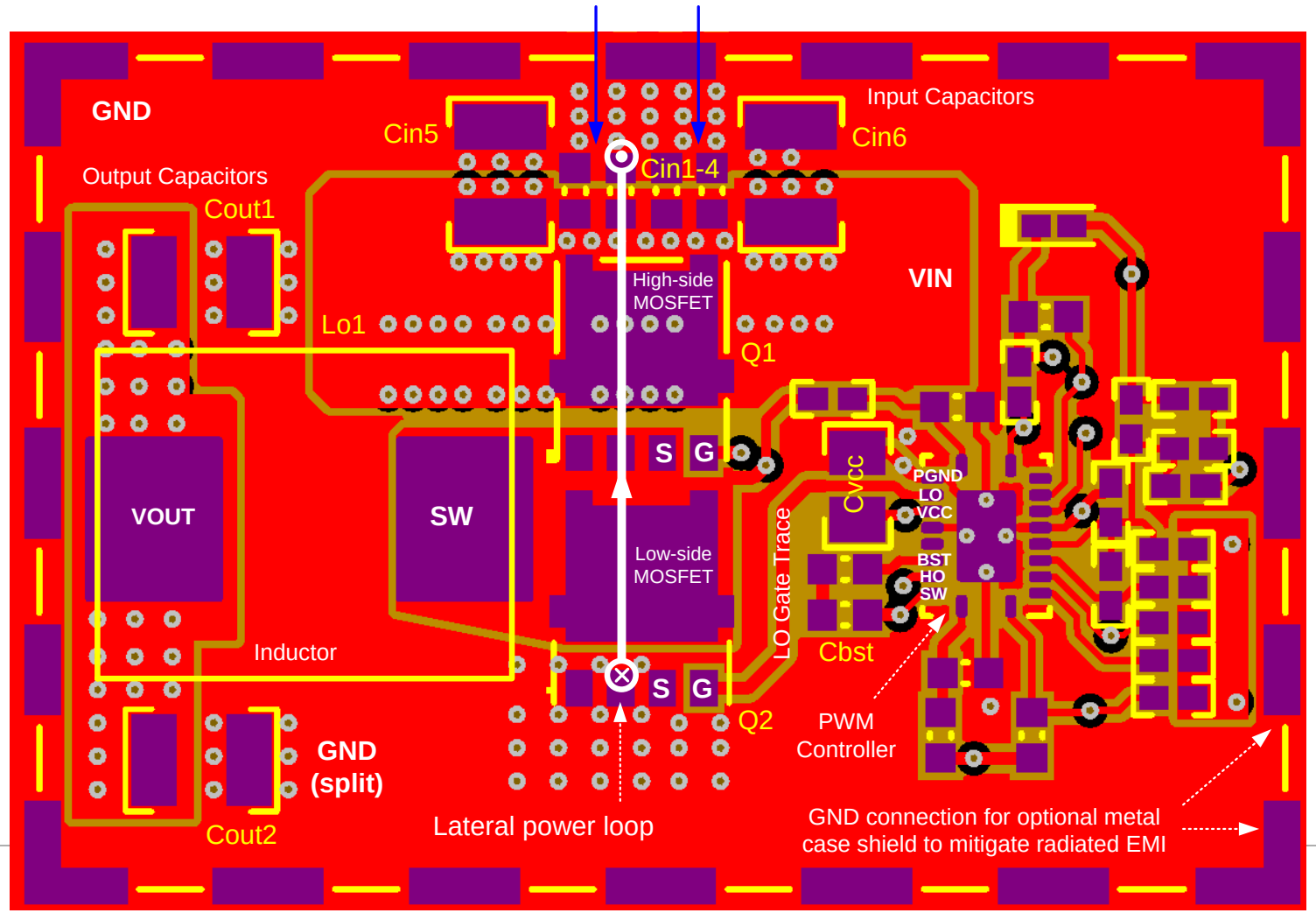


Legend Top Layer Copper | Layer 2 GND Plane | Top Solder

Cin1 = 10nF/100V/X7R/0603

Buck controller PCB layout #3 (vertical loop)

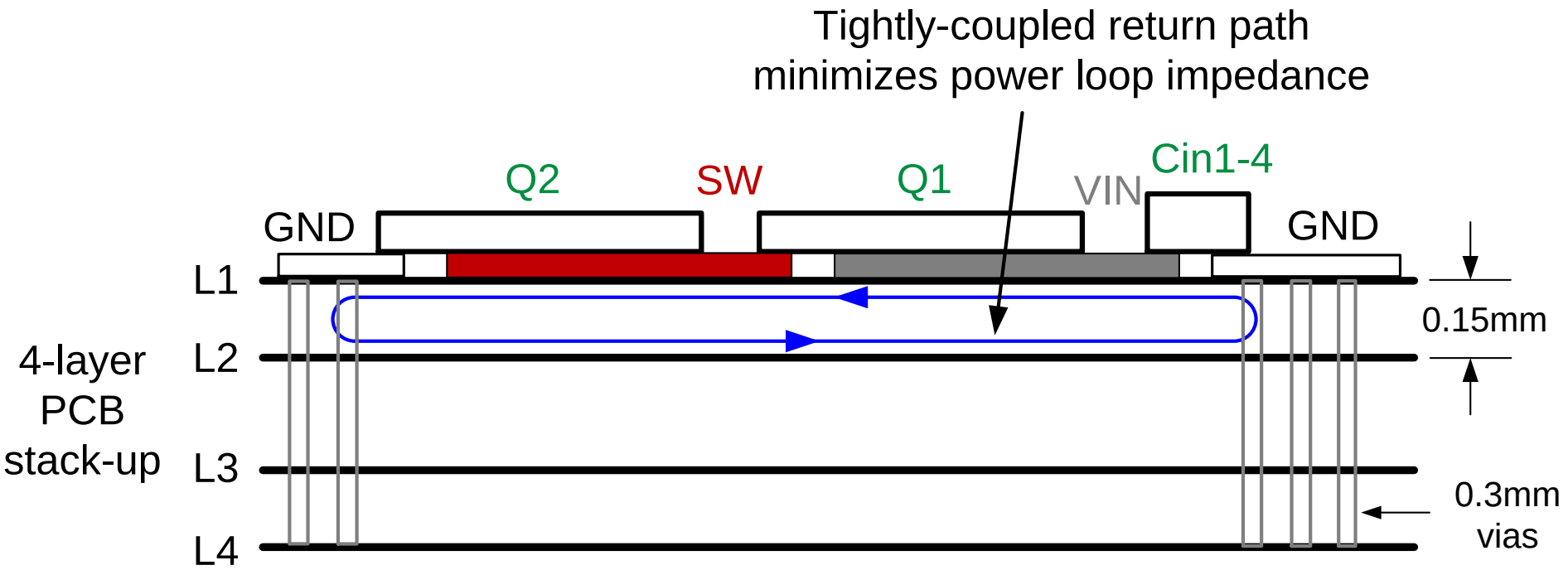
Four 0603 input decoupling capacitors in parallel provide low impedance at high frequency. Together with a tightly-coupled return plane on layer 2, the capacitors provide decoupling for high-frequency currents



Legend

- Top Layer Copper
- Layer 2 GND Plane
- Top Solder

Buck controller PCB layout #3 (side view)

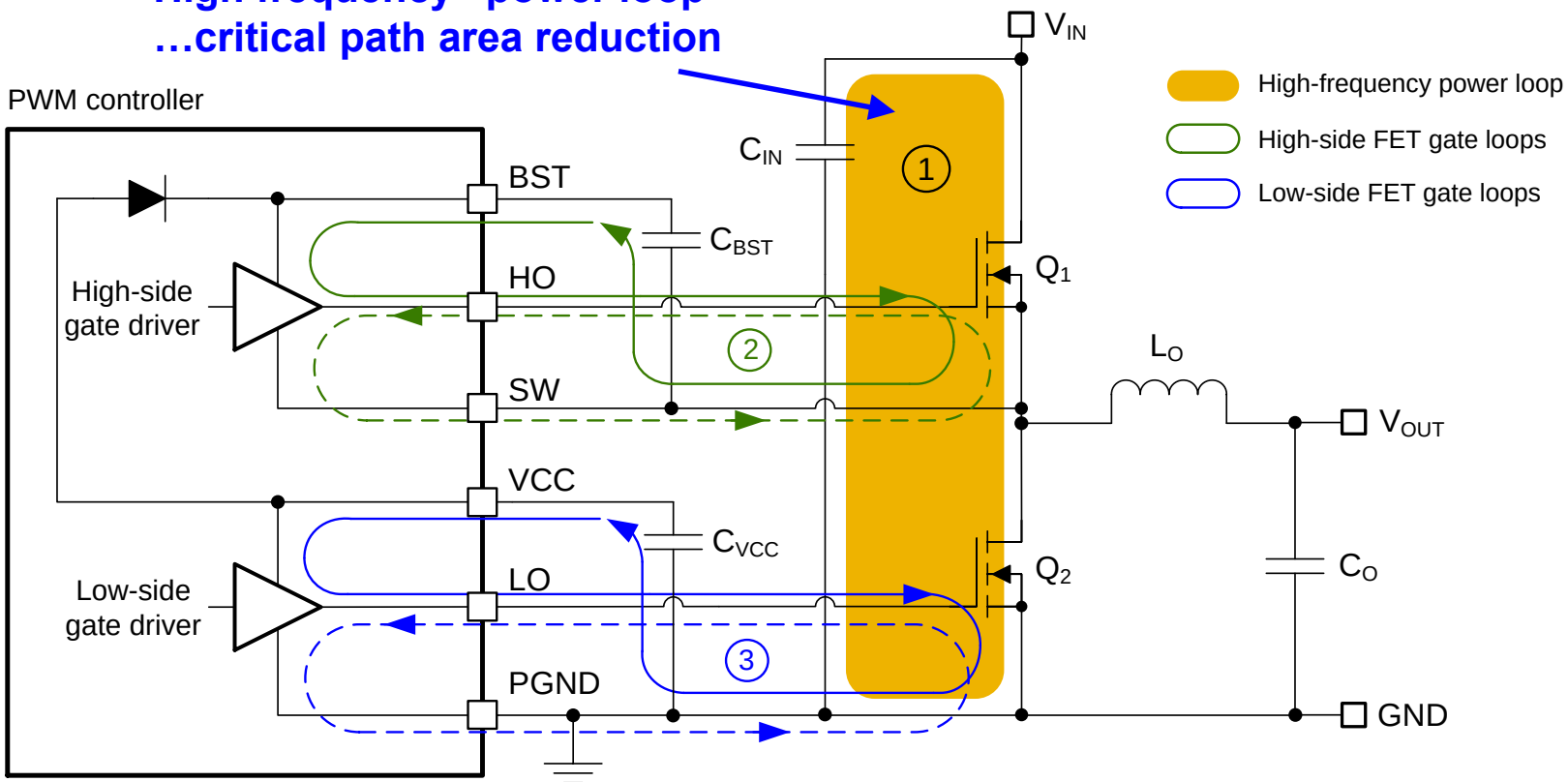


⇒ effective loop area reduced from **~20mm²** to **2mm²**

See **Tech Note** www.ti.com/lit/snva803

Identify critical loops with high di/dt currents

High frequency "power loop"
…critical path area reduction

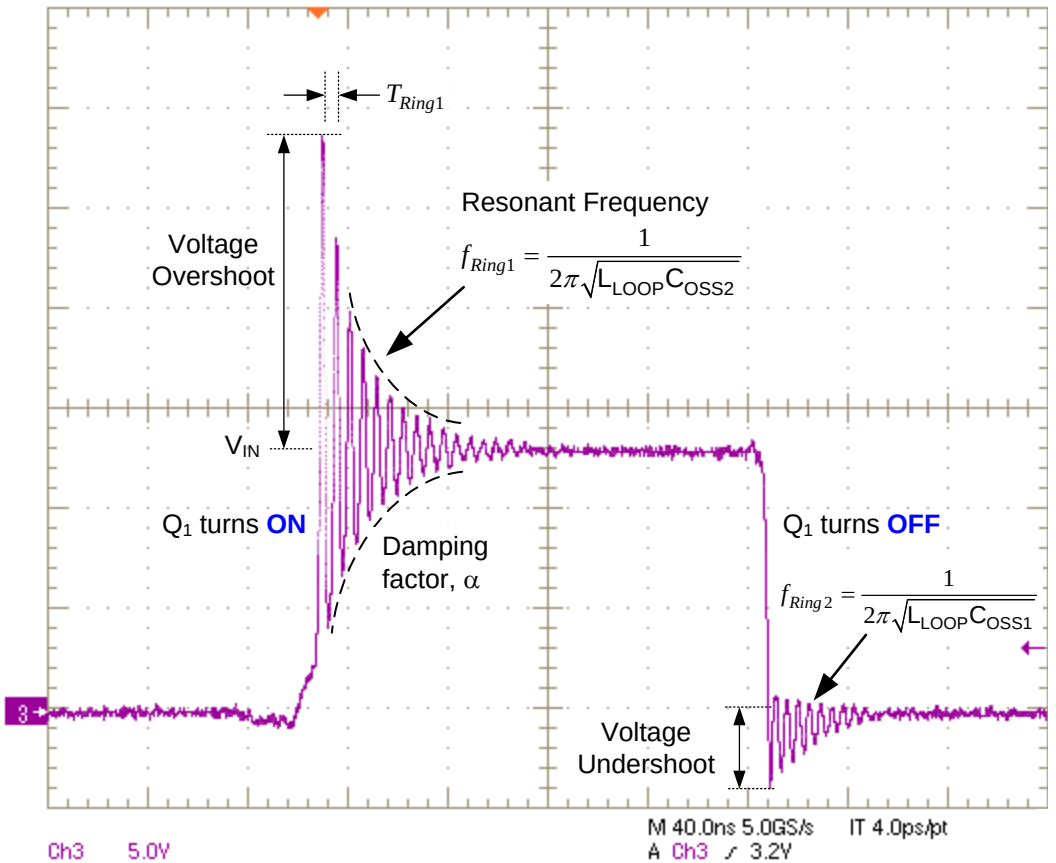


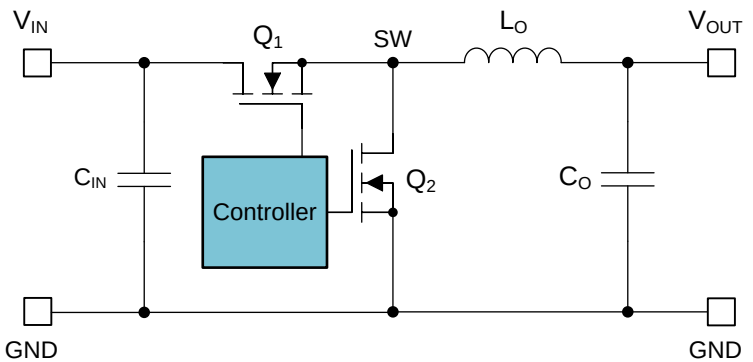
The current in the power loop with fast switching edges and leading-edge resonant ringing is rich in harmonic content, posing a severe threat of **magnetic field coupling** and radiated EMI

The **exposed** SW node and gate drive traces with fast switching edges pose a severe threat of **electric field coupling** (common-mode EMI)

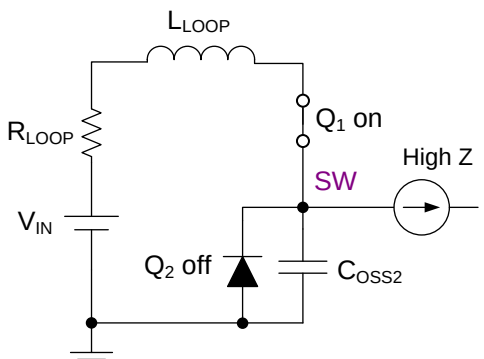
Essential to identify the high slew-rate current (**high di/dt**) **loops** to recognize the layout-induced **parasitic or stray inductances** that cause excessive **noise, overshoot, ringing and ground bounce**

Equivalent RLC circuits for SW node ringing – buck

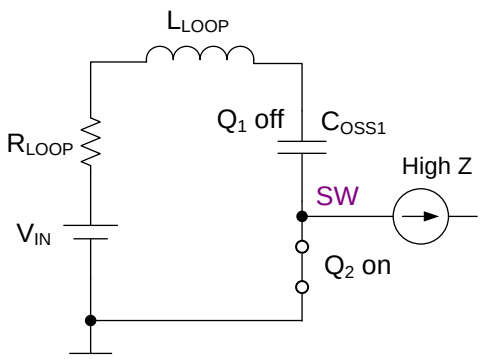




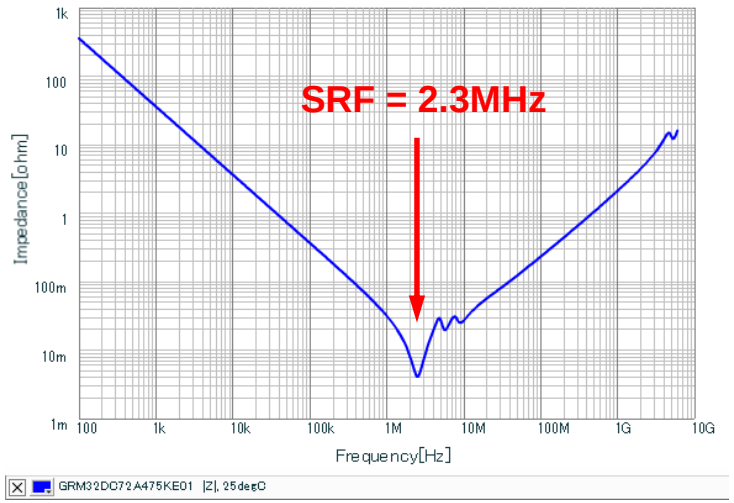
Equivalent RLC circuit after Q_1 turns **ON**

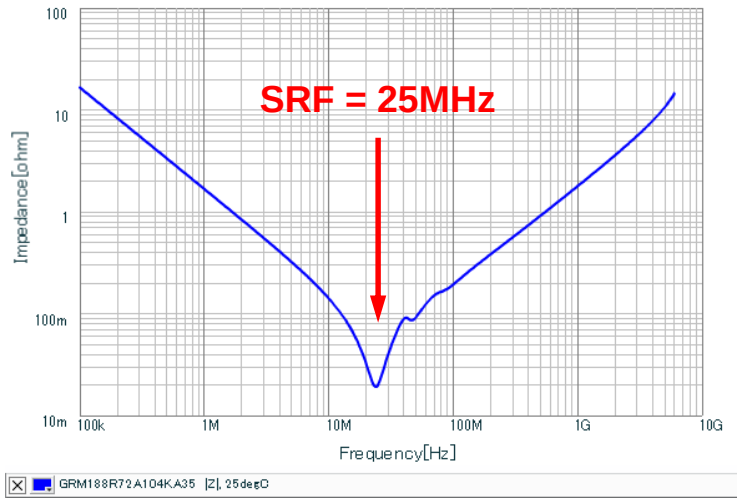


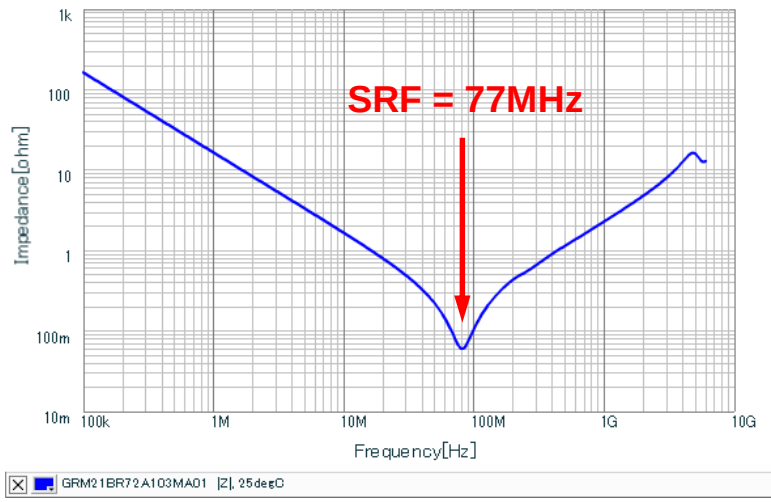
Equivalent RLC circuit after Q_1 turns **OFF**



Input caps: 4.7µF/1210, 100nF/0603, 10nF/0603







4.7µF, 100V, X7S, 1210 (1.5µF @ 48V)

SRF = **2.3MHz** (Z_C = 4mΩ)

ESL = 400pH

Z_C = **237mΩ** @ 100MHz

0.1µF, 100V, X7R, 0603

SRF = **25MHz** (Z_C = 20mΩ)

ESL = 350pH

Z_C = **195mΩ** @ 100MHz

10nF, 100V, X7R, 0603

SRF = **77MHz** (Z_C = 60mΩ)

ESL = 330pH

Z_C = **110mΩ** @ 100MHz

[Ref] Murata Simsurfing tool, http://ds.murata.co.jp/software/simsurfing/en-us/index.html

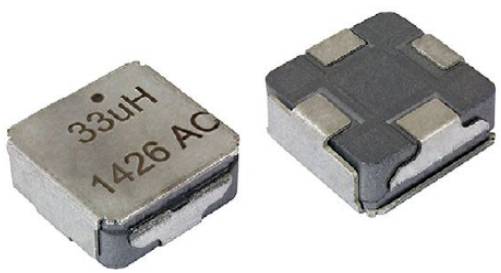
Inductors with improved e-field signature

VISHAY
www.vishay.com

IHLE-4040DD-5A

Vishay Dale

Low Profile, High Current Inductors with e-field Shield



Manufactured under one or more of the following:
US Patents; 6,198,375/6,204,744/6,449,829/6,460,244.
Several foreign patents, and other patents pending.

FEATURES

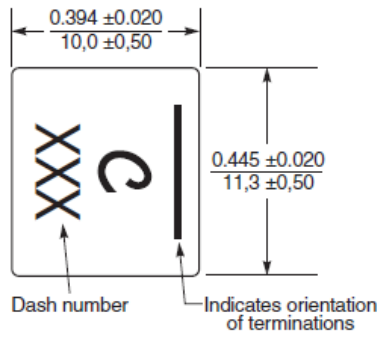
- High temperature, up to 155 °C
- Integrated E-Shield for maximum EMI reduction (1)
- Excellent DC/DC energy storage up to 1 MHz to 2 MHz. Filter inductor applications up the SRF (see Standard Electrical Specifications table).
- Integrated e-field shield eliminates need for separate shielding
- 20 dB e-field reduction at 1 cm
  - Measured vertically from top center of device
- Lowest DCR/µH, in this package size
- Handles high transient current spikes without saturation
- Coplanarity of the 4 terminals ≤ 100 µm
- AEC-Q200 qualified
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

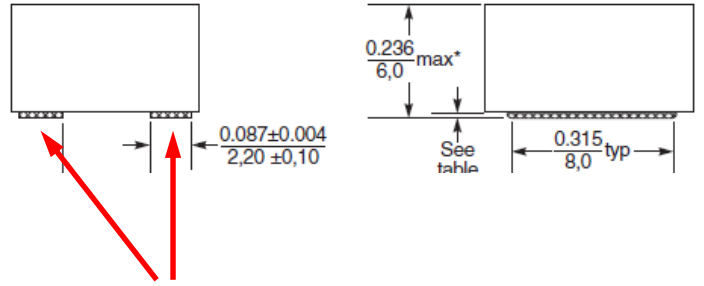
AUTOMOTIVE GRADE
Pb-free
RoHS COMPLIANT
HALOGEN FREE
GREEN (5-2008)

Note

(1) Maximum e-field reduction is realized with the IHLE shield is connected to ground.

Shielded Power Inductors – XAL1060





No vertical sidewall terminals (exposed metal) minimizes e-field coupling

Texas Instruments

PCB layout guidelines for buck controllers

Designing for lowest EMI

1. **Input & output caps**
   - Bypass VIN to GND with multiple low-ESR ceramic caps of X7R dielectric
   - Place C_{IN} as close as possible to the MOSFETs VIN and GND connections
   - Minimize the **loop area** formed by C_{IN} terminals and the MOSFETs
2. **Inductor**
   - Locate the inductor close to the MOSFETs (SW node) and connect **dotted terminal** to SW
   - Minimize the area of the SW trace/polygon to reduce **e-field coupling**
   - Connect dotted terminal of inductor (if provided) to SW – dot indicates inside of circular winding
3. **Ground plane**
   - Use **full copper ground plane on layer 2** immediately (**6 mils**) under the power stage
   - Provides H-field cancellation, parasitic inductance reduction & noise shielding, heat spreading
4. **Gate drives/current sense**
   - Route high-side gate drive traces as diff pair (HO and SW together)
   - Route gate drive traces short and direct, preferably on **inner PCB layer for shielding**
   - Route the **current sense traces** away from noisy nodes such as gate drives or SW node

Collateral

Content title	Content type	Link to content
The engineer's guide to EMI in DC/DC converters – parts 5 and 6	Article series	http://www.how2power.com/other/EMI_Guide.php
Reduce EMI and power loss in dual-battery automotive systems with optimized power-stage layout	Article	https://www.edn.com/design/power-management/4461773/4/Reduce-EMI-and-power-loss-in-dual-battery-automotive-systems-with-optimized-power-stage-layout
Improve high-current DC-DC regulator EMI performance for free with optimized power stage layout design	Tech Note	http://www.ti.com/lit/an/snva803/snva803.pdf
High-density PCB layout of DC/DC converters	Blog	http://e2e.ti.com/blogs_/b/powerhouse/archive/2015/09/11/high-density-pcb-layout-of-dc-dc-converters-part-1
How to do a PCB layout review	Blog	http://e2e.ti.com/blogs_/b/fullycharged/archive/2015/03/20/how-to-do-a-pcb-layout-review
Reduce buck converter EMI and voltage stress by minimizing inductive parasitics	ADJ app note	http://www.ti.com/lit/an/slyt682/slyt682.pdf

QUESTIONS


THANK
YOU
GRACIAS
ARIGATO
SHUKURIA
DANKSCHEEN
BÏYAN
SHUKRIA
TINGKI
YAQHANYELAY
TASHAKKUR ATU
SUKSAMA
EKHMET
MEHRBANI
GRAZIE
MAAKE
KOMAPSUMNIDA
JUSPAXAR
GOZAIMASHITA
EFCHARISTO
PALDIES
BOLZÏN
MERCI
SPASSIBO
SNACHALHUYA
NUHUN
CHALTU
WABEEJA
MAITEKA
YUSPAGARAYAM
HUI
UNALCHEESH
SPASIBO
DENKAUJA
NENACHALHYA
ATTO
MERSI
SANCO
MERASTAWHY
GAEJTHO
LAH
TAVTAPUCH
MEDAWAGSE
AGUYJE
FAKAAUE
BAINKA
HATUR
GU
EKO-U
SIKOMO
MAKETAI
MINMONCHAR

PCB layout checklist

6 key steps

PCB layout checklist

Step 1: Choose the PCB structure and stackup specification	
1.1	A multi-layer PCB structure is vastly superior to a single- or double-sided PCB to reduce conduction loss, lower thermal impedance, mitigate EMI, and minimize noise and interaction among traces and components
1.2	Understand the stack-up construction vis-à-vis board thickness, copper weight and arrangement of core and prepreg layers
1.3	Using a 4-layer or 6-layer PCB stack-up permits a tightly-coupled, solid GND plane on layer 2
1.4	Improve the coupling to and effectiveness of a GND plane on the bottom side of a 2-layer design by specifying a low height PCB. Otherwise, double-sided designs are essentially relegated to two single-sided assemblies
1.5	Use GND plane(s) to shield sensitive small signal traces from power stage switching noise
1.6	Recognize that best practices for PCB design closely align with high density and small solution size
Step 2: Identify high di/dt current loops and high dv/dt voltage nodes	
2.1	Minimize the area of high current, high di/dt power loops and gate drive loops as these create H-fields that can magnetically couple to nearby low impedance circuits
2.2	Minimize the area of high voltage AC nodes with large dv/dt transitions, for example SW, BOOT, and high-side gate drive, as these represent E-fields that can capacitively couple to nearby high impedance circuits
2.3	Avoid slots, gaps and segments in the GND plane that increase the return current path length, leading to common-mode noise currents and radiated emissions

PCB layout checklist

Step 3: Power stage layout	
3.1	Component selection and floor-planning of the MOSFETs, decoupling capacitors, and shunt resistor should target absolute smallest area and circumference of “hot” loops
3.2	Reduce power loop parasitic inductance, including partial inductances from the MOSFET packages, decoupling capacitor, shunt resistor, and PCB interconnections, as it leads to voltage overshoot, ground bounce, ringing, EMI, and power loss
3.3	With a power loop configured for horizontal current flow, add a GND plane on the layer immediately underneath to act as a shield layer for H-field self-cancellation and reduced parasitic inductance
3.4	Connect multiple decoupling capacitors in parallel to reduce ESR and ESL
3.5	Undesirable SyncFET spurious turn-on is strongly related to high SW node dv/dt as well as gate loop and common-source parasitic inductances. Take steps to mitigate this by decreasing gate pulldown impedance and using tightly-coupled gate and source (return) traces
3.6	Place a resistor in series with the boot capacitor for an asymmetric gate drive design. This attenuates voltage and current slew rates of the turn-on transition without affecting turn-off switching loss
3.7	Locate SW node snubber networks and anti-parallel Schottky diodes for deadtime conduction extremely close to the SyncFET
3.8	For optimal thermal field contours in convective environments, avoid airflow shadowing of low-profile power MOSFET by taller components, such as the filter inductor and electrolytic capacitors
3.9	SW node copper land area is a tradeoff between managing dv/dt-related noise and providing acceptable heatsinking for the low-side MOSFET(s). Large planes with high AC voltage become transmit and receive antenna structures for radiated EMI
3.10	Remove GND plane copper directly underneath the inductor to minimize capacitive coupling to GND, especially if a large number of turns are needed to obtain the inductance
3.11	Separate the inductor terminals’ copper pours to avoid increasing the inductor’s equivalent parallel capacitance (EPC), decreasing its self-resonant frequency (SRF)

PCB layout checklist

Step 4: PWM control IC placement and control section layout	
4.1	Consult device datasheets for specific layout recommendations and layout examples
4.2	Keep the IC close to the MOSFETs for reduced gate drive trace lengths. One option with a two-sided layout is to locate the IC on the opposite side of the PCB relative to the MOSFETs
4.3	Connect the IC's exposed thermal pad to the GND plane(s) underneath using multiple thermal vias for heatsinking
4.4	Locate the VIN, VCC and BOOT capacitors close to the applicable IC pins
4.5	Connect the VCC capacitor's negative terminal to PGND as it behaves as the return for the low-side gate drive
4.6	Keep the FB trace short by locating the feedback resistors adjacent to the IC
4.7	With low-I_Q converters that demand high resistance feedback components, be mindful that the FB node is particularly susceptible to noise pickup
4.8	Use short traces for other critical analog nodes such as error amplifier output (COMP), frequency set (RT), and slope compensation (SLOPE) inputs
4.9	Use a dedicated GND plane moat for small-signal component return currents. Connect this plane to the IC's analog GND pin (AGND)
4.10	Connect PGND and AGND at the IC for single-point grounding

PCB layout checklist

Step 5: Routing of critical traces – gate drive, current sense, voltage sense	
5.1	Make the gate driver trace runs from the controller to the MOSFETs as short and direct as possible to minimize gate loop parasitic inductance
5.2	Reduce common source inductance (the mutual effect between the gate loop and switching loop) by tying the gate drive return directly to the source terminal of the MOSFET
5.3	Route the gate drive traces orthogonal to the power stage to avoid mutual coupling
5.4	Place the gate and source traces parallel to each other on one layer or vertically aligned on adjacent layers to reduce inductance and high dv/dt noise
5.5	Place the low-side gate drive trace close to a PGND plane such that the return current is mutually coupled in a path underneath/above the trace
5.6	For very high duty cycle operation, minimize the parasitic inductance in the boot capacitor refresh current path through the low-side MOSFET
5.7	**Route the current sense traces as a tightly-coupled differential pair, and keep away from the inductor, SW copper and gate drive traces. Locate the RC filter components for the current sense close to the CS and VOUT pins of the IC**
5.8	Use keep-outs to ensure that vias for ground-referenced sense return are isolated from GND planes
5.9	Sense VOUT at the point where accurate regulation is required (usually at the point-of-load). Keep VIN and VOUT sense nets away from high di/dt loops

PCB layout checklist

Step 6: Power and GND plane design	
6.1	Keep the copper planes solid and continuous by minimizing the number of vias used for signal routing
6.2	Use many vias in parallel close to the decoupling capacitors' terminals to connect to power and GND planes. Place positive and negative vias pairs close to each other for flux cancellation
6.3	Fill in both top and bottom layers of the PCB with as much copper at GND potential (ground fill) as possible
6.4	Beware of hidden antenna structures where the conduction path dimension approaches one-quarter wavelength (or a multiple) at the frequency of interest
6.5	Finally, review the PCB layout and flush out any design rule violations

Mitigating EMI at the system level

1. Choose switching frequency to least disturb the system (either free-running or SYNC)
2. Adjust high **dv/dt** nodes to shape spectral content, dissipate resonant energy
   - ✓ Slow switching transitions (e.g. series gate resistance, weaker gate drive)
3. Use **spread spectrum** triangular modulation with 10kHz modulating frequency
   - ✓ Match spectrum analyzer RBW for best peak emission reduction
4. **Careful PCB layout (system board)**
   - ✓ Avoid **coupling mechanisms** (capacitive, inductive, common impedance coupling)
   - ✓ Minimize high **di/dt** loop areas (power & gate drive loops) and parasitic inductance
   - ✓ Watch out for **antenna effect** capable of radiated EMI
5. Spread-spectrum **frequency dithering** (SSFD) for harmonic-peak reduction

PCB layout – brief checklist to mitigate EMI

Power stage layout	
1	Component selection and **floor-planning** of the MOSFETs, decoupling capacitors, and shunt resistor should target absolute **smallest area and circumference of "hot" loops.**
2	**Reduce power loop parasitic inductance**, including partial inductances from the MOSFET packages, decoupling capacitor, low-side shunt resistor and PCB interconnections, as it leads to voltage overshoot, ground bounce, ringing, EMI, and power loss
3	With a power loop configured for horizontal current flow, add a **close (6-mil spacing) GND plane** on the layer immediately underneath to act as a shield layer for H-field self-cancellation and reduced parasitic inductance.
4	Connect **multiple decoupling capacitors** in parallel to reduce ESR & ESL, optimize placement for flux cancelation.
5	SW node copper area is a tradeoff between managing dv/dt-related noise and providing acceptable heatsinking for the low-side MOSFET. Large planes with high AC voltage become transmit and receive antenna structures for radiated EMI. Use shielding techniques around the SW node to minimize electric field coupling and use minimum SW copper area.
6	**Route tightly-coupled MOSFET gate and source (return) traces on inner layers** that are shielded by GND planes above and below; use via stitching for 3-D Faraday shielding effect.
7	**Locate SW node snubber network and/or anti-parallel Schottky diode** for deadtime conduction extremely close to the synchronous FET. Reference the snubber resistor to GND for best thermals.
8	Separate the **inductor terminals' copper pours** to avoid increasing the inductor's equivalent parallel capacitance (EPC), decreasing its self-resonant frequency (SRF). Connect the inductor dotted terminal so that SW is on the inside of the winding, shielded by outer turns connected to VOUT.