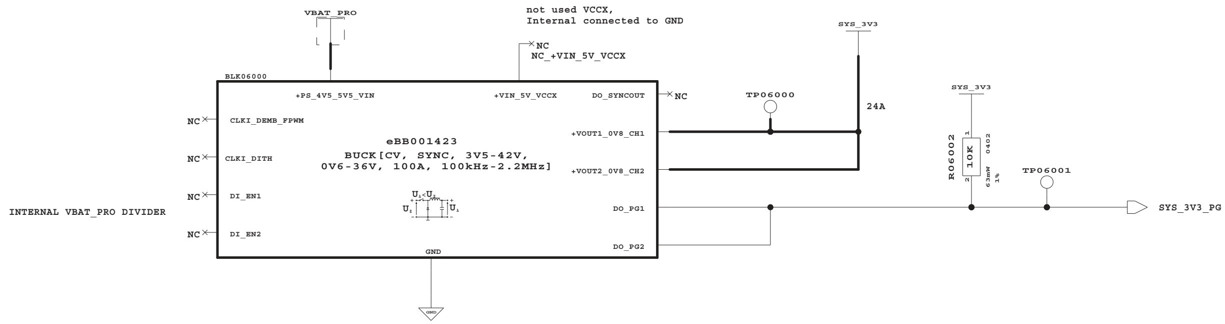
6. PWR-Primary Power Supply 3.3V



Plotted Date : 25/11/11 09:33:28

AUTH.	DATE	DRAWN	REW	MODIFICATIONS	REV
@VL_MO	@VL_MO	@VL_DB	@VL_RE	@VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE	@VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE	@VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE	@VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE	@VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE	@VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE	@VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE	@VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE	@VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE	@VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE	@VL_MO	@VL_RE

Valeo

TITLE: @VL_AS	DRAWN BY: @VL_CR
	DATE: @VL_CR
DRAWING NAME: Definition	CUSTOMER: @VL_CU
PRODUCT: @VL_PR	CONTROLLED BY: @VL_eB
VARIANT: @VL_VA	
BRANCH NO.: @VL_LA — CEE NO.: @VL_LA	APPROVED BY: @VL_eB
@VL_PR — @VL_PR	

DRAWING NUMBER: @VL_PL-ESF020 @VL_DR

SHEET: Page 8 of 98 SIZE: A3

eBB001423

BUCK[CV, SYNC, 3V5-42V, 0V6-36V, 100A, 100kHz-2.2MHz](LM25143)

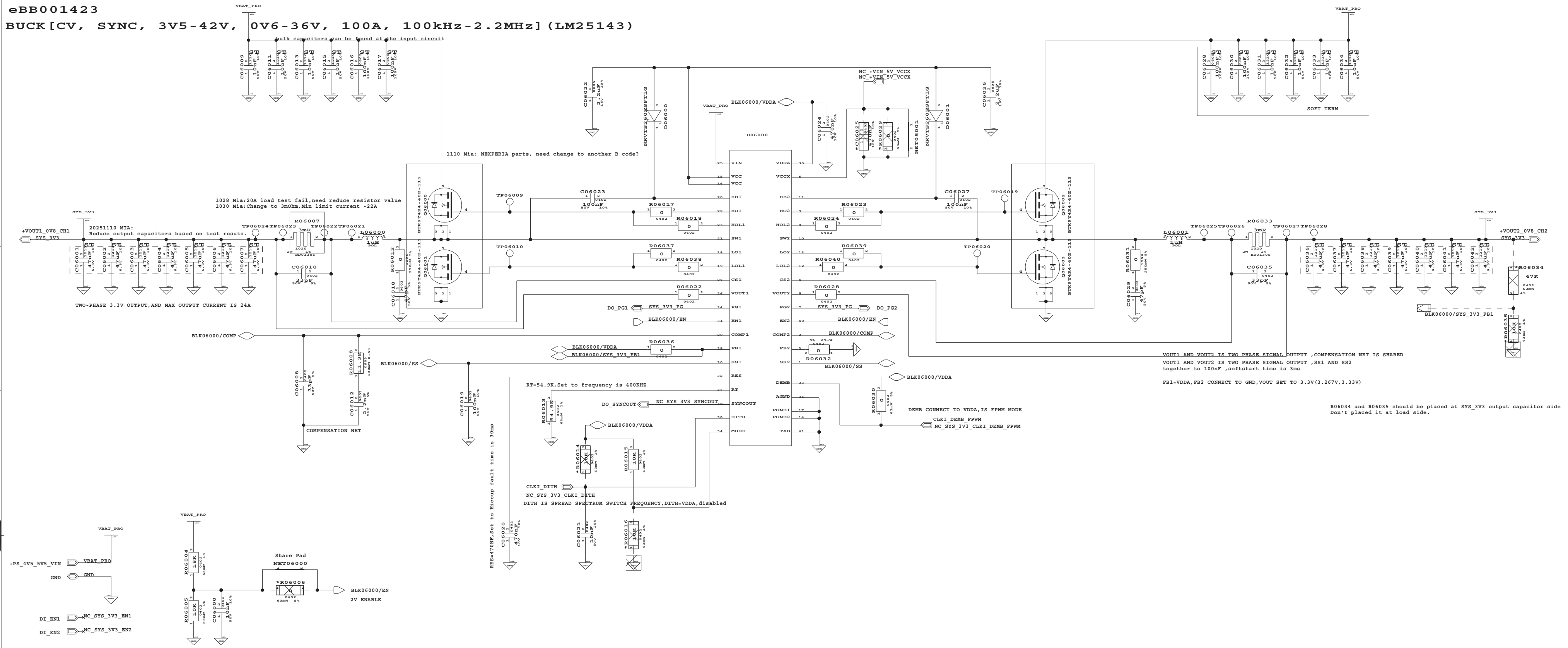


Table 8-2. Single-Output Interleaved Operation

MODE	FB1	FB2	OUTPUT SETPOINT
VDDA	AGND	AGND	5 V
VDDA	VDDA	AGND	3.3 V
VDDA	Rdivider	AGND	0.6 V to 55 V

PIN	DESCIPTION
VCCX	EXTERNAL PS : NEVER CONNECT VCCX TO VOLTAGE GREATER THAN 6.5 V. GND : IF EXTERNAL BIAS VOLTAGE IS NOT USED
VDDA	THERE ARE TWO OPERATING CONDITIONS FOR VDDA BIAS PIN WHERE IT REGULATES AT 0.8 V WHEN VDDA IS 5V. THE FIRST IS IN SKIP CYCLE MODE WHEN VOUT1 IS SET TO 0.8 V AND VOUT2 IS DISABLED. THE SECOND IS IN A COLD-CRANK START-UP WHERE VIN IS 3.8 V AND VOUT1 IS 0.8V
DEMB	AGND : TO ENABLE DIODE EMULATION MODE VDDA : TO ENABLE FPWM OR CCM OPERATION DESIRED THIS PIN 33 ALSO USED AS EXTERNAL CLOCK IN FPWM OPERATION
DITH	CAPACITOR TO AGND : TO ENABLE SPREAD SPECTRUM MODE, VDDA : DISABLES THE DITHER FEATURE. AN EXTERNAL SYNCHRONIZATION CLOCK : DITH IS IGNORED
FB	SINGLE-OUTPUT OUTPUT VOLTAGE SETTING MODE FB1 FB2 OUTPUT VDDA AGND AGND 5 V VDDA VDDA AGND 3.3 V
RT	CONNECT A RESISTOR BETWEEN RT AND AGND TO SET AN OSCILLATOR FREQUENCY. BETWEEN 100 KHZ TO 2.2 MHZ.
CS	IN THIS EBB DCR CURRENT SENSING METHOD IS USED AS PER THE PROJECT REQUIREMENT. FOR OPTIMAL CURRENT SENSE ACCURACY USE SHUNT CURRENT SENSING
COMP	DESIGNED FOR SINGLE OUTPUT OPERATION COMP2(PIN 2) IS CONNECTED TO THE COMP1(PIN 29)
RES	CAPACITOR TO AGND : ENABLE HICCUP MODE PROTECTION FUNCTION VDDA : DISABLE HICCUP FUNCTION CRES (nF) = 17 * tRES(ms) WHERE tRES IS THE SPECIFIED HICCUP DELAY WHEN CRES = 470NF,Set to Hiccup fault time is 28ms

Plotted Date : 25/11/11 09:33:29

AUTH.	DATE	DRAWN	REV	MODIFICATIONS
@VL_MO	@VL_MO	@VL_DB	@VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE @VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE @VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE @VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE @VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE @VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE @VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE @VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE @VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE @VL_MO	@VL_RE
@VL_MO	@VL_MO	@VL_DB	@VL_RE @VL_MO	@VL_RE

Valeo

TITLE: @VL_AS

DRAWING NAME: Definition

PRODUCT: @VL_PR

VARIANT: @VL_VA

BRANCH NO.: @VL_LA

CEE NO.: @VL_LA

@VL_PR

DRAWN BY: @VL_CR

DATE: @VL_CR

CUSTOMER: @VL_CU

CONTROLLED BY:

APPROVED BY:

DRAWING NUMBER: @VL_PL-ESF020 @VL_VA@VL_DR

SHEET: Page 2 of 98

SIZE: A2