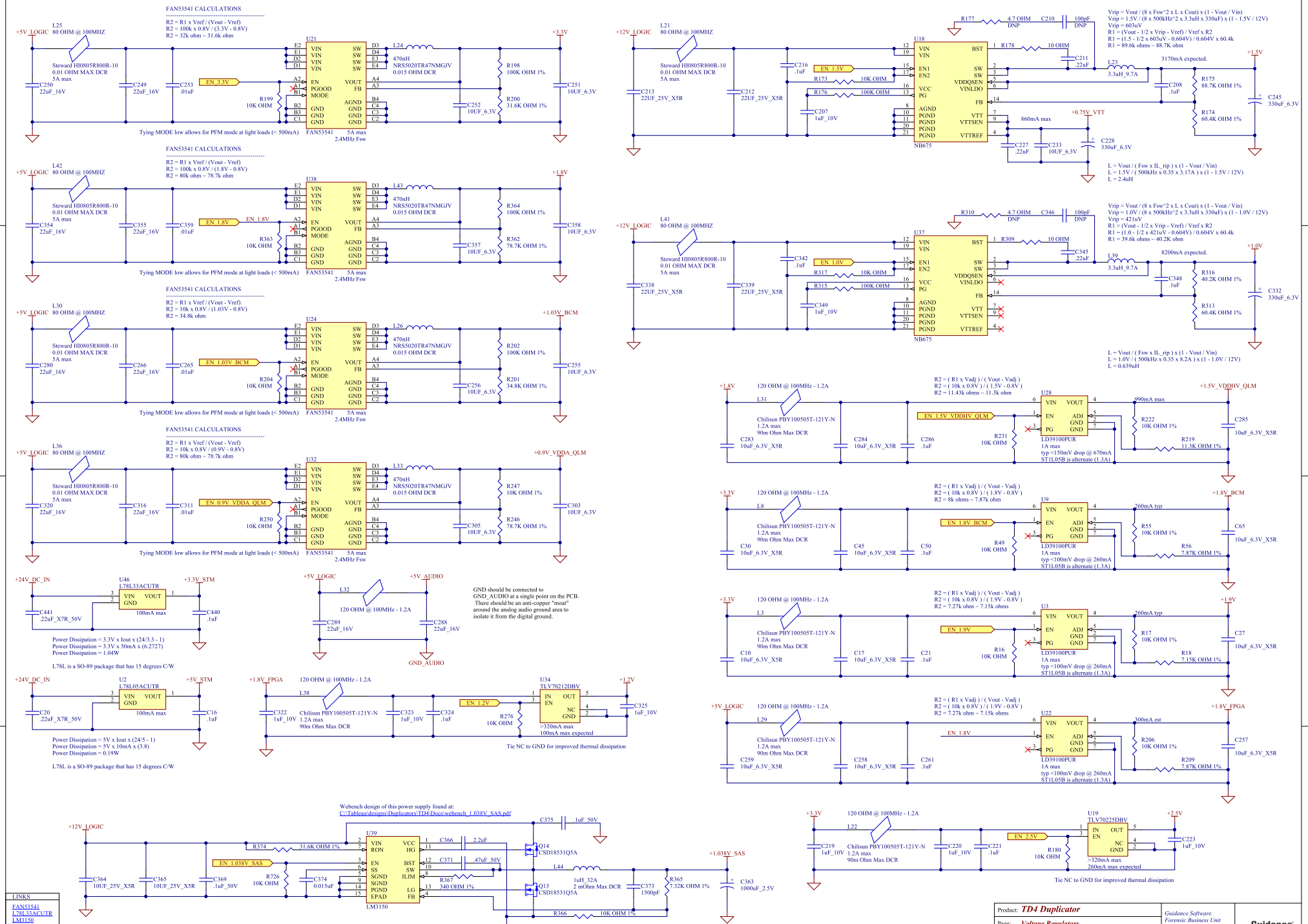
FAN53541 CALCULATIONS
R2 = R1 x Vref / (Vout - Vref)
R2 = 100k x 0.8V / (3.3V - 0.8V)
R2 = 32k ohm ~ 31.6k ohm
+5V_LOGIC
L25
80 OHM @ 100MHZ
Steward HI0805R800R-10
0.01 OHM MAX DCR
5A max
C250
22uF_16V
C249
22uF_16V
C253
.01uF
EN_3.3V
R199
10K OHM
U21
VIN
EN
PGOOD
MODE
GND
SW
VOUT
FB
AGND
FAN53541
5A max
2.4MHz Fsw
L24
470nH
NRS5020T47NMGJV
0.015 OHM DCR
R198
100K OHM 1%
R200
31.6K OHM 1%
C252
10UF_6.3V
C251
10UF_6.3V
+3.3V
Tying MODE low allows for PFM mode at light loads (< 500mA)
FAN53541 CALCULATIONS
R2 = R1 x Vref / (Vout - Vref)
R2 = 100k x 0.8V / (1.8V - 0.8V)
R2 = 80k ohm ~ 78.7k ohm
+5V_LOGIC
L42
80 OHM @ 100MHZ
C354
22uF_16V
C355
22uF_16V
C359
.01uF
EN_1.8V
R363
10K OHM
U38
L43
470nH
NRS5020T47NMGJV
0.015 OHM DCR
R364
100K OHM 1%
R362
78.7K OHM 1%
C357
10UF_6.3V
C358
10UF_6.3V
+1.8V
FAN53541 CALCULATIONS
R2 = R1 x Vref / (Vout - Vref)
R2 = 10k x 0.8V / (1.03V - 0.8V)
R2 = 34.8k ohm
+5V_LOGIC
L30
80 OHM @ 100MHZ
C280
22uF_16V
C266
22uF_16V
C265
.01uF
EN_1.03V_BCM
R204
10K OHM
U24
L26
470nH
NRS5020T47NMGJV
0.015 OHM DCR
R202
100K OHM 1%
R201
34.8K OHM 1%
C256
10UF_6.3V
C255
10UF_6.3V
+1.03V_BCM
FAN53541 CALCULATIONS
R2 = R1 x Vref / (Vout - Vref)
R2 = 10k x 0.8V / (0.9V - 0.8V)
R2 = 80k ohm ~ 78.7k ohm
+5V_LOGIC
L36
80 OHM @ 100MHZ
C320
22uF_16V
C316
22uF_16V
C311
.01uF
EN_0.9V_VDDA_QLM
R250
10K OHM
U32
L33
470nH
NRS5020T47NMGJV
0.015 OHM DCR
R247
10K OHM 1%
R246
78.7K OHM 1%
C305
10UF_6.3V
C303
10UF_6.3V
+0.9V_VDDA_QLM
+24V_DC_IN
U46
L78L33ACUTR
VIN
VOUT
GND
100mA max
C441
.22uF_X7R_50V
C440
.1uF
+3.3V_STM
Power Dissipation = 3.3V x Iout x (24/3.3 - 1)
Power Dissipation = 3.3V x 50mA x (6.2727)
Power Dissipation = 1.04W
L78L is a SO-89 package that has 15 degrees C/W
+5V_LOGIC
L32
120 OHM @ 100MHz - 1.2A
C289
22uF_16V
C288
22uF_16V
+5V_AUDIO
GND_AUDIO
GND should be connected to
GND_AUDIO at a single point on the PCB.
There should be an anti-copper "moat"
around the analog audio ground area to
isolate it from the digital ground.
+24V_DC_IN
U2
L78L05ACUTR
VIN
VOUT
GND
100mA max
C20
.22uF_X7R_50V
C16
.1uF
+5V_STM
Power Dissipation = 5V x Iout x (24/5 - 1)
Power Dissipation = 5V x 10mA x (3.8)
Power Dissipation = 0.19W
L78L is a SO-89 package that has 15 degrees C/W
+1.8V_FPGA
120 OHM @ 100MHz - 1.2A
L38
C322
1uF_10V
Chilisun PBY100505T-121Y-N
1.2A max
90m Ohm Max DCR
C323
1uF_10V
C324
.1uF
EN_1.2V
R276
10K OHM
U34
TLV70212DBV
IN
EN
OUT
NC
GND
>320mA max
100mA max expected
C325
1uF_10V
+1.2V
Tie NC to GND for improved thermal dissipation
Webench design of this power supply found at:
C:\Tableau\designs\Duplicators\TD4\Docs\webench_1.038V_SAS.pdf
+12V_LOGIC
C364
10UF_25V_X5R
C365
10UF_25V_X5R
C369
.1uF_50V
EN_1.038V_SAS
R374
31.6K OHM 1%
R726
10K OHM
C374
0.015uF
U39
VIN
RON
EN
SS
SGND
PGND
EPAD
VCC
HG
BST
SW
ILIM
LG
FB
LM3150
C366
2.2uF
C371
.47uF_50V
R367
340 OHM 1%
C375
.1uF_50V
Q14
CSD18531Q5A
Q13
CSD18531Q5A
L44
1uH_32A
2 mOhm Max DCR
C373
1500pF
R365
7.32K OHM 1%
R366
10K OHM 1%
+1.038V_SAS
C363
1000uF_2.5V
It is important that the sense resistors for the
+1.038V_SAS regulator be located in the ball field of
the LSISAS2308 to ensure minimal voltage drop.
+12V_LOGIC
L21
80 OHM @ 100MHZ
Steward HI0805R800R-10
0.01 OHM MAX DCR
5A max
C213
22UF_25V_X5R
C212
22UF_25V_X5R
C216
.1uF
EN_1.5V
R173
10K OHM
R176
100K OHM
C207
1uF_10V
U18
NB675
BST
SW
VDDQSEN
VINLDO
FB
VTT
VTTSEN
VTTREF
R177
4.7 OHM
DNP
C210
100pF
DNP
R178
10 OHM
C211
.22uF
L23
3.3uH_9.7A
3170mA expected.
+1.5V
C208
.1uF
R175
88.7K OHM 1%
R174
60.4K OHM 1%
C245
330uF_6.3V
860mA max
+0.75V_VTT
C227
.22uF
C233
10UF_6.3V
C228
330uF_6.3V
Vrip = Vout / (8 x Fsw^2 x L x Cout) x (1 - Vout / Vin)
Vrip = 1.5V / (8 x 500kHz^2 x 3.3uH x 330uF) x (1 - 1.5V / 12V)
Vrip = 603uV
R1 = (Vout - 1/2 x Vrip - Vref) / Vref x R2
R1 = (1.5 - 1/2 x 603uV - 0.604V) / 0.604V x 60.4k
R1 = 89.6k ohms ~ 88.7K ohm
L = Vout / (Fsw x IL_rip) x (1 - Vout / Vin)
L = 1.5V / (500kHz x 0.35 x 3.17A) x (1 - 1.5V / 12V)
L = 2.4uH
+12V_LOGIC
L41
80 OHM @ 100MHZ
Steward HI0805R800R-10
0.01 OHM MAX DCR
5A max
C338
22UF_25V_X5R
C339
22UF_25V_X5R
C342
.1uF
EN_1.0V
R317
10K OHM
R315
100K OHM
C349
1uF_10V
U37
NB675
BST
SW
VDDQSEN
VINLDO
FB
VTT
VTTSEN
VTTREF
R310
4.7 OHM
DNP
C346
100pF
DNP
R309
10 OHM
C345
.22uF
L39
3.3uH_9.7A
8200mA expected.
+1.0V
C348
.1uF
R316
40.2K OHM 1%
R313
60.4K OHM 1%
C332
330uF_6.3V
Vrip = Vout / (8 x Fsw^2 x L x Cout) x (1 - Vout / Vin)
Vrip = 1.0V / (8 x 500kHz^2 x 3.3uH x 330uF) x (1 - 1.0V / 12V)
Vrip = 421uV
R1 = (Vout - 1/2 x Vrip - Vref) / Vref x R2
R1 = (1.0 - 1/2 x 421uV - 0.604V) / 0.604V x 60.4k
R1 = 39.6k ohms ~ 40.2K ohm
L = Vout / (Fsw x IL_rip) x (1 - Vout / Vin)
L = 1.0V / (500kHz x 0.35 x 8.2A) x (1 - 1.0V / 12V)
L = 0.639uH
+1.8V
120 OHM @ 100MHz - 1.2A
L31
Chilisun PBY100505T-121Y-N
1.2A max
90m Ohm Max DCR
C283
10uF_6.3V_X5R
C284
10uF_6.3V_X5R
C286
.1uF
EN_1.5V_VDDHV_QLM
R231
10K OHM
U28
LD39100PUR
1A max
typ <150mV drop @ 670mA
ST1L05B is alternate (1.3A)
990mA max
R222
10K OHM 1%
R219
11.3K OHM 1%
C285
10uF_6.3V_X5R
+1.5V_VDDHV_QLM
R2 = (R1 x Vadj) / (Vout - Vadj)
R2 = (10k x 0.8V) / (1.5V - 0.8V)
R2 = 11.43k ohms ~ 11.3k ohm
+3.3V
120 OHM @ 100MHz - 1.2A
L8
Chilisun PBY100505T-121Y-N
1.2A max
90m Ohm Max DCR
C30
10uF_6.3V_X5R
C45
10uF_6.3V_X5R
C50
.1uF
EN_1.8V_BCM
R49
10K OHM
U9
LD39100PUR
1A max
typ <100mV drop @ 260mA
ST1L05B is alternate (1.3A)
260mA typ
R55
10K OHM 1%
R56
7.87K OHM 1%
C65
10uF_6.3V_X5R
+1.8V_BCM
R2 = (R1 x Vadj) / (Vout - Vadj)
R2 = (10k x 0.8V) / (1.8V - 0.8V)
R2 = 8k ohms ~ 7.87k ohm
+3.3V
120 OHM @ 100MHz - 1.2A
L3
Chilisun PBY100505T-121Y-N
1.2A max
90m Ohm Max DCR
C10
10uF_6.3V_X5R
C17
10uF_6.3V_X5R
C21
.1uF
EN_1.9V
R16
10K OHM
U3
LD39100PUR
1A max
typ <100mV drop @ 260mA
ST1L05B is alternate (1.3A)
260mA typ
R17
10K OHM 1%
R18
7.15K OHM 1%
C27
10uF_6.3V_X5R
+1.9V
R2 = (R1 x Vadj) / (Vout - Vadj)
R2 = (10k x 0.8V) / (1.9V - 0.8V)
R2 = 7.27k ohm ~ 7.15k ohms
+5V_LOGIC
120 OHM @ 100MHz - 1.2A
L29
Chilisun PBY100505T-121Y-N
1.2A max
90m Ohm Max DCR
C259
10uF_6.3V_X5R
C258
10uF_6.3V_X5R
C261
.1uF
EN_1.8V
U22
LD39100PUR
1A max
typ <100mV drop @ 260mA
ST1L05B is alternate (1.3A)
300mA est
R206
10K OHM 1%
R209
7.87K OHM 1%
C257
10uF_6.3V_X5R
+1.8V_FPGA
R2 = (R1 x Vadj) / (Vout - Vadj)
R2 = (10k x 0.8V) / (1.9V - 0.8V)
R2 = 7.27k ohm ~ 7.15k ohms
+3.3V
120 OHM @ 100MHz - 1.2A
L22
C219
1uF_10V
Chilisun PBY100505T-121Y-N
1.2A max
90m Ohm Max DCR
C220
1uF_10V
C221
.1uF
EN_2.5V
R180
10K OHM
U19
TLV70225DBV
IN
EN
OUT
NC
GND
>320mA max
260mA max expected
C223
1uF_10V
+2.5V
Tie NC to GND for improved thermal dissipation
LINKS
FAN53541
L78L33ACUTR
LM3150
CSD18531Q5A
TLV70212DBV
LD39100PUR
NB675
Product: TD4 Duplicator
Page: Voltage Regulators
Size: C
Engineer: MB
Revision: 1.0
Date: 1/22/2016
Time: 10:49:55 AM
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File: C:\Tableau\designs\Duplicators\TD4\Design\REV 1.0\Schematic Sheets\[P.34] Voltage Regulators.SchDoc
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