TI Designs

50-W, 92% Efficiency, Compact, Isolated DC-DC Reference Design for 24/36/48-V Battery Systems/UPS

Description

The TIDA-00711 design is a compact, low-cost, high-efficiency, dual output, 50-W, isolated DC-DC converter solution designed for use in uninterruptible power supplies (UPS), energy storage banks, and battery-powered systems that require regulated and isolated power for internal operation.

This reference design is an isolated single-ended primary inductor converter (SEPIC) implemented using the wide-input, current mode controller LM5020. The design is low cost due to a minimal external component count as compared to standard flyback designs realized with 384× series controllers. Additionally, the design operates at a high-switching frequency of 300 kHz, resulting in smaller magnetics and a high-power density solution.

The TIDA-00711 design has built-in protections for output overcurrent and input undervoltage. The hardware has been tested to meet the conducted emission norm EN55011/22 Class A.

Resources

TIDA-00711	Design Folder
LM5020	Product Folder
CSD19534Q	Product Folder

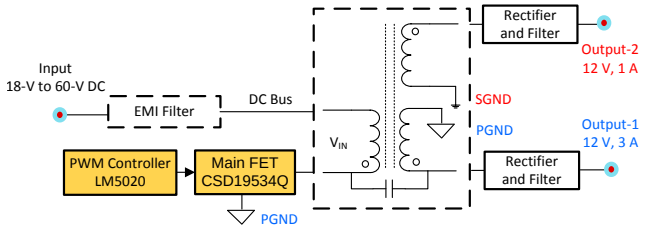
TI E2E™ Community — ASK Our E2E Experts

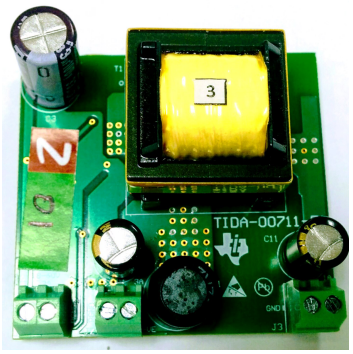
Features

- Designed to Power Wide Range of Applications Using Batteries: Li-Ion, Li-Poly, and Lead-Acid; Voltage Range of 18 V to 60 V
- High Operating Efficiency of 92% at 24-V DC and 90% at 48-V DC
- High Power Density Solution (40 mm × 48 mm × 20 mm) Helps to Optimize Form-Factor of End Equipment Platforms
- Reduced Stress on Switching Components Compared to Standard Flyback Designs Implemented Using 384x Series Devices
- Full Power Delivery Over Entire Input Voltage Range and Wide Temperature Range (up to 55°C) Without Requirement for External Cooling
- Dual Output: 12 V/3 A and 12 V_ISO/1.0 A With Tight Load Regulation of <± 1% and Cross Regulation <± 3%
- Robust Supply Protected for Short Circuit; Overload on Both Isolated Outputs, Non-Isolated outputs, and Input Undervoltage
- Meets Requirements of Conducted Emissions Standard: EN55011/22 Class A

Applications

- Uninterruptible Power Supplies (UPS)
- 24-V/36-V/48-V Battery Powered Systems
- Bidirectional Power Converters
- Energy Storage Banks
- DC Inverters





1 System Overview

1.1 System Description

Uninterruptible power supplies (UPS) and high-power converters used in energy storage banks require auxiliary power supplies to support the housekeeping requirements of the system. An auxiliary power supply is commonly used to power the internal control electronics, switching pulse width modulation (PWM) driver stages and feedback sensing circuits of the system.

Figure 1 shows a typical block diagram of the UPS system which illustrates the use of an auxiliary power converter.

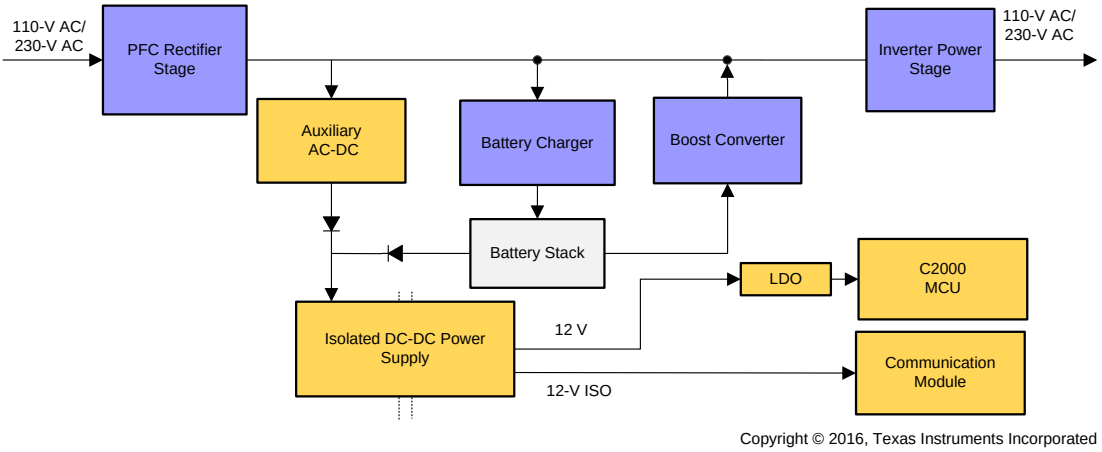


Figure 1. Typical System Block Diagram of UPS

In UPS systems, such as the example shown in Figure 1 and in energy storage banks (powered from mains as well as battery-operated), there are two auxiliary power converters: one operating from AC input/high-voltage DC input and the other operating from battery voltage. Each of these auxiliary power converters is redundant to another and only one is active at a time. The AC-powered auxiliary supply is active during the start-up of the system as well as during the absence of the battery, while the battery-powered, low-voltage, isolated DC-DC converter is active at all times.

The isolated DC-DC converter generates two or multiple outputs to power primary- and secondary-side control electronics. This converter operates from an input voltage range from 10 V to 60 V and addresses the systems with varied batteries such as 12 V, 24 V, 36 V, or 48 V. The power output of this converter ranges from 10 W to 50 W based on the system and application.

This reference design is a 50-W isolated DC-DC converter, which has been specifically designed to accommodate the systems which require two rails: one a regulated rail for primary side (36 W) and the other an isolated rail (12 W) for powering the secondary side of the system. This reference design has a low cost, low component count, isolated single-ended primary-inductance converter (SEPIC), and offers several advantages compared to a standard flyback configuration. Section 2.1 and Section 2.2 explain the advantages in detail. The design operates over a wide input range from 18 V to 60 V and has a high efficiency of 92% for a 24-V input and 90% for a 48-V input.

With an additional input filter, the design meets class A levels of conducted emission norm EN-55011/22. The unit has built-in protection for overcurrent, short circuit, and input undervoltage. The design has been fully tested and validated for various parameters such as regulation, efficiency, electromagnetic interference (EMI) signature, output ripple, start-up, and switching stresses.

Overall, the design meets the key challenges of industrial power supplies to provide safe and reliable power with all protections built-in, while delivering high performance with low power consumption and a low bill-of-material (BOM) cost.

1.2 Key System Specifications

Table 1. Key System Specifications

PARAMETERS	TEST CONDITIONS	MIN	NOM	MAX	UNIT
INPUT CONDITIONS					
Input voltage (V_{IN})	—	18	24	60	V
UVLO	—	16	17	18	V
OUTPUT CONDITIONS					
12-V voltage	Referred to primary	—	12	—	V-DC
12-V current	—	—	—	3	A
12-V line regulation	—	—	—	0.5	%
12-V load regulation	—	—	—	0.5	%
12-V ripple	Peak to peak	—	—	100	mV
12V_Iso rail voltage	Isolated	—	12	—	V-DC
12V_Iso rail current	—	—	—	1	A
12V_Iso rail line regulation	—	—	—	2	%
12V_Iso rail load regulation	—	—	—	2	%
12V_Iso rail cross regulation	When load on Output-1 is 10% and 12V_Iso is varied from 10% to 100% load	—	—	3	%
12V_Iso ripple	Peak to peak	—	—	100	mV
Output power	Indoor and outdoor	—	48	—	W
SYSTEM CHARACTERISTICS					
Efficiency (η)	V_{IN} = V_{NOM} and full load	90	—	—	%
Operating ambient	—	–10	25	55	°C
Board size	Length × width × height	40 × 48 × 20			mm

1.3 Block Diagram

Figure 2 shows the high-level block diagram of TIDA-00711. The main parts of this design are the wide V_{IN} current mode PWM controller LM5020 and 100-V switching MOSFET CSD19534Q.

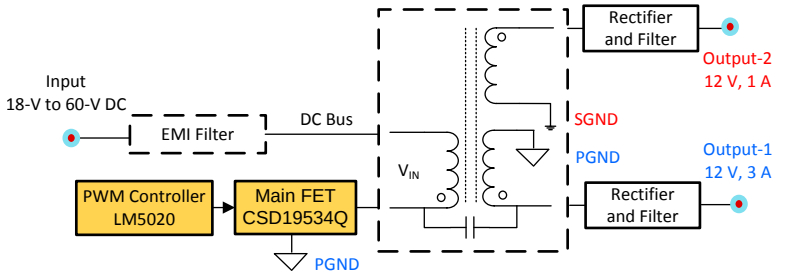


Figure 2. TIDA-00711 Block Diagram

1.4 Highlighted Products

This TIDA-00711 reference design features the following devices that were selected based on their specifications and appropriateness for this design. The key features of the highlighted products are mentioned as follows. For more information on each of these devices, see their respective product folders at http://www.ti.com or click on the links for the product folders on the first page of this reference design.

1.4.1 LM5020—100-V Current-Mode PWM Controller

The LM5020 high-voltage PWM controller contains all of the features required to implement single-ended, primary-power converter topologies. Output voltage regulation is based on current-mode control, which eases the design of loop compensation while providing inherent line feedforward. The LM5020 includes a high-voltage start-up regulator that operates over a wide input range up to 100 V. The PWM controller is designed for high-speed capability including an oscillator frequency range to 1 MHz and total propagation delays less than 100 ns.

Additional features include an error amplifier, precision reference, line undervoltage lockout (UVLO), cycle-by-cycle current limit, built-in slope compensation, soft start, oscillator synchronization capability, and thermal. The controller is available in both VSSOP-10 and WSON-10 packages. For more details on this PWM controller, refer to the datasheet [1].

1.4.2 CSD19534Q

For effective thermal management in small form-factor, high-power density designs, having high-efficient devices and the capability to extract heat effectively is vital.

CSD19534 is a cost-optimized, 100-V, 12.6-mΩ, SON 5×6-mm NexFET™ power MOSFET which is designed to minimize losses in DC-DC power conversion applications.

The lower Qg and Qgd parameters make this MOSFET an ideal choice to reduce switching loss for this high-frequency application switching at 300 kHz. Additionally, the field-effect transistor (FET) is optimized for effective cooling with low thermal resistance from junction to case.

For more details on this FET, refer to the datasheet [2].

2 System Design Theory

This reference design provides 50 W of continuous power over a wide DC input range from 18- to 60-V DC. The design has an isolated SEPIC power stage implemented using an LM5020 current-mode PWM controller to deliver two regulated power rails 12 V/3 A and 12V-ISO/1A.

2.1 SEPIC Versus Flyback Converter

For most of the low-to-mid voltage (6- to 100-V DC input) and high-wattage (10 W to 50 W) converters, designers face a challenge to decide between a flyback or SEPIC topology. The popular choice is typically the flyback mostly because of a lack of familiarity with SEPIC; however, this choice may not be the best decision. This section highlights the trade-offs between the two topologies based on analytic comparisons and demonstrates that the SEPIC is often the best choice

Figure 3 shows a simplified power-stage schematic for both topologies.

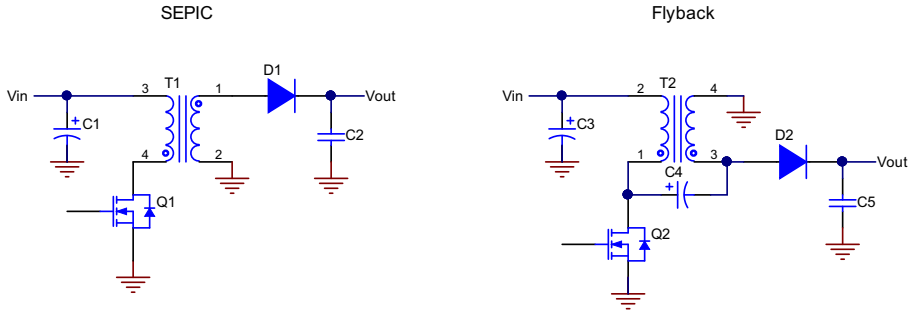


Figure 3. Simplified Power-Stage Schematic for SEPIC and Flyback Topologies

Table 2 shows the comparison of critical component parameters for each of the topologies. In the comparison, the converters are considered to be operating in continuous-conduction mode (CCM) because of a lower input voltage range and higher wattage.

Table 2. Comparison Table—Flyback and SEPIC Converter Parameters

PARAMETERS OR COMPONENTS	KEY DIFFERENCES BETWEEN FLYBACK AND SEPIC CONFIGURATION
MOSFET voltage rating and associated losses	The flyback must switch an unclamped inductance and has a significantly higher FET voltage stress and diode peak inverse voltage (PIV) than the SEPIC. Because the flyback requires a higher voltage-rated FET, the conduction losses increase by approximately 50% due to the higher Rds(on) of the FET. The large voltage spike also increases the switching turn OFF losses relative to that of the SEPIC. Voltage spikes on the power switch and output diode caused by the flyback transformer leakage inductance usually require a voltage clamp, and/or snubber circuit to limit the peak voltage, further reducing efficiency. In SEPIC, the advantage is that the voltage across the FET is well-clamped by the AC-coupling capacitor, hence the main switching FET experiences lower voltage stress and has lower switching losses.
Diode PIV rating and associated losses	The negative voltage spike on the flyback transformers secondary makes a Schottky diode unacceptable and forces the use of an ultra-fast diode, with its higher conduction losses and correspondingly lower efficiencies. In SEPIC, the output diode voltage is clamped by an AC-coupling capacitor, resulting in less circuit ringing and lower stress on the component.
Isolation transformer	The only significant component advantage of a flyback is a smaller inductance requirement. The volume of an inductor is generally related to the energy storage requirement of L multiplied by I, with the flyback requiring about 60% to 70% of the SEPICs energy storage. This lower-energy storage requirement typically allows the flybacks inductor to be smaller than the SEPICs inductor.

Table 2. Comparison Table—Flyback and SEPIC Converter Parameters (continued)

PARAMETERS OR COMPONENTS	KEY DIFFERENCES BETWEEN FLYBACK AND SEPIC CONFIGURATION
Input and coupling capacitors	The flyback uses two or more input capacitors rated to handle the large AC_{RMS} requirement of the pulsating current generated by the FET switch. The significantly-lower RMS input ripple current of the SEPIC "relaxes" the input-capacitance requirement. With the SEPIC, only a single input capacitor is required to handle the rather low AC_{RMS} rating of the triangular inductor current. However, another AC-coupling capacitor is required on the SEPIC. Capacitor ripple currents are identical for both topologies, when the input capacitor of the flyback is compared to the coupling capacitor of the SEPIC. These components have the same voltage stress and have similar voltage ratings because they are each charged to the input voltage.
Output capacitors	Both converters have the same output capacitance requirement because each must fully support the output load current during the OFF time of the diode. Both topologies have large AC-ripple currents and must use low equivalent series resistance (ESR) capacitors.

While the relative simplicity and familiarity of the flyback converter has its advantages, the SEPIC converter can provide higher efficiency and lower component stress. The SEPIC is more efficient because semiconductors with lower voltage ratings can be used due to lower circuit-voltage stresses. Continuous input current not only reduces the input-capacitor ripple-current rating of the SEPIC, but it also improves a system's electromagnetic emissions. If there are other loads on the input, the flyback's discontinuous input current is more likely to generate an unacceptable ripple on the input, which may require additional filtering. One downside of the SEPIC is that it has an additional passive component, an AC-coupling capacitor, which complicates the control characteristics. However, when implemented correctly, the SEPIC converter provides an excellent, highly-efficient solution.

2.2 Advantages of LM5020 Solution Over Conventional 384x Solution

Figure 4 and Figure 5 show the actual schematics of the solutions for a 50-W isolated DC-DC converter designed with a wide-input, current-mode PWM controller LM5020 and traditional PWM controller UC3842. The differences in the schematics and additional components required for each of the circuit implementations are highlighted in red color for ease of differentiation.

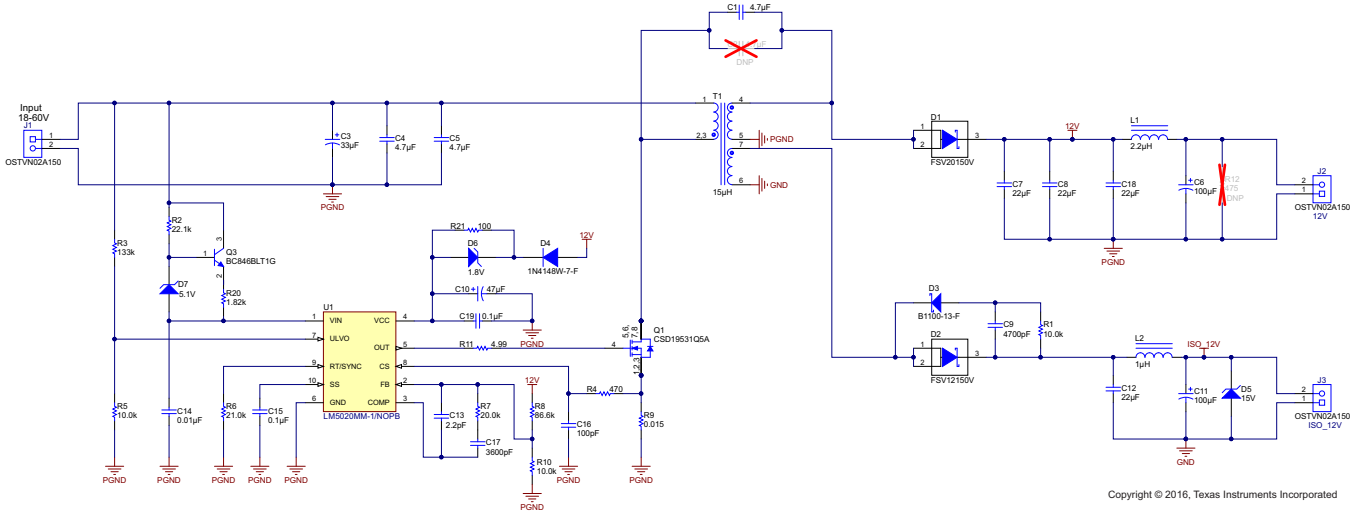


Figure 4. LM5020 Solution

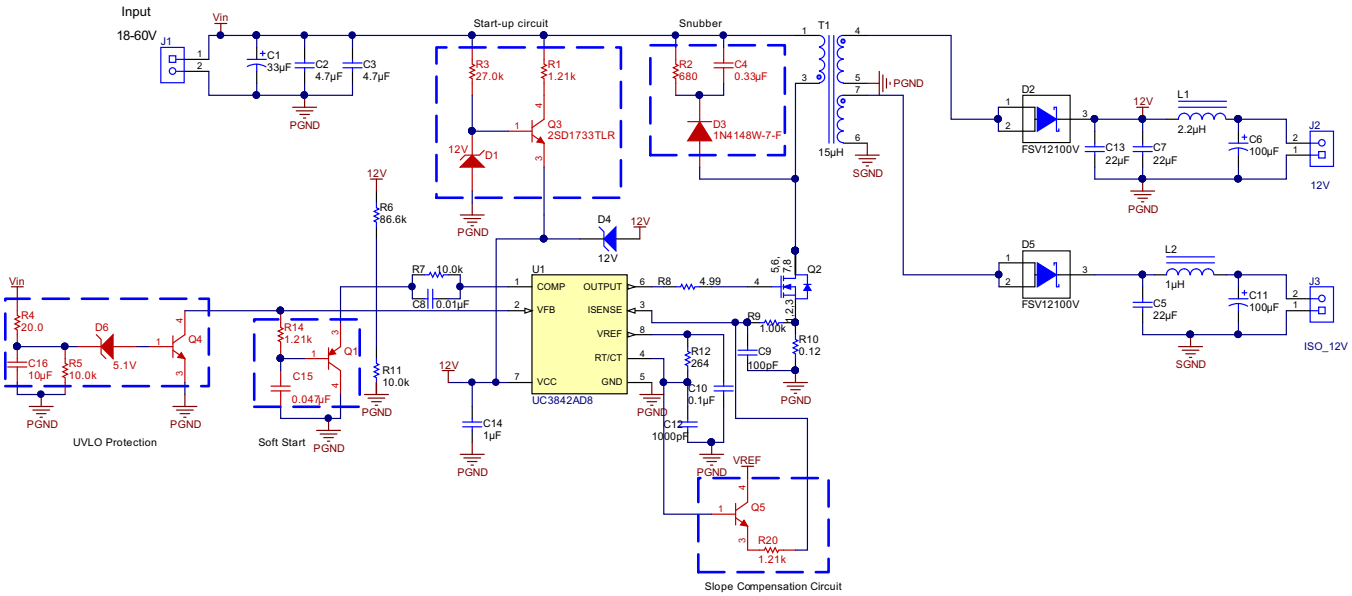


Figure 5. 384x Solution

The traditional solution requires additional circuit components to incorporate the following feature set:

- External start-up circuit for input voltages > 30-V DC
- Undervoltage lockout (UVLO) circuit for cutoff during low battery conditions
- Slope compensation circuit for operation over a 50% duty cycle and in continuous-conduction mode (CCM)
- Soft-start circuit to ensure a smooth startup for all load conditions

Each of the preceding circuits is built-in to an LM5020 controller, which reduces the associated component count and cost significantly.

Secondly, the LM5020 offers the following advantages:

- Lower current sense threshold (0.5 V in LM5020 versus 1.0 V in UC3842), which reduces power loss and results in high efficiency
- Lower device power consumption I_{VCC_MAX}: 3 mA for LM5020 versus 17 mA in UC3842, which implies a higher power consumption; for example, at a 15-V input, the LM5020 consumes 45 mW of power compared to 260 mW of power from the UC3842.

2.3 SEPIC Circuit Component Design

2.3.1 Design Goal Parameters

Table 3 shows the design goal parameters for this design. These parameters are used in further calculations to select components.

Table 3. Reference Design Performance Specifications

PARAMETERS	MIN	TYP	MAX	UNIT
INPUT CHARACTERISTIC				
Input voltage range, V_{IN}	18	24	60	V
Switching frequency, f_{SW}	—	300	—	kHz
OUTPUT CHARACTERISTIC				
Output voltage (main)	—	12	—	V
Output current (main)	—	3	—	A
Output voltage (ISO)	—	12	—	V
Output current (ISO)	—	1	—	A
Output voltage ripple	—	100	—	mVpp

Refer to the schematic in the preceding Figure 4 for all the component nomenclature used in the equations.

2.3.2 Switching Frequency (R6)

Choosing the switching frequency is one of the main tradeoffs to consider when creating a design. Lower switching frequencies are generally used for higher efficiency with relatively larger external component size. Alternatively, a higher switching frequency results in a smaller component size with relatively lower efficiency. This design uses 300 kHz to optimize the size of the board as well as to achieve high efficiency.

A single external resistor connected between the RT and GND pins sets the LM5020 oscillator frequency. The resistance to set this frequency is calculated with Equation 1 from the product datasheet and the nearest standard value is used. For a 300-kHz switching frequency, the calculated resistance is 21.09 kΩ. The nearest standard value used is 21.0 kΩ.

$$RT = \frac{1}{F \times 158 \times 10^{-12}} \tag{1}$$

2.3.3 Duty Cycle Calculations

For further calculations, the minimum and maximum duty cycles are first estimated in CCM, which is performed using Equation 2. Limitations are placed on the duty cycle based on the maximum duty cycle of the LM5020 controller to 85%.

$$D = \frac{V_{OUT} + V_D}{V_{OUT} + V_D + V_{IN}} \tag{2}$$

V_D is the forward voltage drop of the rectifying diode, estimated at 0.5 V. With the minimum input voltage V_{IN_MIN} = 18 V, the maximum duty cycle is, D_{max} = 0.409. Similarly, with the maximum input voltage V_{IN_MAX}max = 60 V, the minimum duty cycle is D_{min} = 0.182.

The regulator enters discontinuous conduction mode (DCM) when the sum of the currents in the two inductors ramp to zero at the end of each switching cycle. The critical current when the device operates in DCM can be calculated with Equation 3. While operating in this mode, in addition to the input and output voltage, the duty cycle is a function of the load current, inductance, and switching frequency. The duty cycle can be estimated using Equation 4.

$$I_{OUT\_CRIT} = \frac{V_{IN}^2 \times (V_{OUT} + V_D)}{2 \times f_{SW} \times L \times (V_{OUT} + V_D + V_{IN})^2} \tag{3}$$

$$D_{DCM} = \frac{\sqrt{2 \times L \times (V_{OUT} + V_D) \times I_{OUT} f_{SW}}}{V_{IN}} \quad (4)$$

2.3.4 Maximum Output Current

A few design parameters must first be considered before determining the maximum output current. For stable power supply operation and to minimize EMI, the inductor is selected as such to keep the inductor ripple current (ΔI_L) a fraction of the DC current in La. The DC current in La is equal to the maximum DC input current (I_{IN_DC}). The fraction is represented by the coefficient K_{IND} and is typically 0.2 to 0.4. Similar to other switching regulators, by choosing a higher K_{IND}, the recommended inductance is lower. This lower inductance increases the current ripple and a smaller inductor package is possible for a given saturation current. The higher current ripple typically leads to higher EMI, a lower maximum output current, larger output capacitance for a desired output ripple, and a faster transient performance; the opposite is true for a lower K_{IND}. The recommended inductance is higher, decreasing the current ripple and increasing the inductor package size. The lower current ripple typically reduces EMI, increases the maximum output current, reduces the required output capacitance, and slows the transient response. The tradeoffs must be made based on the system level goals of the design.

The maximum input current is first calculated with Equation 5 using a conservative, estimated full-load efficiency, η_{EST} = 85% and V_{IN_MIN} = 18 V. Equation 6 then calculates the desired peak-to-peak current ripple.

$$I_{IN\_DC} = \frac{V_{OUT} \times I_{OUT}}{\eta_{EST} \times V_{IN\_MIN}} \quad (5)$$

$$\Delta I_L = I_{IN\_DC} \times K_{IND} \quad (6)$$

I_{IN_DC} is estimated at 3.13 A and with K_{IND} = 0.4, the desired ripple current is 1.255 A.

2.3.5 Inductor (L)

Based on the targeted ΔI_L, the minimum inductance (L) is calculated with Equation 7. The maximum input voltage and its corresponding duty cycle are used because this is when the current ripple in a SEPIC is at the maximum. Again, the equation assumes that a coupled inductor is being used to reduce the required inductance by half.

$$L \geq \frac{V_{IN} \times D}{2 \times f_{SW} \times \Delta I_L} \quad (7)$$

For this design, a recommended minimum L of 14.5 µH is calculated and the nearest standard value of 15 µH is chosen. With a 15-µH inductor, by rearranging Equation 7, ΔI_L is calculated to 1.2133 A at V_{IN_MAX} and 818 mA at V_{IN_MIN}. At this point, the designer can choose to reevaluate the maximum output current with the chosen inductance. The peak current and RMS current must then be calculated to ensure the inductor is properly rated. In a coupled inductor, the total peak current is the sum of the peak current in each winding.Equation 8 calculates the peak current (La is the primary-side inductance and Lb is the output-side inductance referred to primary).

$$I_{L\_peak} = I_{La\_peak} = \left(I_{IN\_MAX} + \frac{\Delta I_L}{2}\right) + \left(I_{OUT} + \frac{\Delta I_L}{2}\right) \quad (8)$$

For this design, the peak current is estimated to be 8.343 A. TI recommends that the saturation current of the inductor be 20% higher than the peak current, which leaves a margin for transient conditions when the peak inductor current potentially increases above the steady state value.

Equation 9 and Equation 10 calculate the RMS current in each winding. Equation 11 and Equation 12 takes these current values and converts them to the ratings (I_{RMS_one} and I_{RMS_both}) that the datasheets typically show for coupled inductors. I_{RMS_one} represents only one winding conducting and I_{RMS_both} represents both windings conducting equally. The ratings are typically given for a 40°C temperature rise.

$$I_{La\_RMS} \approx I_{IN\_DC} \quad (9)$$

$$I_{Lb\_RMS} \approx I_{OUT} \quad (10)$$

$$I_{RMS\_one} = \sqrt{\left(I_{La\_RMS}\right)^2 + \left(I_{Lb\_RMS}\right)^2} \quad (11)$$

$$I_{RMS\_both} = \sqrt{\frac{\left(I_{RMS\_one}\right)^2}{2}} \quad (12)$$

The equivalent RMS values calculated for the inductor are I_{RMS_one} = 5.08 A and I_{RMS_both} = 3.59 A.

2.3.6 Output Capacitor (C7-C8)

The output capacitor is chosen based on the maximum output voltage ripple and minimum output voltage variation from load transients. A typical, output-voltage ripple (V_{RIPPLE}) specification is 0.5% of the nominal output voltage; however, this value is typically selected at a system level. Based on the specification of 100-mVpp output ripple, Equation 13 is used to calculate the minimum output capacitance.

$$C_{OUT} \geq \frac{D_{max} \times I_{OUT}}{f_{SW} \times V_{RIPPLE}} \quad (13)$$

The minimum output capacitance to meet this specification is 40.9 µF. This specification assumes that a ceramic output capacitor is being used with negligible equivalent series resistance (ESR). The use of non-ceramic capacitors contributes to additional voltage ripple. Equation 14 calculates the total ripple and Equation 15 calculates the maximum ESR to meet the voltage ripple specification. One important fact to note is that the ripple in the ESR is not in phase with the ripple from the output capacitance and Equation 15 underestimates the maximum ESR. A higher ESR may be possible with testing or simulation of the circuit under real test conditions.

$$V_{RIPPLE} = \frac{D_{max} \times I_{OUT}}{f_{SW} \times C_{OUT}} + ESR_{COUT} \times \left(I_{La\_peak} + I_{Lb\_peak}\right) \quad (14)$$

$$ESR_{COUT} \leq \frac{V_{RIPPLE} - \frac{D_{max} \times I_{OUT}}{f_{SW} \times C_{OUT}}}{\left(I_{La\_peak} + I_{Lb\_peak}\right)} \quad (15)$$

If non-ceramics are used or the output capacitors are specified at an RMS current rating, use Equation 16 to calculate the RMS current. The RMS current has been calculated at 2.499 A for this design.

$$I_{COUT\_RMS} = I_{OUT} \sqrt{\frac{D_{max}}{\left(1 - D_{max}\right)}} \quad (16)$$

The selected output capacitors are 3×22-µF, 25-V X7R 1210 ceramic capacitors. When using ceramic capacitors, accounting for derating due to DC bias is important. With a 12-V output voltage, the estimated capacitance is 46% of the nominal value with a given derated capacitance of 30.4 µF.

2.3.7 AC Capacitor (C1-C2)

TI recommends to choose the AC capacitor (C_P) so that the ripple voltage ΔV_{CP} is no more than 5% of the maximum V_{CP_DC} equal to V_{IN_MAX}. Equation 17 calculates the minimum capacitance.

$$C_P \geq \frac{I_{OUT} \times D_{max}}{0.05 \times V_{IN\_max} \times f_{SW}} \quad (17)$$

The minimum capacitance is calculated to be 1.8 µF; due to derating, and to account for the current through the capacitor, a higher standard value of 4.7 µF is used. This capacitor must be rated for the maximum input voltage and the capacitance derating due to DC bias must be taken into consideration. The capacitor must also be rated for the RMS current (I_{CP_RMS}), which is calculated as 3.75 A using Equation 18. The capacitor selected is a 4.7-µF, 80-V X7R 1210 ceramic capacitor.

$$I_{CP\_RMS} = I_{IN\_DC} \times \sqrt{\frac{\left(1 - D_{max}\right)}{D_{max}}} \quad (18)$$

2.3.8 Rectifying Diode (D1)

Similar to a boost converter, the average current through the diode is equal to the output current. The rectifying diode must be chosen to handle the output current and voltage at the switching node. A margin of at least 20% is recommended for the average current rating of the diode. A conservative design uses the maximum output current with V_{IN_MAX} with the typical current limit to choose the current rating.

Equation 19 calculates the minimum breakdown voltage (V_{BR}) of the diode to be 30.5 V, assuming V_D is 0.5 V.

$$V_{BR} = V_{OUT} + V_{IN\_MAX} + V_D \tag{19}$$

The diode package must be rated for the power dissipation. The power is calculated using Equation 20 to be 1.5 W with a 3-A output.

$$P_D = I_{OUT} \times V_D \tag{20}$$

Based on these criteria, the FSV12100V diode is chosen, which is a 100-V, 12-A diode.

2.3.9 MOSFET Ratings

The voltage at the switching node is the sum of V_{OUT} and V_{IN}. Similarly, the peak current is equal to the sum of the input current, output current, and peak-to-peak ripple current. Equation 21 calculates the voltage, Equation 22 calculates the current, and Equation 23 calculates the RMS current.

$$V_Q = V_{OUT} + V_{IN\_MAX} \tag{21}$$

$$I_{Q\_peak} = I_{OUT} + I_{IN\_DC} + \Delta I_L \tag{22}$$

$$I_{Q\_RMS} = \frac{I_{IN\_DC}}{\sqrt{D_{max}}} \tag{23}$$

In this design, the voltage stress of the MOSFET is 100 V and the peak current is 8.343 A. Based on these criteria, the CSD19534Q MOSFET is chosen. Also, for smaller form factor requirements, consider using the CSD19537Q.

2.3.10 Feedback Resistors (R8, R10)

The feedback resistors are chosen as per the internal reference of the LM5020. The bottom resistor (R10) is fixed at the recommended 10 kΩ to minimize noise and current through the feedback divider. The top resistor (R1) is then calculated with Equation 24 using the LM5020 voltage reference (V_{REF}) of 1.229 V. R1 is calculated at 87.6 kΩ and the nearest standard value of 86.6 kΩ is chosen.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{24}$$

2.3.11 Soft-Start Capacitor (C3)

To have soft start with a full load, a 0.047-µF soft-start capacitor has been used for this design.

2.3.12 Compensating Control Loop (R7, C13, C17)

Deriving a mathematical model of the SEPIC converter is extremely complicated. The easiest and fastest method to design the compensation is to use a SPICE model or measured data. For this design, load transient waveforms for step change in load conditions (10% to 90%) are used to choose and optimize the compensation components.

3 Getting Started Hardware

3.1 Required Test Equipment for Board Validation

- Isolated DC source
- Digital oscilloscope
- Multimeters
- Electronic or resistive load

3.2 Test Conditions

Input voltage range

The DC source must be capable of varying between V_{IN}DC: 10-V and 60-V DC. Set the input current limit to 4 A.

Output

Connect an electronic load capable of 20 V and a load variable in the range of 0 A to 3 A for each of the outputs. A rheostat or resistive decade box can be used in place of an electronic load.

3.3 Test Procedure

1. Connect the DC source at the input terminals (pin 1 and pin 2 of connector J1) of the reference board.
2. Connect the output terminals (pin 1 and pin 2 of connector J2 and pin 1 and pin 2 of connector J3) to the electronic load or rheostat while maintaining the correct polarity. Pin 1 is the VOUT output terminal pin and pin 2 is the GND terminal pin
3. Set and maintain a minimum load of about 10 mA.
4. Gradually Increase the input voltage from 0 V to turn on 18-V DC.
5. Turn on the load to draw current from the output terminals of the converter.
6. Observe the start-up conditions for smooth switching waveforms.

4 Testing and Results

The test results are divided into multiple sections that cover the steady-state performance measurements, functional performance waveforms and test data, transient performance waveforms, thermal measurements, and conducted emission (CE) measurements.

4.1 Performance Data

4.1.1 Efficiency and Regulation With Load Variation

Table 4 shows the efficiency and regulation performance data at 24 V.

Table 4. Efficiency and Regulation at 24 V

LOAD %	V_{IN}	I_{IN}(A)	P_{INDC}(W)	V_{OUT1}(V)	I_{OUT1}(mA)	V_{OUT2}(V)	I_{OUT2}(mA)	P_{OUT}(W)	EFF (%)	%REG VOUT1	%REG VOUT2	POWER LOSS (W)
10	23.85	0.247	5.89	12.155	0.302	12.233	0.105	4.96	84.12	0.02	0.65	0.94
25	23.60	0.588	13.88	12.157	0.753	12.252	0.252	12.24	88.22	0.04	0.81	1.64
50	23.21	1.167	27.09	12.153	1.502	12.175	0.535	24.77	91.44	0.00	0.18	2.32
75	22.80	1.746	39.81	12.150	2.251	12.102	0.761	36.56	91.84	-0.02	-0.42	3.25
100	22.35	2.387	53.35	12.147	3.007	12.005	1.020	48.77	91.42	-0.04	-1.22	4.58

Table 5 shows the efficiency and regulation performance data at 36 V.

Table 5. Efficiency and Regulation at 36 V

LOAD %	V_{IN}	I_{IN}(A)	P_{INDC}(W)	V_{OUT1}(V)	I_{OUT1}(mA)	V_{OUT2}(V)	I_{OUT2}(mA)	P_{OUT}(W)	EFF (%)	%REG VOUT1	%REG VOUT2	POWER LOSS (W)
10	35.90	0.183	6.57	12.131	0.305	12.225	0.103	4.96	75.48	0.12	0.26	1.61
25	35.74	0.405	14.47	12.128	0.752	12.248	0.251	12.19	84.25	0.09	0.44	2.28
50	35.50	0.766	27.19	12.117	1.502	12.223	0.501	24.32	89.45	0.00	0.24	2.87
75	35.32	1.130	39.91	12.108	2.250	12.169	0.752	36.39	91.19	-0.07	-0.20	3.52
100	35.07	1.521	53.35	12.099	3.011	12.104	1.002	48.55	91.01	-0.15	-0.74	4.79

Table 6 shows the efficiency and regulation performance data at 48 V.

Table 6. Efficiency and Regulation at 48 V

LOAD %	V_{IN}	I_{IN}(A)	P_{INDC}(W)	V_{OUT1}(V)	I_{OUT1}(mA)	V_{OUT2}(V)	I_{OUT2}(mA)	P_{OUT}(W)	EFF (%)	%REG VOUT1	%REG VOUT2	POWER LOSS (W)
10	47.90	0.152	7.281	12.154	0.303	12.263	0.104	4.96	68.10	0.11	0.28	2.32
25	47.79	0.320	15.293	12.150	0.757	12.263	0.252	12.29	80.35	0.07	0.28	3.00
50	47.59	0.583	27.745	12.142	1.490	12.256	0.490	24.10	86.85	0.01	0.22	3.65
75	47.54	0.869	41.312	12.134	2.260	12.209	0.768	36.80	89.08	-0.06	-0.16	4.51
100	47.17	1.153	54.387	12.125	3.006	12.153	1.034	49.01	90.12	-0.13	-0.62	5.37

Table 7 and Table 8 show the cross-reference data for the 12-V_ISO/1A rail. The cross-reference data for the rail was noted while the other output was at 10% load and full load, respectively, with a 48-V input voltage.

Table 7. Cross Regulation for V_{OUT2} (12 V_ISO/1 A) With 10% Load on V_{OUT1}

LOAD ON 12V_ISO	VOUT2(V)	%REG
10	12.246	2.10
25	12.137	1.19
50	11.980	-0.12
75	11.880	-0.96
100	11.730	-2.21

Table 8. Cross Regulation for V_{OUT2} (12 V_ISO/1 A) With 100% Load on V_{OUT1}

LOAD ON 12V_ISO	VOUT2(V)	%REG
10	12.717	2.61
25	12.470	0.61
50	12.363	-0.25
75	12.258	-0.96
100	12.161	-2.21

4.2 Performance Curves

4.2.1 Efficiency With Load Variation

Figure 6 shows the measured efficiency of the system with DC input voltage variation.

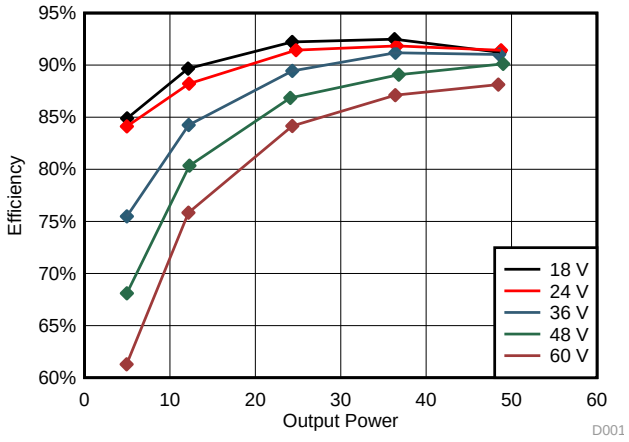


Figure 6. Efficiency versus Output Power

4.2.2 Load and Line Regulation

Figure 7 shows the measured load regulation of the 12V_Main/3A output. Figure 8 shows the measured load regulation of the 12V_ISO/1A output.

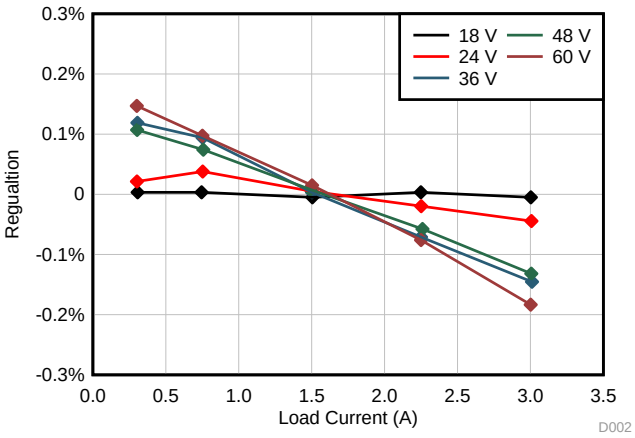


Figure 7. 12-V_Main Output Voltage Regulation With Load Current

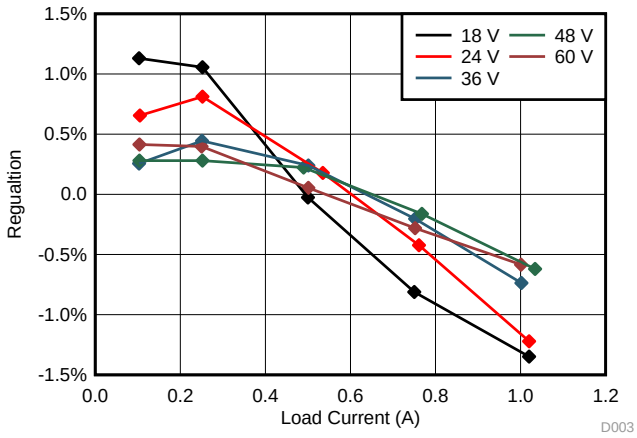


Figure 8. 12-V_ISO Output Voltage Regulation With Load Current

Figure 9 shows the measured cross regulation of 12V_ISO when 12V_Main is at 10% load and at full load. Figure 10 shows the measured line regulation of both the outputs at full load.

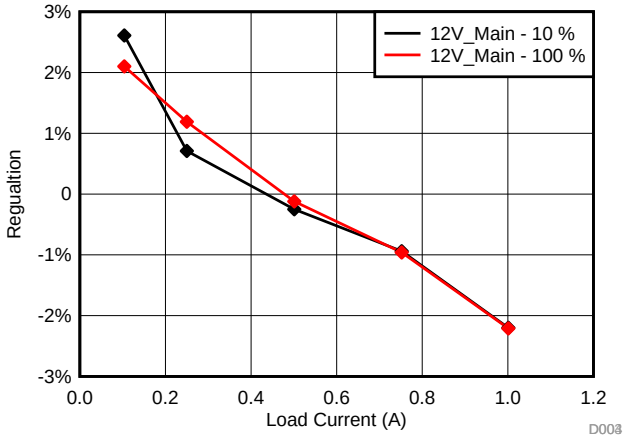


Figure 9. Cross Regulation of 12V_ISO

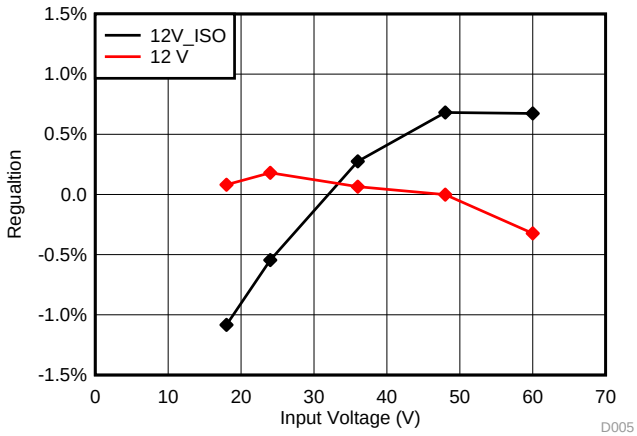


Figure 10. Line Regulation at Full Load

4.3 Functional Waveforms

4.3.1 Flyback MOSFET Switching Node Waveforms

Waveforms at the flyback switching (SW) node were observed along with the MOSFET current for 24 V and 48 V under full load conditions.

Figure 11 and Figure 12 show the SW node waveform along with the MOSFET current for a 24-V input and a 48-V input, respectively, with all the rails fully loaded.

NOTE: Green trace: Drain-to-source voltage, 20 V/div

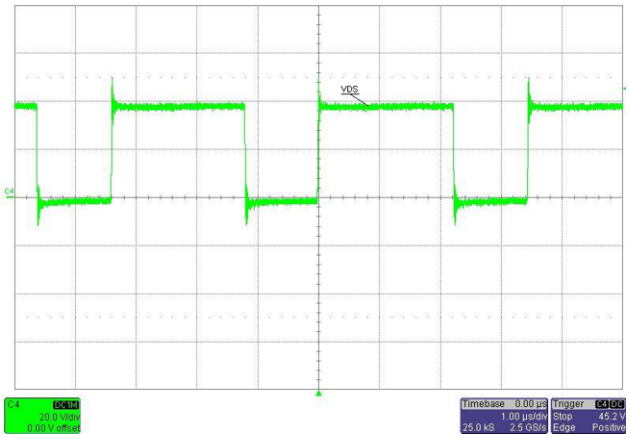


Figure 11. SW Node Waveform V_{IN}= 24 V, Full Load

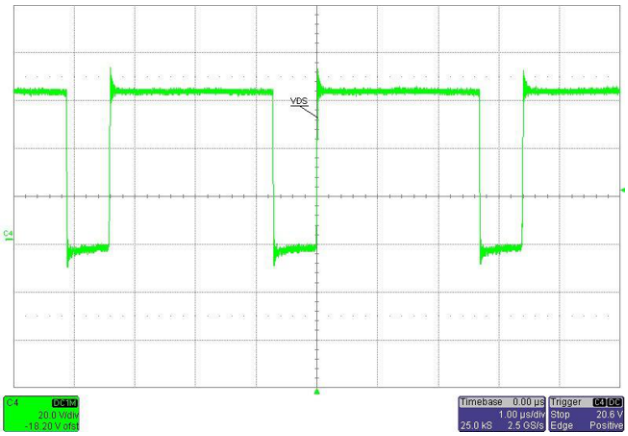


Figure 12. SW Node Waveform V_{IN}= 48 V, Full Load

Figure 13 and Figure 14 show the VDS turnon and turnoff waveforms at a 48-V DC input voltage and full load.

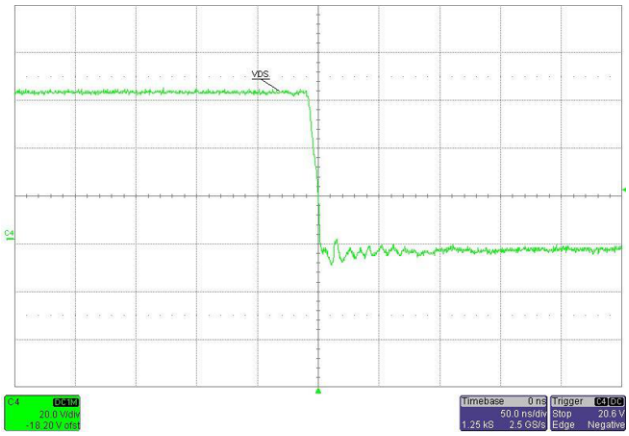


Figure 13. V_{DS} Turnon Waveform at 48-V Input

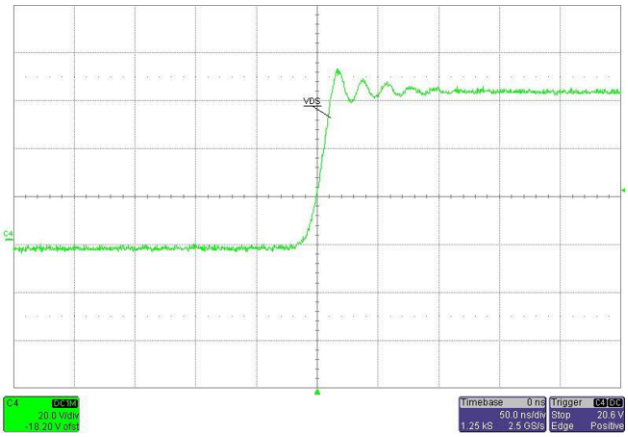


Figure 14. V_{DS} Turnoff Waveform at 48-V Input

4.3.2 Rectifier Waveforms

Waveforms at the anode of both the rectifier diodes were observed at 48 V under full load conditions

Figure 15 and Figure 16 show the voltages across diode D1 and diode D2 at 48 V, respectively, with both rails fully loaded.

NOTE: Green trace: Diode Voltage, 20 V/div

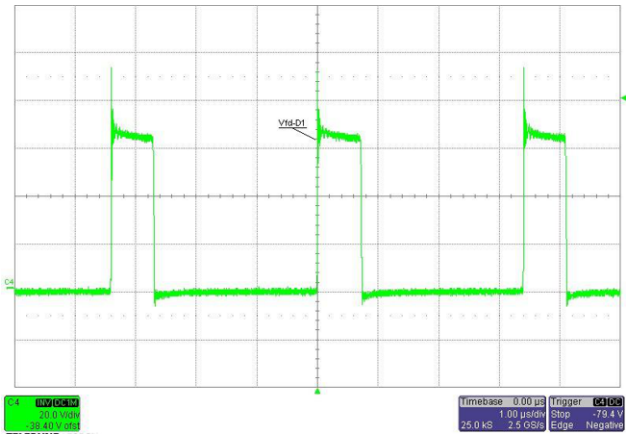


Figure 15. Voltage Across Diode D1 at 48-V Input at Full Load

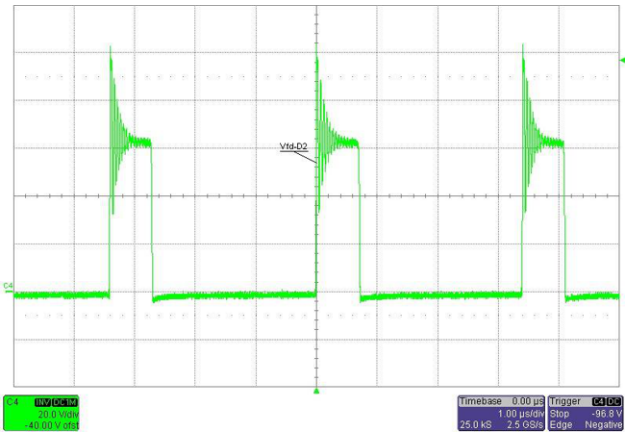


Figure 16. Voltage Across Diode D2 at 48-V Input at Full Load

4.3.3 Output Ripple

For the following figures, the ripple was observed at both the outputs at full load with a 48-V input voltage.

The peak-to-peak ripple voltage is around 100 mV for the 12-V_Main output and around 25 mV for 12-V_ISO.

Figure 17 and Figure 18 show the ripple for 12-V_Main/3-A rail and 12-V_ISO/1-A rail, respectively.

NOTE: Red trace: Output Ripple, 50 mV/div

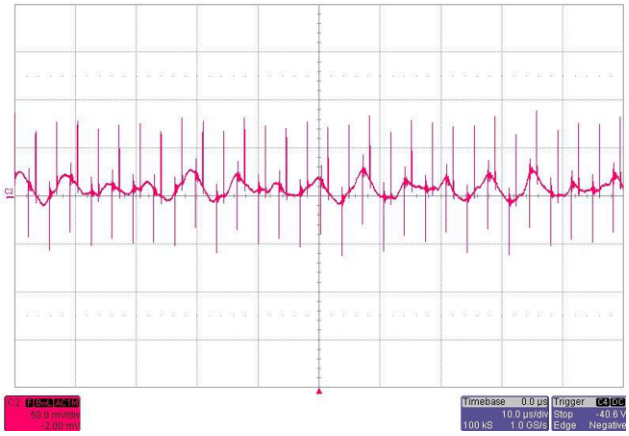


Figure 17. 12-V_Main Output Ripple at V_{IN}= 48 V and Full Load

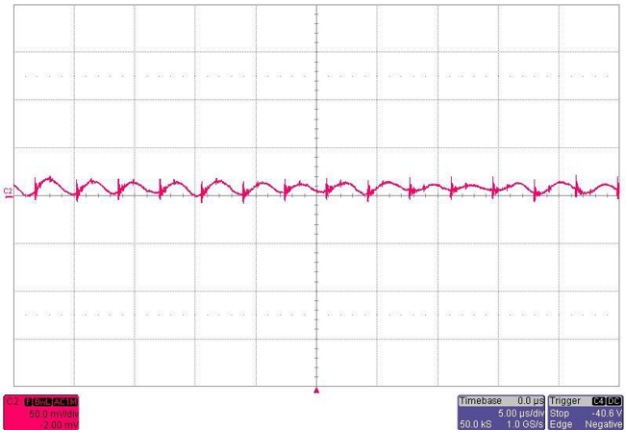


Figure 18. 12-V_ISO Output Ripple at V_{IN}= 48 V and Full Load

4.4 Transient Waveforms

4.4.1 Turnon Characteristics

The output turnon waveforms were observed with a resistive load. Figure 19 and Figure 20 show the turnon waveform at the 12-V_Main/3-A and 12-V_ISO/1-A outputs at 48-V input voltage and full load, respectively.

NOTE: For Figure 19 – Red trace: Output voltage, 5 V/div; Green trace: Output current, 2 A/div
For Figure 20 – Red trace: Output voltage, 5 V/div; Green trace: Output current, 500 mA/div

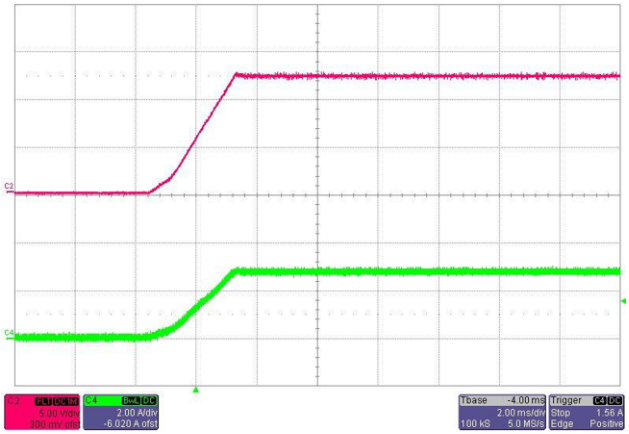


Figure 19. 12-V_Main and 3-A Output Turnon Waveform at 48 V

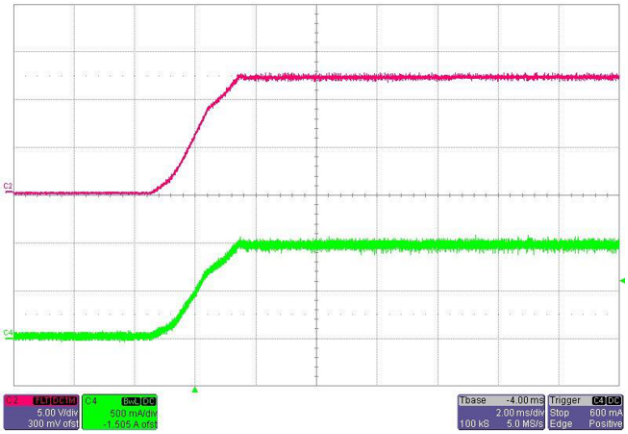


Figure 20. 12-V_ISO and 1-A Output Turnon Waveform at 48 V

4.4.2 Turnoff Characteristics

The output turnoff waveforms were observed with a resistive load. Figure 21 and Figure 22 show the turnoff waveform at the 12-V_Main/3-A and 12-V_ISO/1-A outputs at 48-V input voltage and full load, respectively.

NOTE: For Figure 21 – Red trace: Output voltage, 5 V/div; Green trace: Output current, 2 A/div
For Figure 22 – Red trace: Output voltage, 5 V/div; Green trace: Output current, 500 mA/div

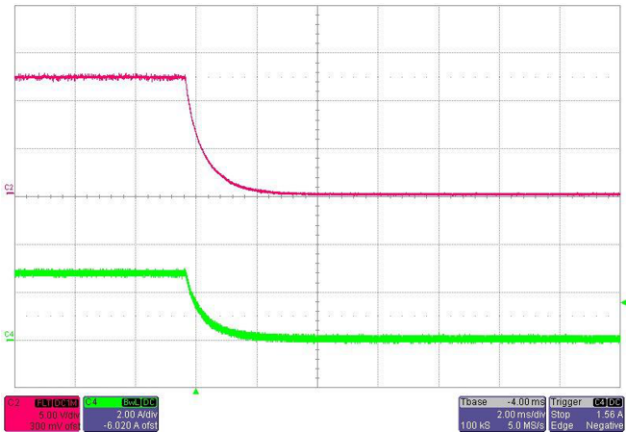


Figure 21. 12-V_Main and 3-A Output Turnoff Waveform at 48 V

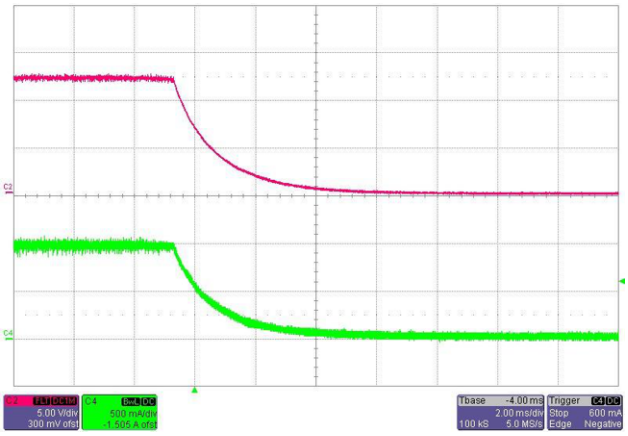


Figure 22. 12-V_ISO and 1-A Output Turnoff Waveform at 48 V

4.4.3 Transient Load Response

The load transient performance was observed for both the rails with the load switched at a 0.2-m wire length. The load transient was observed with the output switched on from 10% to 100% and switched off back to 10% load.

Figure 23 and Figure 24 show the transient load response for the 12-V_Main output at an input voltage of 48 V with a load transient from 0.275 A to 2.75 A and vice versa.

NOTE: Red trace: Output voltage, 500 mV/div; Green trace: Output current, 2 A/div

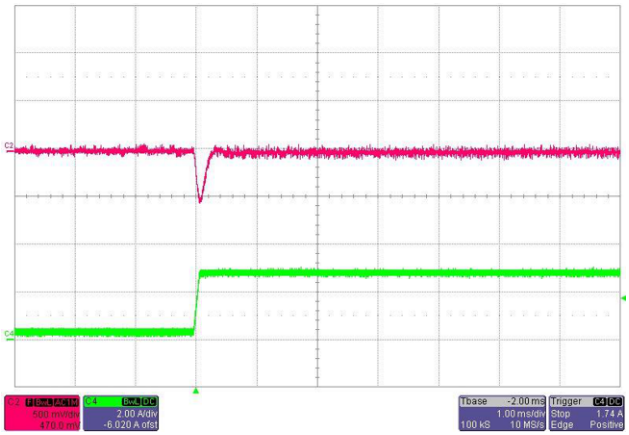


Figure 23. 12-V_Main Output Waveform—Load Transient From 0.3 A to 3 A

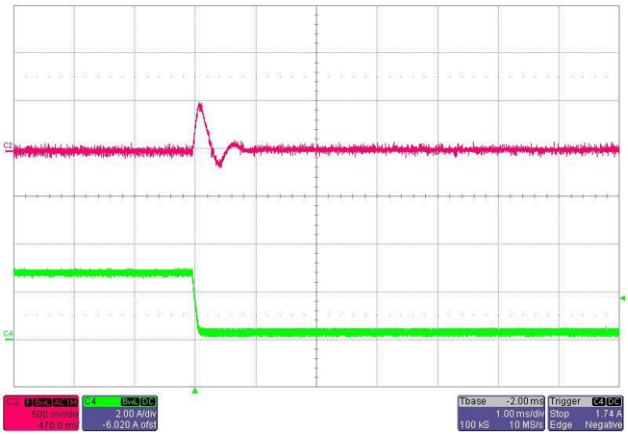


Figure 24. 12-V_Main Output Waveform—Load Transient From 3 A to 0.3 A

Figure 25 and Figure 26 show the transient load response for the 12-V_ISO output at an input voltage of 48 V with a load transient from 0.1 A to 1 A and vice versa.

NOTE: Red trace: Output voltage, 500 mV/div; Green trace: Output current, 2 A/div

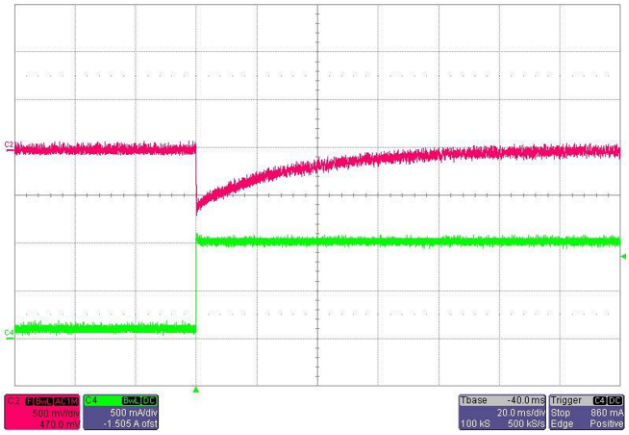


Figure 25. 12-V_ISO Output Waveform—Load Transient From 0.1 A to 1 A

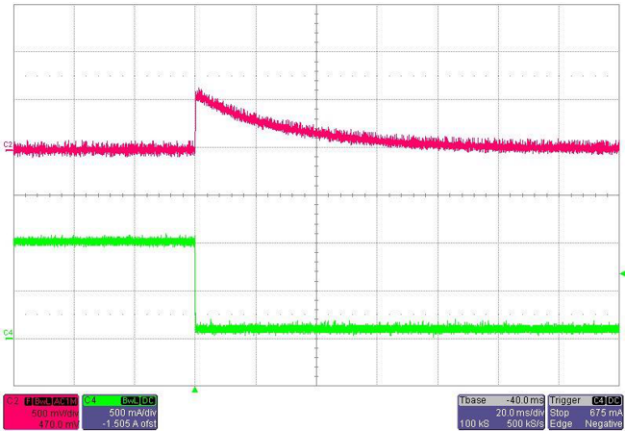


Figure 26. 12-V_ISO Output Waveform—Load Transient From 1 A to 0.1 A

4.4.4 UVLO Condition

The ULVO protection of the LM5020 controller was observed by turning the input voltage on and off and observing the 12V_Main output voltage during the turnon and turnoff.

Figure 27 and Figure 28 show the turnon and turnoff of the input voltage, respectively.

NOTE: Red trace: Output voltage, 5 V/div; Green trace: Input voltage, 10 V/div

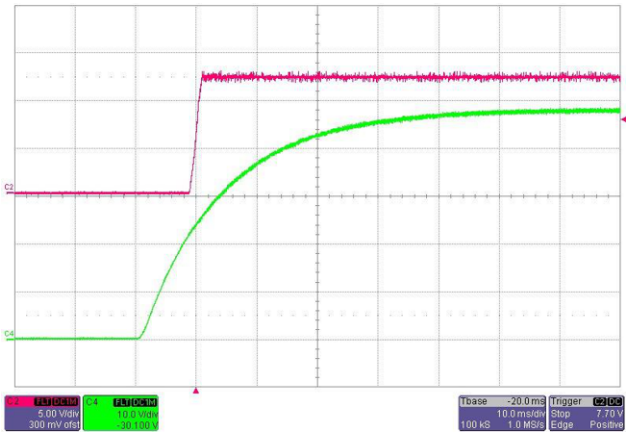


Figure 27. 12-V_Main Output Waveform—Turnon of Input Voltage

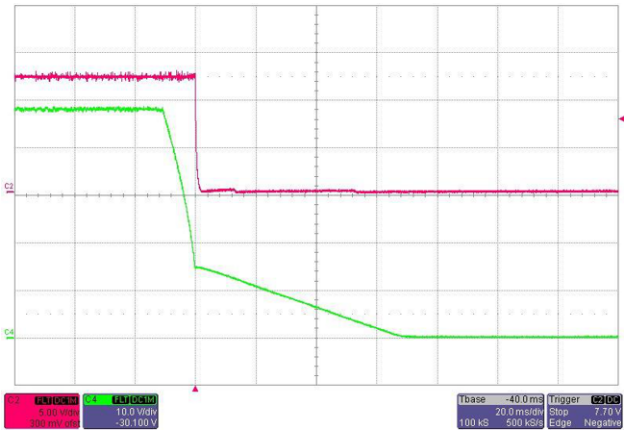


Figure 28. 12-V_Main Output Waveform—Turnoff of Input Voltage

4.5 Conducted Emissions

The test for measuring conducted EMI was performed at an input voltage of 24 V and with a full load across both outputs. The conducted emissions in a pre-compliance test setup were compared against EN55011 class-A limits and found to meet the class-A limits comfortably.

The results of the test are shown in the following Figure 29, Figure 30, Figure 31, and Figure 32. The figures show the peak and average emissions on both input positive and negative.

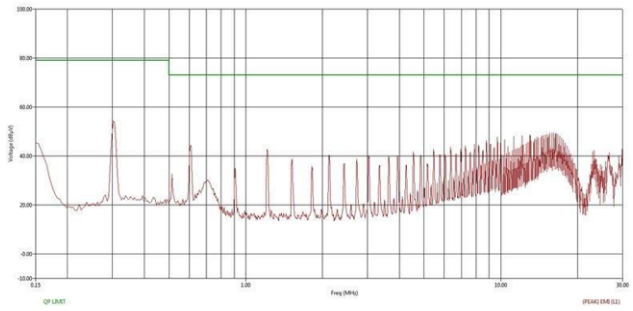


Figure 29. Peak on Positive Input

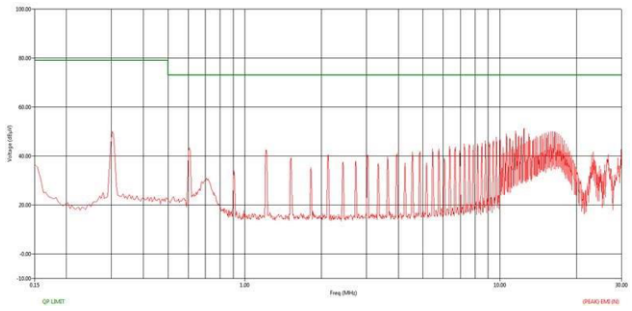


Figure 30. Peak on Negative Input

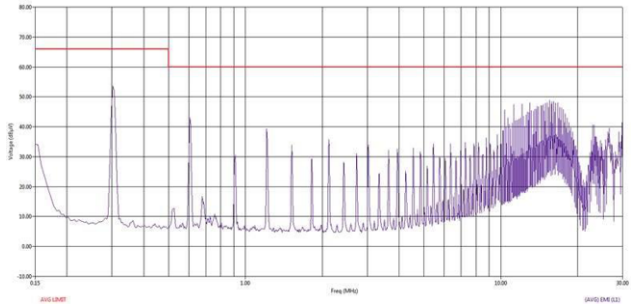


Figure 31. Average on Positive Input

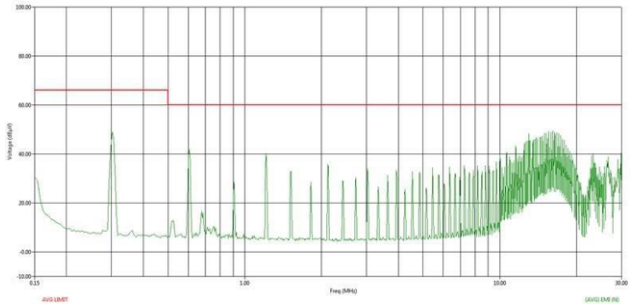


Figure 32. Average on Negative Input

NOTE: Figure 29 through Figure 32 are conducted emissions as per EN55011 Class A.

4.6 Thermal Measurements

The thermal measurements were performed at room temperature (25°C) with a 48-V input voltage after allowing the board to run for half an hour.

Figure 33 shows the bottom-side thermal images of the TIDA-00711 device at 36 W (12V_Main/2A and 12V_ ISO/1A) without any external cooling (0 LFM).

Figure 34 shows the bottom-side thermal images of the TIDA-00711 device, at 50 W (12V_Main/3A and 12V_ ISO/1A) with external cooling from a fan placed at a 10-cm distance from the board, which is controlled to provide 200 LFM of airflow.

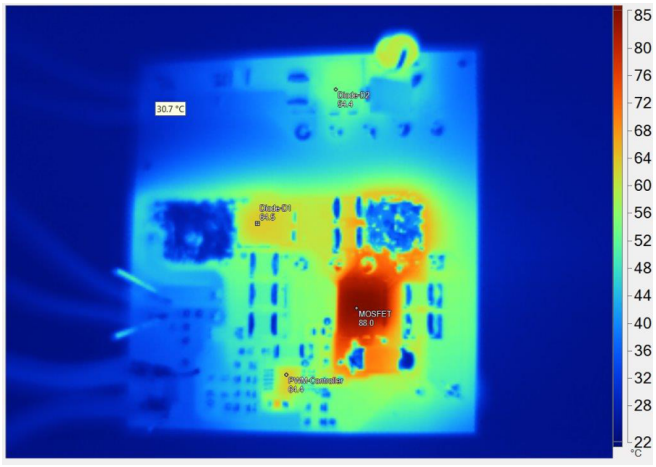


Figure 33. Bottom-Side Thermal Image at 48-V Input, 36 W, and Without Fan

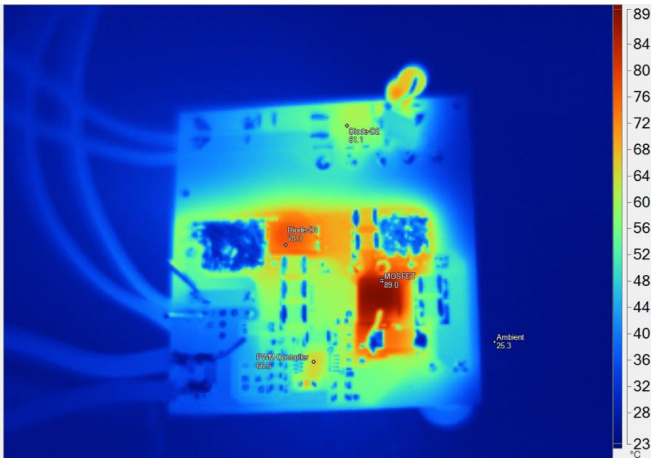


Figure 34. Bottom-Side Thermal Image at 48-V Input, 50 W, and With Fan

Table 9. Highlighted Image Markers for Figure 33 and Figure 34

NAME	TEMPERATURE (AT 48-V INPUT, 36 W, 0 LFM, NO AIRFLOW)	TEMPERATURE (AT 48-V INPUT, 50 W, WITH 200-LFM AIRFLOW)
MOSFET	88.0°C	89.0°C
PWM controller	64.4°C	66.6°C
Diode D1	64.5°C	78.3°C
Diode D2	54.4°C	61.1°C

4.7 Overcurrent Protection Test

Figure 35 shows the overcurrent protection for 150% overload on the 12-V main output. The red waveform is the 12-V main output and the green waveform is the current.

Figure 36 shows the overcurrent protection for 250% overload on the 12-V isolated rail. The red waveform is the 12-V isolated rail and the green waveform is the current.

NOTE: Red trace: Voltage, 5 V/div; Green trace: Current, 2 A/div

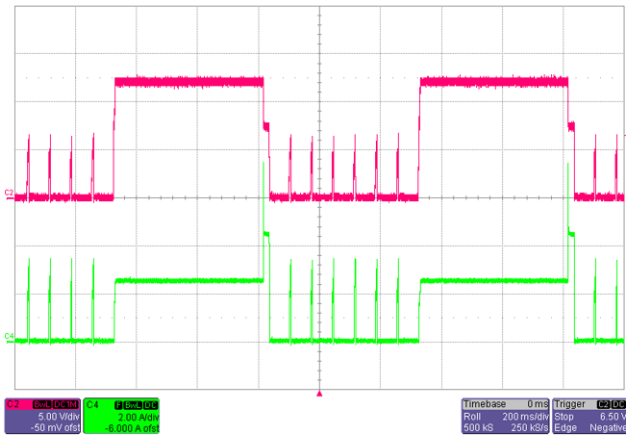


Figure 35. Overcurrent Protection for 12-V Main Output

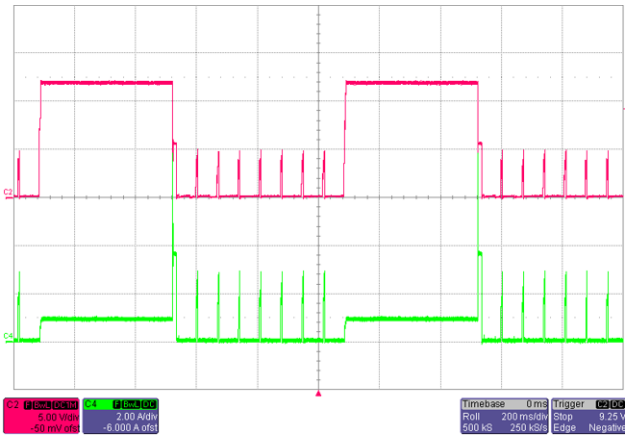


Figure 36. Overcurrent Protection for 12-V Isolated Rail

5 Design Files

5.1 Schematics

To download the schematics, see the design files at TIDA-00711.

5.2 Bill of Materials

To download the bill of materials (BOM), see the design files at TIDA-00711.

5.3 PCB Layout Recommendations

A careful PCB layout is critical and extremely important in a high-current fast-switching circuit to properly operate the controller devices and attain the robust nature of the design. As with all switching power supplies, attention to detail in the layout can save much time in troubleshooting later on. A proper layout also aids in maximizing efficiency and preventing radiation of high-frequency resonance problems; for these reasons, proper layout of the high-frequency switching path is essential.

5.3.1 Specific Guidelines for Power Stage

Follow these key guidelines to route power stage components:

- Minimize the loop area and trace length of the power path circuits, which contain high-frequency switching currents. This step reduces EMI and improves the overall performance of the converter.
- Keep the switch node as short as possible. A short and optimal trace width helps to reduce induced ringing caused by parasitic inductance.
- Keep traces with high dV/dT potential and high dI/dT capability away from or shielded from sensitive signal traces with adequate clearance and ground shielding.
- For each power supply stage, keep the power ground and control ground separate. Tie them together (if they are electrically connected) at one point near the DC input return or output return of the given stage.
- When multiple capacitors are used in parallel for current sharing, maintain the symmetrical layout across both leads of the capacitors. If the layout is not identical, the capacitor with the lower series trace impedance experiences higher peak currents and become hotter (i2R).
- Choose the width of PCB traces based on the acceptable temperature rise at the rated current as per IPC2152 as well as acceptable DC and AC impedances. The traces should also be able to withstand the fault currents (such as short-circuit current) before the activation of electronic protections, such as a fuse or circuit breaker.
- Adapt thermal management to fit the end-equipment requirements.

5.3.2 Specific Guidelines for Controller

Follow these key guidelines to route controller components and signal circuits:

- The optimum placement for the decoupling capacitor is closest to the VCC/VDD and GND terminals of the device. Minimize the loop area formed by the bypass-capacitor connection and the GND terminal of the IC.
- Make the reference ground for the control devices a low-current signal ground (SGND), copper plane, or island.
- Place all controller-support components at specific signal pins close to their respective connection pins.
- Connect the other end of the component to the SGND with the shortest trace length possible.
- The trace routing for the voltage-sensing and current-sensing circuit components to the device should be as short as possible to reduce parasitic effects on the current limit and current and voltage monitoring accuracy. These traces should not have any coupling to switching signals on the board
- Connect the SGND plane to high current ground (main power ground) at a single point that is at the negative terminal of the DC I/O capacitor, respectively.

- If an overlap exists, keep the signal traces perpendicular to high frequency and the high-current traces perpendicular to signal traces instead of parallel. Shielding the signal traces with ground traces can help to reduce noise pickup.
- See the placement and routing guidelines and layout example in the LM5020 datasheet.

5.3.3 Layout Prints

To download the layer plots, see the design files at TIDA-00711.

5.4 Altium Project

To download the Altium project files, see the design files at TIDA-00711.

5.5 Gerber Files

To download the Gerber files, see the design files at TIDA-00711.

5.6 Assembly Drawings

To download the assembly drawings, see the design files at TIDA-00711.

6 References

1. Texas Instruments, *LM5020 100V Current Mode PWM Controller*, LM5020 Datasheet (SNVS275)
2. Texas Instruments, *CSD19534Q5A 100 V N-Channel NexFET™ Power MOSFETs*, CSD19534Q5A Datasheet (SLPS483)
3. Texas Instruments, *Using the TPS55340 as a SEPIC Converter, Application Report*, TPS55340 Application Report (SLVA516)
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5. Texas Instruments, *Benefits of a coupled-inductor SEPIC converter*, Technical Brief (SLYT411)
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6.1 Trademarks

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7 About the Authors

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2016) to A Revision	Page
• Added updated images for optimized resolution and lower file sizes	1

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