LM5036

Half-Bridge PWM Controller with Integrated Auxiliary Supply

New Product Overview

Texas Instruments

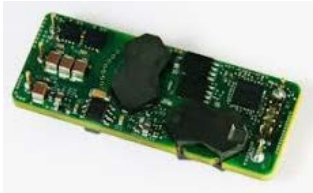
Topics

LM5036 Overview	• Key features, Use cases • Device introduction • EVM, Sample, Reference design, Calculator tools, Simulation models, Webench • Companion parts to use • TI Half-Bridge controller positioning
LM5036 Training	• Summary of features and benefits • Pin configuration • Integrated auxiliary bias power, Fully regulated pre-bias start-up, Cycle-by-Cycle current limit and Pulse matching, OCP hiccup, Optimized maximum duty cycle, fault latching • High voltage start-up, UVLO, OVP, OTP, use when VIN > 100V, synch'ed clock, etc.
Half-bridge, Active Clamp Forward Comparison	• Half-bridge, Active Clamp Forward pros and cons • An example to compare efficiency with HF and ACF designs • TI Half-Bridge and Active Clamp controller positioning

LM5036 Overview

LM5036 is a highly integrated half-bridge PWM controller with integrated auxiliary bias supply which offers high power density solutions for

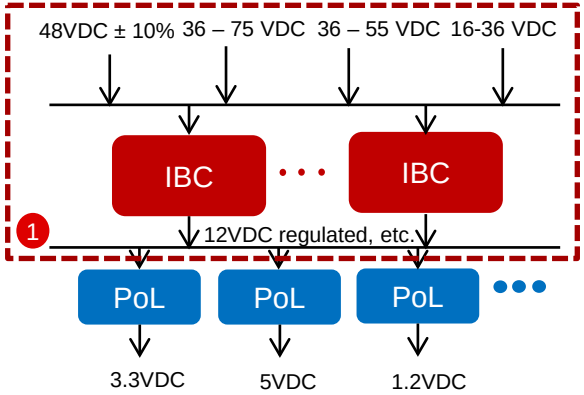
- Telecom isolated power suppliers
- Data communication isolated power suppliers
- Industrial and transport power converters

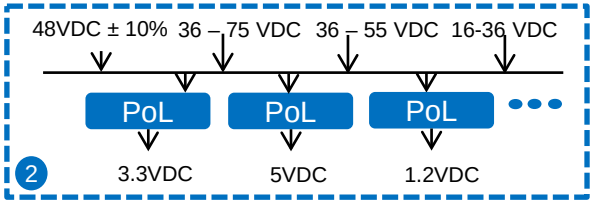


LM5036 is commonly used in:

1. **Intermediate bus converter (IBC)**
2. **Point of Load converter (PoL)**

LM5036 contains all of the features necessary to implement half-bridge topology power converters using voltage-mode control for **60W to 500W isolated DCDC**. This device is intended to operate on the primary side with input voltage up to 100V. LM5036 can also be used in full-bridge controller for higher power level and also support > 100V input as needed.





LM5036 Top Features

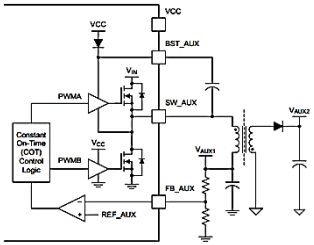
High Power Density

>390W/in^3 High power-density isolated DC/DC (48V_{in}/200W,12V_{out})

>200W in DOSA 1/16 brick

100V Half-Bridge PWM With 2A integrated Gate Drivers & 100mA Auxiliary Bias.

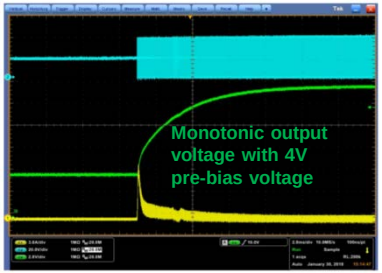
Low System Cost



Integrates a Fly-buck converter inside LM5036 to provide auxiliary bias to power on both primary and secondary sides

Built-in Fly-buck converter with integrated power MOSFETs, high + low side drivers, current sense.

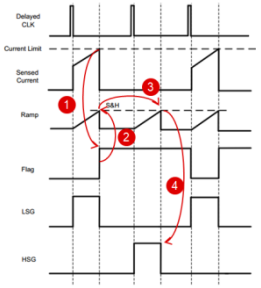
Solve Pre-bias Start-up Challenge



Achieves monotonic output voltage ramp up in pre-bias condition.

Intelligent pre-bias start-up procedure to eliminate the risk of restarting the load or damaging the DCDC converter.

High Reliability



Programmable protections to secure reliability

- **Almost constant output power/current limit across wide VIN range.**
- **Both positive and reverse current protection and hiccup OCP.**
- **High/low PWMs matching in OCP.**
- **OVP, OTP, ULVO, latching, etc.**

LM5036

Half-Bridge PWM Controller with Integrated Auxiliary Bias Supply

Features

- 100V auxiliary bias converter (with integrated FETs for aux power)
- Fully regulated pre-biased start-up
- 5V synchronous rectifier PWM outputs with intelligent soft start that allows linear turn-on into pre-biased loads
- Enhanced cycle-by-cycle current limit with pulse matching
- Programmable latching operation
- Optimized maximum duty to improve efficiency
- 100V high voltage startup regulator
- Programmable synchronous rectifier dead time adjustments
- Integrated 100V/2A MOSFET drivers for primary FETs
- Voltage mode control with input voltage feedforward
- Programmable protections: reverse current, hiccup mode OCP, line UVLO and OVP
- Package: 5x5 mm 28-pin QFN

Applications

- Isolated DC/DC brick modules (e.g. 1/16th & 1/8th Brick)
- Telecom, Data Communication Systems
- Industrial Power Supplies

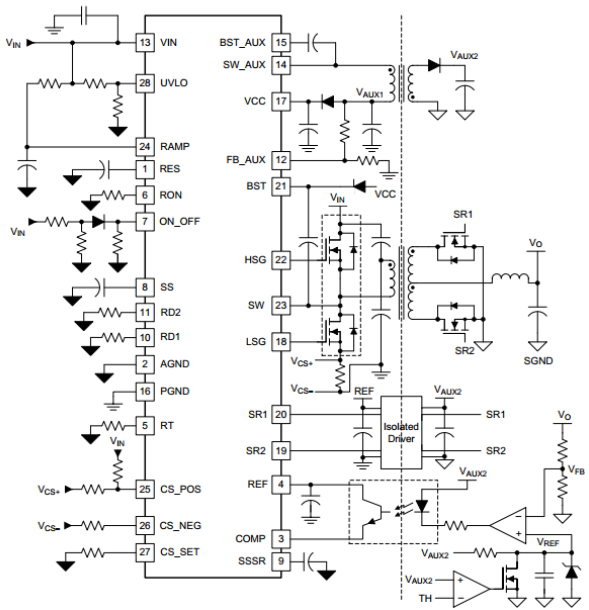
LM5036 product folder Datasheet EVM Simplis Model Design Calculator

Function Block Diagram

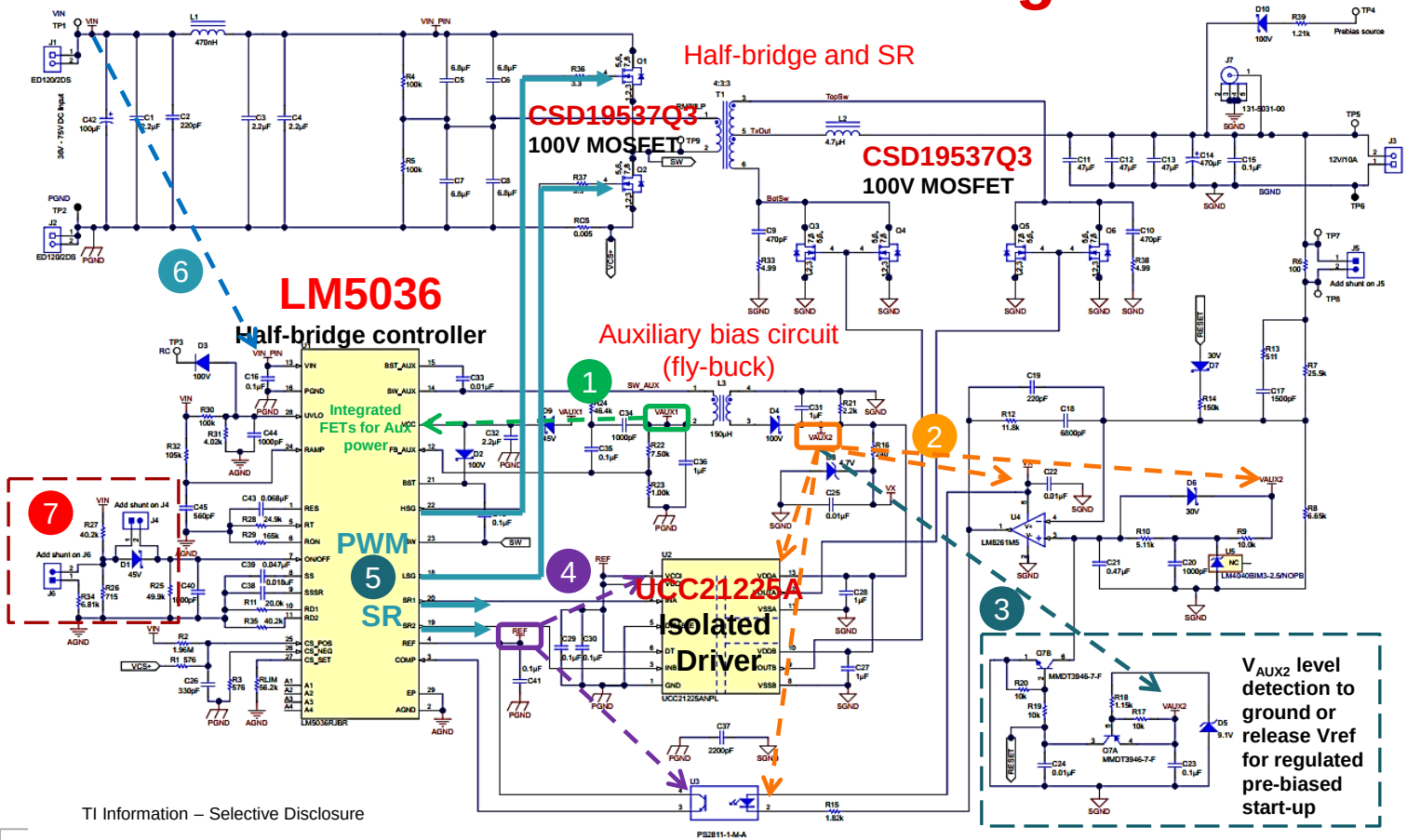
Benefits

- Higher efficiency and greater power density
- Monotonic startup into pre-biased load conditions
- Enhanced OCP with uniform current limit across input voltage range

Simplified Application



LM5036 DCDC Converter Design

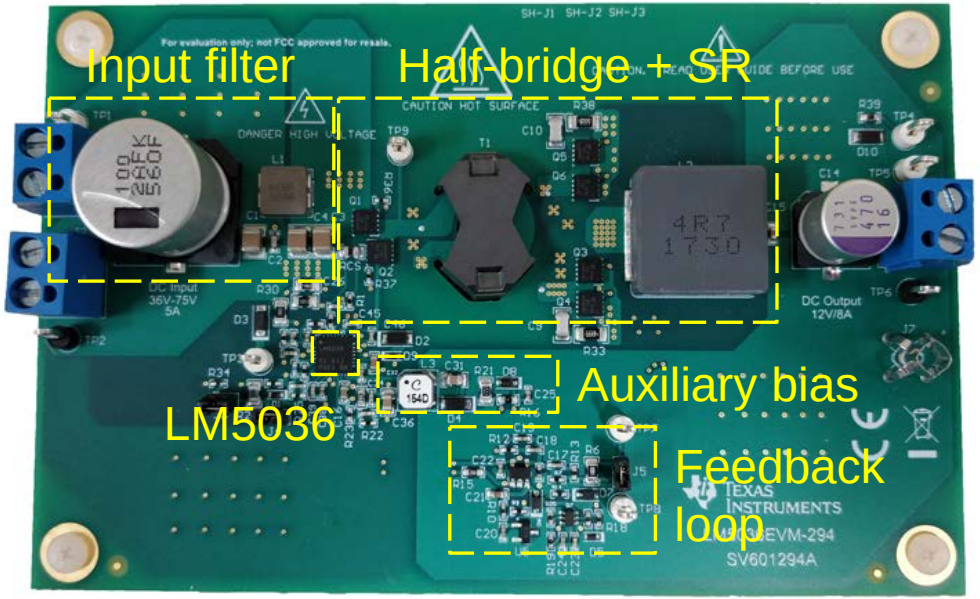


1. V_{AUX1} power to power on LM5036.
2. V_{AUX2} to power isolated driver, opto-coupler, op-amp, etc.
3. V_{AUX2} is also used as ENABLE signal in regulated pre-bias start-up. (more info)
4. 5V REF to bias isolated driver, opto-coupler, and for other housekeeping ICs.
5. 2A primary side FETs drivers. SR outputs.
6. Up to direct 100V VIN range.
7. Configurable Latch or re-start. (more info)

Used in LM5036EVM-294 Design
(36-75 VDC input, 12V/8A output)

Support: E2E AC/DC and Isolated DC/DC Power Forum

LM5036 EVM, Samples



- http://www.ti.com/tool/LM5036EVM-294
- EVM User Guide
- Samples, TI Store (up to 9999 pcs)

EVM Spec

Parameters	Test Conditions	MIN	TYP	MAX	Units
Input Characteristics					
DC voltage range		36	48	75	VDC
Load regulation			0.2%		
Line regulation			0.1%		
UVLO line voltage ON			34		VDC
UVLO line voltage OFF			32		VDC
OVP line voltage ON			80		V
OVP line voltage OFF			78		V
Latch threshold			80		V
V_{AUX1}	Off-state auxiliary output voltage		12.6		V
	On-state auxiliary output voltage		9		V
Max. load current for auxiliary supply			100		mA
Input DC current	Input = 36 VDC, full load = 8 A		2.858		A
	Input = 48 VDC, full load = 8 A		2.161		A
	Input = 75 VDC, full load = 8 A		1.416		A
Output Characteristics					
Vout output voltage	No load to full load = 8 A		12		VDC
Iout output current	35 to 75 VDC			8	A
Output current limit	35 to 75 VDC		10		A
Output voltage ripple	75 VDC and full load = 8 A		120		mVpp
System Characteristics					
Switching frequency			200		kHz
Peak efficiency	36 VDC, Load = 5.5 A		94.41%		
Maximum load efficiency	48 VDC, Load = 8 A		93.46%		
Operating temperature	Natural convection	–40		85	°C

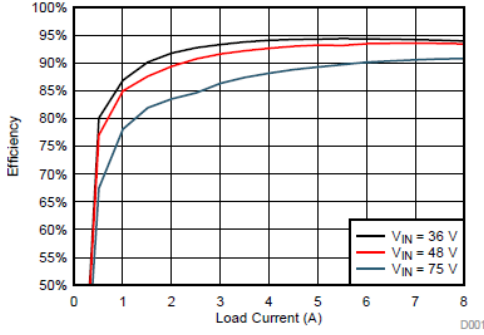


Figure 3. Efficiency vs Load Current (A) at Vin = 36 VDC, 48 VDC, and 75 VDC

PMP40500/ *54Vdc Input, 12V42A Output Half-Bridge Reference Design*

Design Status: (available)

TIDesigns

Features

- 100V auxiliary bias converter
- Peak Efficiency Up to 94.62%
- L*W*H=122mm*59mm*20mm
- Enhanced cycle-by-cycle current limit with pulse matching
- Fully regulated pre-biased start-up

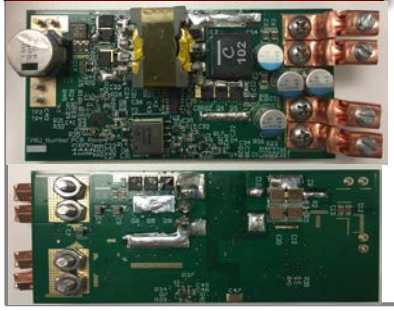
Benefits

- Hight efficiency and greater power density
- Good thermal performance
- Suitable for compact form
- Enhanced OCP with uniform current limit across input voltage range
- Monotonic startup into pre-biased load conditions.

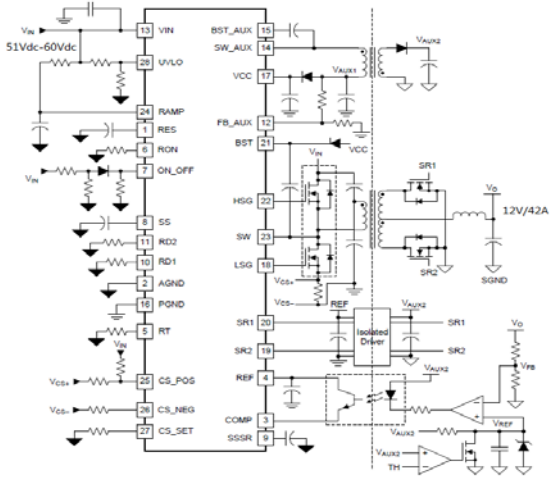
Target Applications

- Telecom, Data Communication System
- Isolated DC/DC brick modules

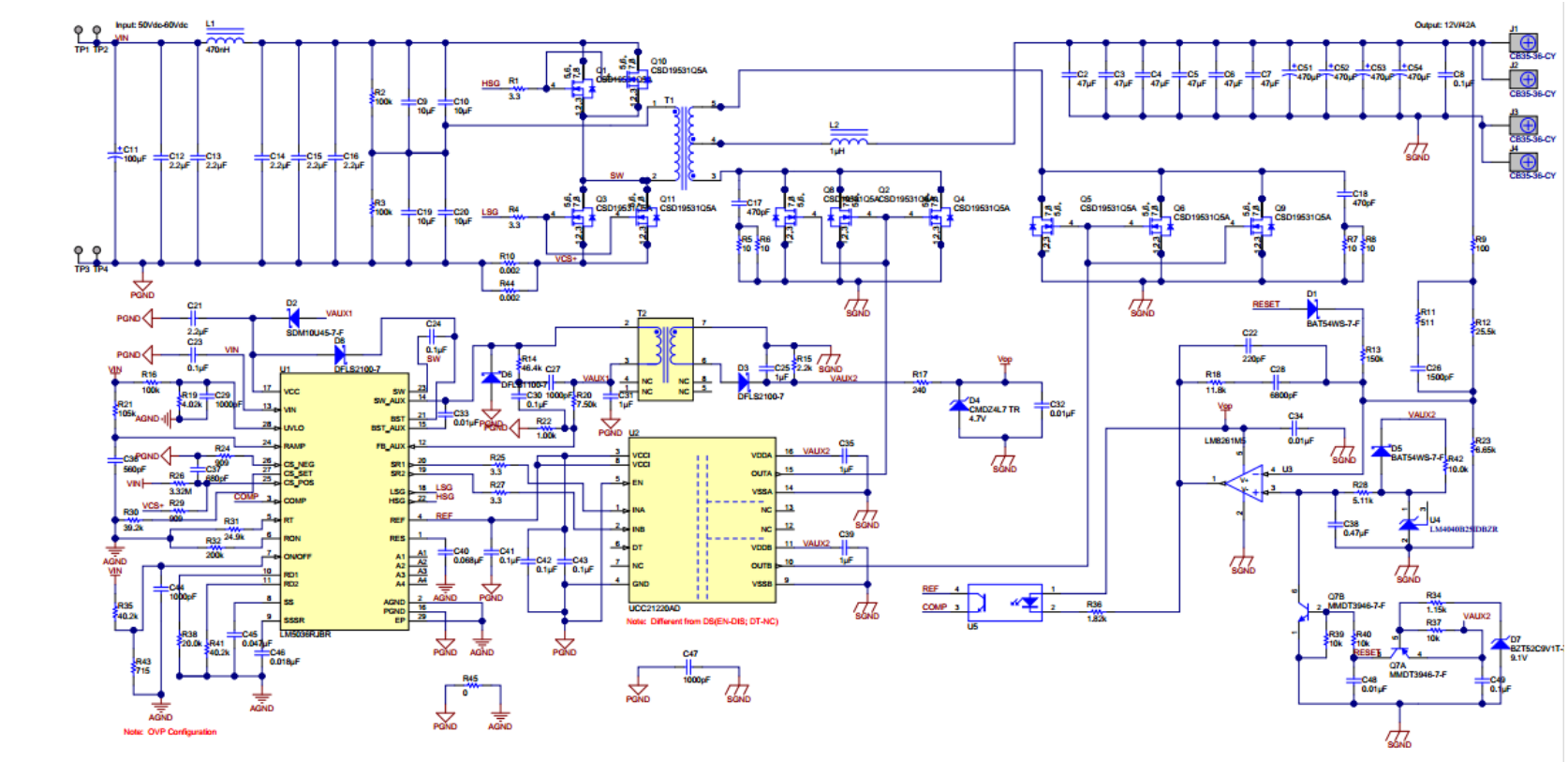
Tools & Resources



- **PMP40500 Tools Folder**
  - Relevant Design Files
- **Design Files:** Schematics, BOM, Gerbers, and more
- **Device Datasheets:**
  - LM5036RJBR
  - UCC21220AD
  - CSD19531Q5A
  - LM8261M5
  - LM4040B25IDBZR



PMP40500 500W design is similar as 100W EVM



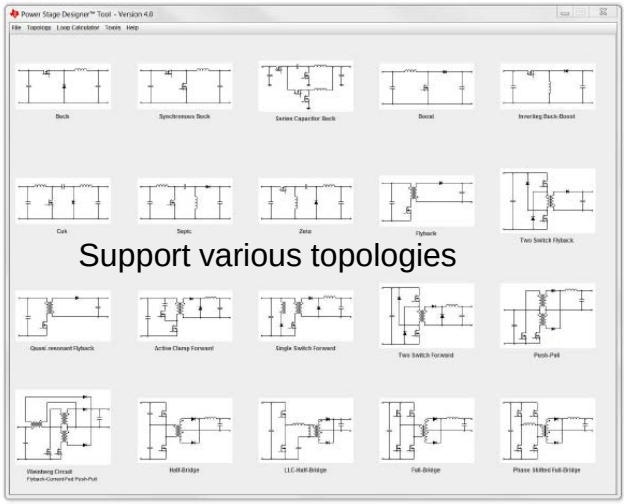
LM5036 Design Calculator

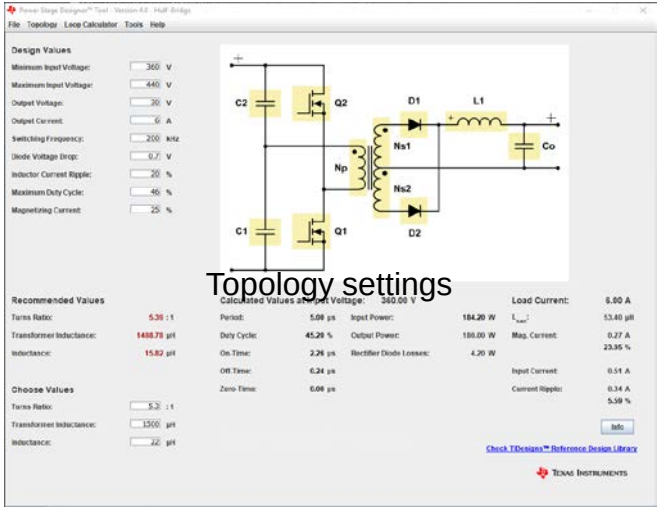
	Parameter	Parameter Designator	User Input and Calculated Values	Unit		Intermediated Calculated Values (no edit in this column)	Comments
Design Specifications							
Input design specifications	$V_{IN(min)}$		36.0	V	1.0E+00	36	Min Input Voltage
	$V_{IN(nom)}$		48.0	V	1.0E+00	48	Nominal Input Voltage
	$V_{IN(max)}$		75.0	V	1.0E+00	75	Max Input Voltage
	$V_{IN(pk)}$		100.0	V	1.0E+00	100	Max Input Voltage (HB not operating)
	Vout		12.0	V	1.0E+00	12	Output Voltage
	ΔV_{RIP}		50.0	mV	1.0E-03	0.05	Max Output Voltage Ripple
	I_{LIM}		10.0	A	1.0E+00	10	Output Current Limit
	F_S		200	kHz	1.0E+03	200000	LM5036 Switching Frequency of Each Primary MOSFET.
	η		0.92		1.0E+00	0.92	Efficiency Target
MOSFET Parameters							
Primary MOSFET Parameters							
Input MOSFET parameters for the bridge	V_{GS_Qp}		9	V	1.0E+00		Primary FET gate drive voltage
	Q_{G_Qp}		16	nC	1.0E-09	1.60E-08	Primary FET gate charge
	C_{OSS_Qp}		251	pF	1.0E-12	2.51E-10	Primary FET output cap
	R_{dson_Qp}		12.1	mΩ	1.0E-03	0.0121	Primary FET Rdson
SR MOSFET Parameters							
Input MOSFET parameters for the SR	V_{GS_sr}		9	V	1.0E+00	9	SR FET gate drive voltage
	Q_{G_sr}		16	nC	1.0E-09	1.60E-08	SR gate charge
	R_{dson_sr}		12.1	mΩ	1.0E-03	1.21E-02	SR FET on resistance
	Q_{rr_sr}		134	nC	1.0E-09	1.34E-07	SR body diode reverse recovery charge

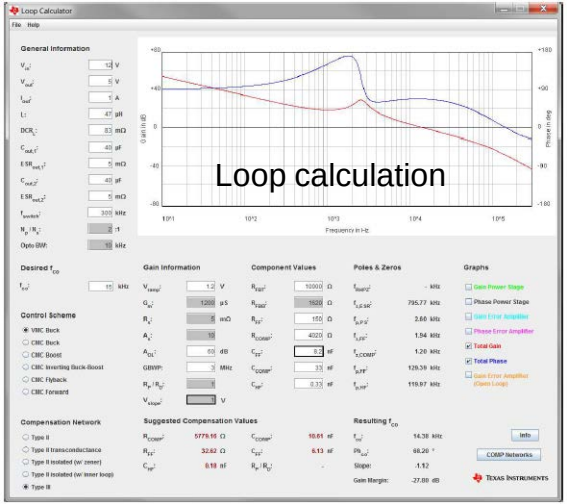
	Parameter	Parameter Designator	User Input and Calculated Values	Unit		Intermediated Calculated Values (no edit in this column)	Comments
Controller Configuration							
UVLO Configuration							
Calculate values of two resistors connecting to UVLO pin for UVLO voltage divider	Target UVLO Rising Threshold	VinUvloRise	34	V	1	34	Target input voltage at which Half Bridge will start operation
	Target UVLO Falling Threshold	VinUvloFall	32	V	1	32	Must be >15V and < VinUvloRise
	$V_{HYS(UVLO)}$		2	V	1	2	VinUvloRise - VinUvloFall
	R_{UV1}		100	kΩ	1000	100000	Upper resistor divider required to achieve specified UVLO hysteresis
	R_{UV1}	R30	100.00	kΩ	1000	100000	User selected value for R30 based on R30 calculation above
	R_{UV2}		4.07	kΩ	1000	4065.04	Lower resistor divider required to achieve specified OVP latch voltage threshold
	R_{UV2}	R31	4.02	kΩ	1000	4020	User selected value for R31 based on R31 calculation above
	Actual VinUvloRise	VinUvloRise	34.34	V	1	34.34	Half Bridge will start operation when VIN rises above this level
Over - Voltage / Latch (ON/OFF) Configuration							
Calculate values of resistors connecting to ON_OFF pin for OVP or Latch mode.	In the design example in datasheet and LM5036EVM-204 design, it uses jumper 4 and 6 to configure the design to work either in OVP mode or latch mode. For OVP mode, close jumper J4 and J6. In latch mode, open jumper J4 and J6. In OVP mode. Resistors R25, R26, R34 parallle to implement ROV2. In Latch mode, R26 - ROV2, R34 - RL.						
	OVP Rising Threshold	VinOvpRise	80	V	1	80	OVP Rise voltage threshold
	OVP Falling Threshold	VinOvpFall	78	V	1	78	OVP Fall voltage threshold (OVP mode only)
	$V_{HYS(OVP)}$		2	V		2	VinOvpRise - VinOvpFall
	R_L	R25	49.9	kΩ	1000	49900	Latch resistor must be > 33kΩ to ensure latched operation.
	R_{OV1}	R27	49.0	kΩ	1000	49000.00	This resistor sets hysteresis band between VIN_OVP_RISE and VIN_OVP_FALL
	V_F	D1	0.138	V	1.0E+00		Forward voltage drop of the latch diode (ON_OFF pin)
	$R_{OV2(latch)}$	R26	710.1	Ω	1	710.1	For latched operation use this value for R_{OV2}
	$R_{OV2(non\ latch)}$		634.9	Ω	1	634.9	For non-latched operation use this value for R_{OV2}
	Rx	R34	6.814	kΩ	1000	6813.860	Resistor value to add in parallel with R26 for jumper configurable operation.
Soft Start Capacitor							
Calcualte capacitor value at SS pin to set Soft start delay	Soft Start Delay	$t_{D(SS)}$	4.7	msec	0.001	0.0047	User specified soft-start delay time
	C_{SS}	C39	0.046	µF	0.000001	4.563E-08	Capacitor value required to achieve specified delay time
Soft Start SR Capacitor							
Calcualte capacitor value at SSSR pin to set SR Soft-start ramp.	SR Soft Start	t_{SSRP}	10	msec	0.001	0.010	Ramp time of output voltage
	SSSR Capacitor (C_{SSSR})	C38	10	nF	0.000000001	1.000E-08	Capacitance to achieve SSSR ramp in 25% of t_{SSRP}.
Current Sense and CBC Resistor							
Set current sense resistor Rcs and calculate values of resistors and capacitor connecting to CS_POS, CS_NEG and CS_SET pins based on selected	RMS current	Ics_rms_Vmin	6.00	A	1	6.00	RMS current is sense resistor at $V_{IN(min)}$ and ILIM
		Ics_rms_Vmax	3.47	A	1	3.47	RMS current is sense resistor at $V_{IN(max)}$ and ILIM
	Current sense resistor	Rcs_Vmin	26.67	mΩ	0.001	0.03	Current sense resistor value that will dissipate 0.5% P(out)max at $V_{IN(min)}$ and I(out)max
		Rcs	5	mΩ	0.001	0.005	User specified value of current sense resistor
	Power of CS	Pcs_Vmin	126.1	mW	0.001	0.1261	Power dissipation in Rcs resistor at $V_{IN(min)}$ and ILIM
		Pcs_Vmax	60.2	mW	0.001	0.0603	Power dissipation in Rcs resistor at $V_{IN(max)}$ and ILIM
	Inductor current slope	m_L	9.57	mV/µs	1.00E+03	9574.47	Down-Slope of output inductor transformed to primary side
		Ratio	1		1	1	User selected ratio of actual slope/m_ Should be > 0.6
	Resistor R_1 suggested to achieve Ratio	R_1	441.6	Ω	1	441.6	R_1 is determined based on the slope compensation requirement
	Resistor R_1 value selected	R1	576.0	Ω	1	576.0	R_1 value selected by user
	Resistor R_2 suggested value	R_2	2.32	MΩ	1000000	2316030.6	Calculated R_2 value
	Resistor R_2 value selected	R2	1.96	MΩ	1000000	1960000	R_2 value selected by user

- LM5036 Design Calculator (http://www.ti.com/lit/zip/sluc654) is an Excel worksheet that to help users to calculate most of the component values needed in the design without remembering the equations listed in datasheet.
- Users can just simply fill in the design spec (VIN range, Vout, Iout, switching frequency, etc.) and a few key settings (in yellow), this design calculator can calculate the components values that to meet the design spec, and also provide related parameters, such as power loss and efficiency estimation.
- Following are functions that covered in design calculator: input/output parameters, primary MOSFET losses, capacitive divider, current sense, output filter, auxiliary circuit, latch/OVP, UVLO, RAMP, Oscillator frequency, soft-start capacitor, SR soft-start, timing resistors, hiccup, CBC, etc.
- Download at: LM5036 Design Calculator
- Excel sheet is locked and protected to prevent accidently changing the embedded equations.
- Password to unlock the Excel protection to see the embedded equations in column G: *LM5036*

Power Stage Designer™ Tool of Most Commonly Used Switch-mode Power Supplies

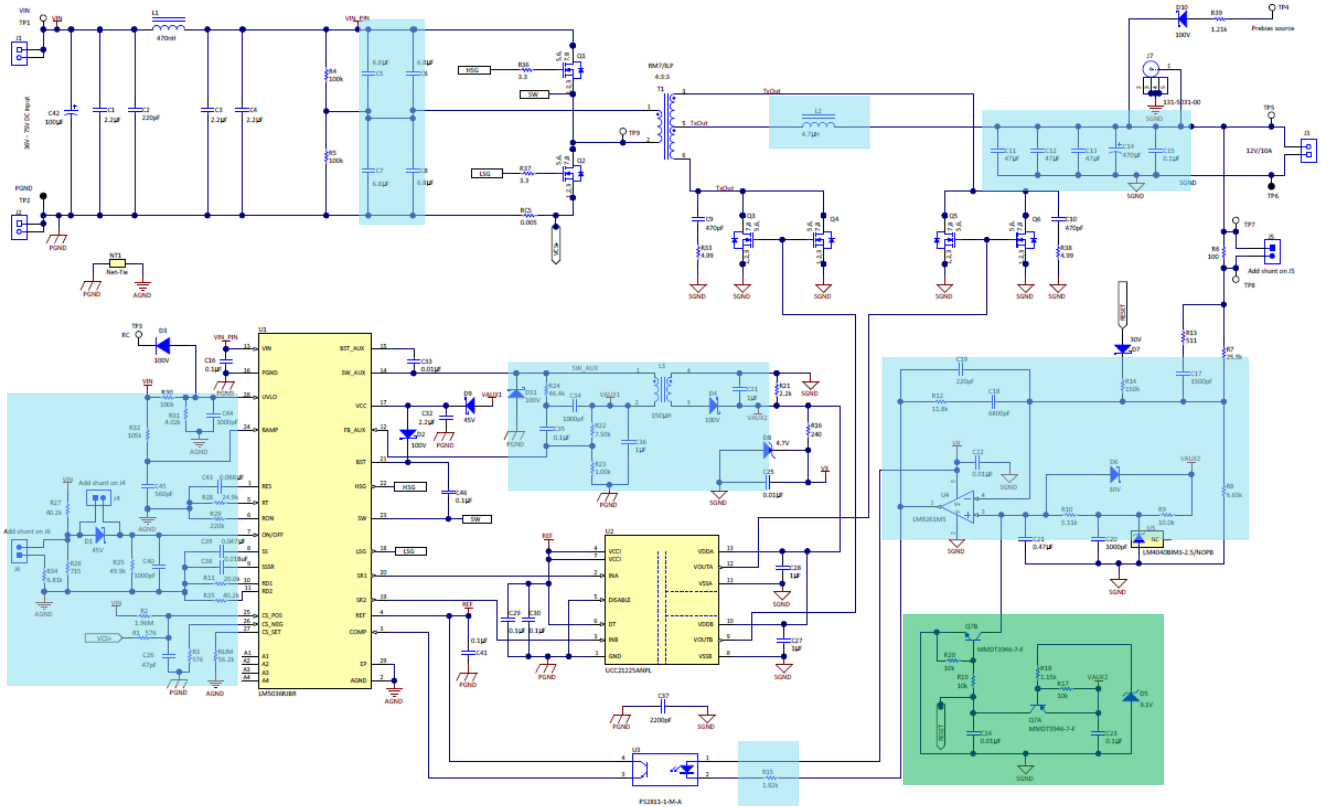






- Power Stage Designer™ is a Java® based *free tool* that helps engineers speed up their power supply designs as it calculates voltages and currents of 20 topologies according to the user's inputs.
- Additionally, PowerStage Designer contains a Bode plotting tool and a helpful toolbox with various functions for power supply design.
- More info and download from here: http://www.ti.com/tool/POWERSTAGE-DESIGNER

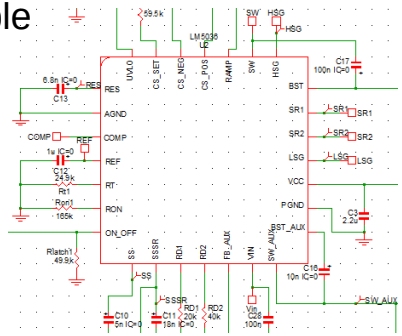
Using LM5036 Design Calculator and Power Stage Designer Tool



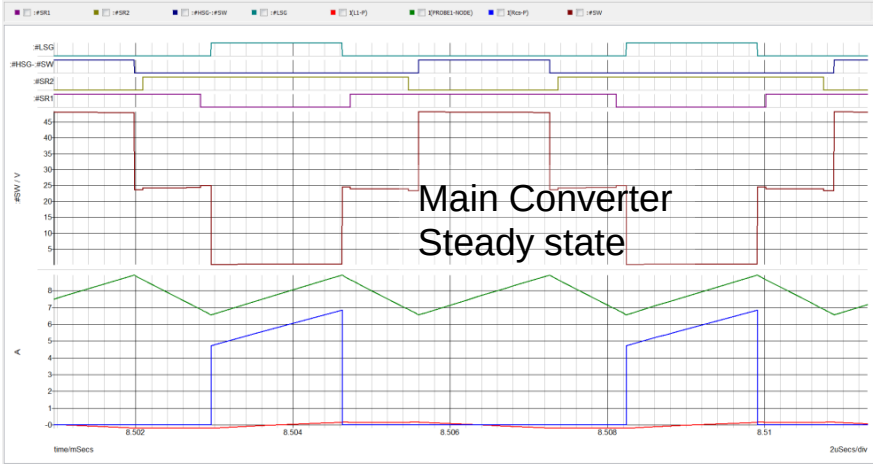
- By using LM5036 Design Calculator and Power Stage Designer Tool, all component values in the blue shaded circuits can be configured and generated.
- The green shaded circuit is level-shift detection circuit that can be copied from design example in datasheet.

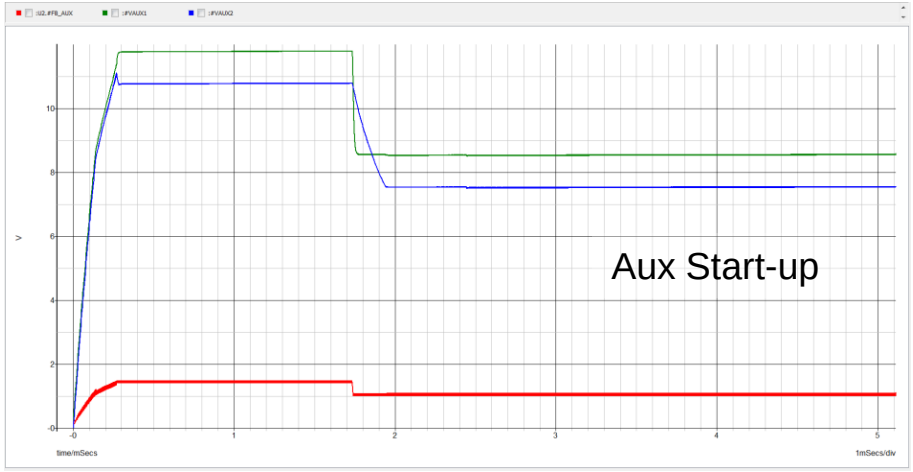
LM5036 Simulation Models

- Simplis Model and PSpice Model available to download: http://www.ti.com/product/LM5036/toolssoftware
- All features modelled including:
  - Integrated auxiliary power
  - Pre-biased start-up
  - Cycle-by-Cycle current limit
  - High voltage regulator



Title	Category	Type	Size (KB)
LM5036 PSpice Transient Model	PSpice Model	ZIP	1687 KB
LM5036 Macromodels Transient	Macromodels	ZIP	137 KB





LM5036 WEBENCH Tool

[Webench Tranining Video: Transformer Designer for Isolated High-Voltage Power Design]

WEBENCH® Designer LM5036

	Min		Max		Range
Vin	36.00	–	75.00	V	18.0 to 100.0V
Vout			12	V	3.3 to 95V
Iout			8	A	≤ 310A
Ambient Temp			30	°C	-40 to 125° C

Footprint	BOM Cost	Efficiency
1669.0mm²	$21.33	93.0%

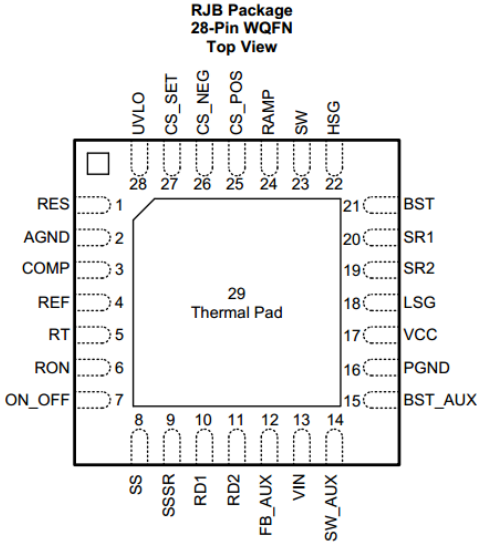
Open Design

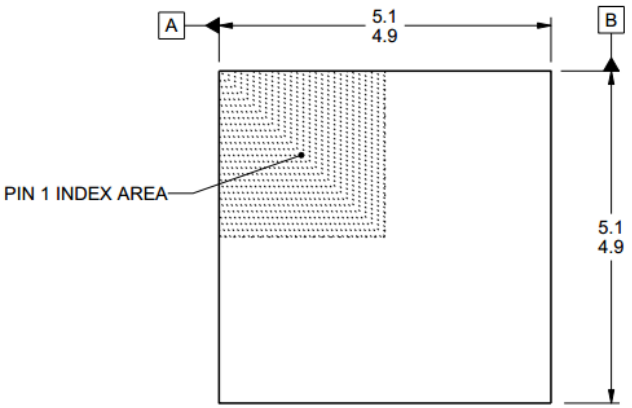
WEBENCH®
Interactive design
Preview design

LM5036 Mechanical, Packaging, Orderable

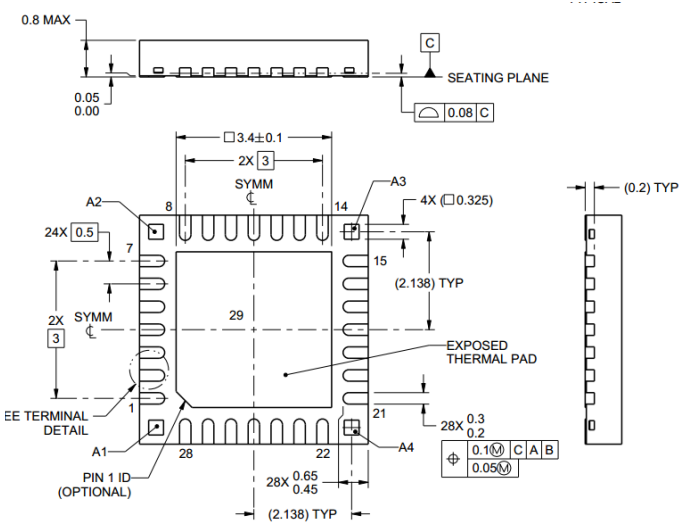
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)
LM5036RJBR	ACTIVE	WQFN	RJB	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM5036
LM5036RJBT	ACTIVE	WQFN	RJB	28	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LM5036





5x5x0.8 mm, 28-Pin QFN



TI Half-Bridge Controller Positioning

	Hard-switched Half-bridge/Full-Bridge				
Features/Standards	LM5036	LM5039	LM5035/B/C	UCC28250/ UCC28251	LM5045 (Full-Bridge)
Integrated 100V Auxiliary Bias Supply to power on IC/components at primary and secondary sides	YES	NO	NO	NO	NO
Fully Regulated Soft Start (FRSS) into Pre-biased Load (PBL)	YES	NO	NO	~~FRSS~~/PBL assumes on primary side	~~FRSS~~/PBL
Enhanced Cycle by Cycle Current Limiting with Pulse Matching	YES	CBC + Avg Current Limit	CBC/ ~~PulseMatch~~	YES	NA (Full Bridge)
High Voltage Startup	100V	105V	105V	NO	100V
Control Mode	Voltage	Voltage	Voltage	Voltage or Current	Voltage or Current
Integrated MOSFET Drivers	2A	2A	2A	NO	2A
5V Synchronous Rectifier Outputs	YES	NO	Only LM5035C	NO	YES
Programmable Hiccup Mode OCP	YES	YES	YES	YES	YES
Programmable Line UVLO and OVP	YES	UVLO/~~OVP~~	YES	~~UVLO~~/OVP	YES
Resistor Programmable Oscillator Frequency up to 2MHz	YES	YES	YES	NO, up to 1.4MHz Only	YES

LM5036 Training

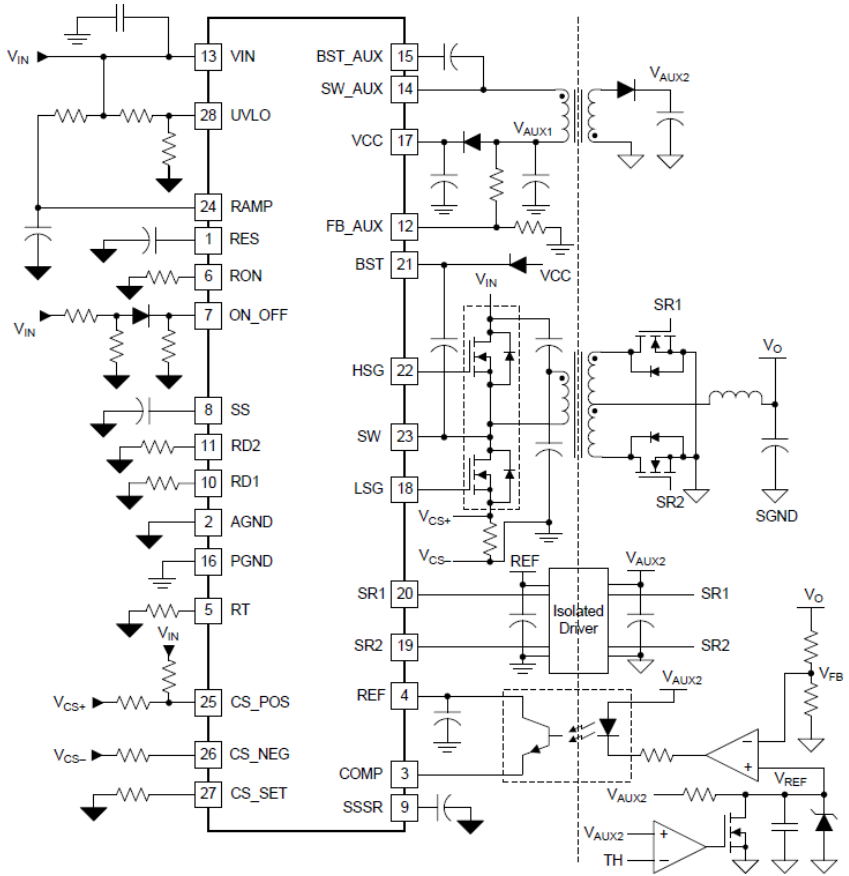
Topics

- Technical features and benefits
- LM5036 pin configuration
- Integrated auxiliary bias supply
- Fully regulated pre-bias start-up
- Cycle-by-cycle current limit and pulse matching
- Programmable hiccup mode OCP
- High voltage start-up, and undervoltage lockout (UVLO), and REF
- Applications with VIN > 100V
- Optimized maximum duty cycle
- OVP, fault latch
- Other features: full-bridge, Synchronized clock input, OTP, input voltage feedforward
- Layout guideline
- Half-bridge, active clamp forward comparison

LM5036 Technical Features Top Level Overview

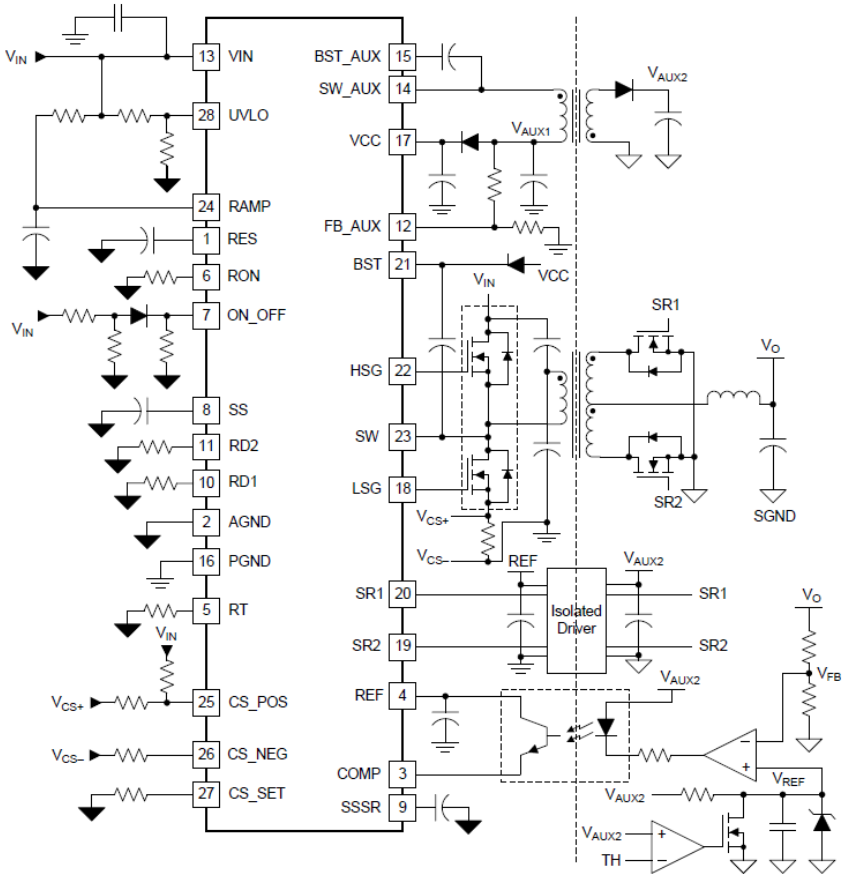
Feature	Why	Without	How
Integrated 100V Auxiliary Bias Supply	Reduces BOM, increases power density	Need separate bias supply with more components. Cannot easily adjust bias voltage to control soft-start process	Integrated aux power devices, drivers and current sense. Constant ON time with programmable frequency to allow use of small external transformer.
Fully regulated pre-bias start-up	Monotonic rise of output voltage ensures digital circuits start operating in correct sequence.	Energy in the output capacitor at start-up may be transferred to the input causing a dip in output voltage, or even damage to the power stage.	LM5036 start-up sequence ramps the secondary side reference and only activates the SR's when the reference level is above the output voltage.
Enhanced cycle-by-cycle current limit with pulse matching	Reduces output current limit variation. Increases power density.	Poor tolerance of output current limit. Designs thermally rated for highest over-load condition. More design margin needed, poor power density.	Stable CBC operation is ensured by matching t_{ON} times of primary MOSFETs. Peak current limit threshold adjusted with V_{IN} to minimise output current limit variation.
Integrated High Voltage Start-up	Reduces BOM, increases power density	External boot-strap required. Increase BOM and power loss.	Integrated HV regulator that is disabled once Aux bias supply is operating.
High maximum duty cycle	Improves efficiency	Higher current crest factor and power loss	Internal logic provides accurate maximum duty cycle
5V SR Outputs and programmable dead times	Improves efficiency	Longer SR body diode conduction increases power loss	Resistor on RD1 and RD2 provides accurate programming of dead-time between primary an SR switches.
Programmable Hiccup Mode OCP	Fault current can be matched to application. Reduces size.	Difficult to control temperature rise in over-load conditions. Need design margin to ensure safety.	Single external capacitor controls Hiccup Mode timing.
Programmable Line UVLO and OVP	Part can be configured to suit wide range of applications	More external parts required to meet range of requirements.	External resistor dividers set UVLO and OVP levels. Latched fault operation is also configurable.
Osc Freq programmable up to 2MHz	Enables transformer size reduction	Not able to take advantage of MOSFETs with reduced switching loss	High speed digital core.

LM5036 Pin Configuration



Pin #	Name	I/O	Description	Associated Features
13	VIN	I	Input voltage	High voltage startup
28	UVLO	I	Input undervoltage lockout	UVLO, Latch
24	RAMP	I	RAMP signal input to half-bridge PWM comparator	Voltage mode control
1	RES	I	Hiccup mode restart timer	Hiccup OCP
6	RON	I	Auxiliary supply on-time control	Integrated aux power
7	ON_OFF	I	Configure OVP or latch mode	OVP, Latch
8	SS	I	Soft-start input	Pre-bias start-up
11	RD2	I	SR leading-edge delay	SR deadtime control
10	RD1	I	SR trailing-edge delay	SR deadtime control
2	AGND	G	Analog ground	
16	PGND	G	Power ground	
5	RT/SYNC	I	Oscillator frequency control or external clock synchronization	Oscillator
25	CS_POS	I	Current sense amplifier positive input	CBC current limit
26	CS_NEG	I	Current sense amplifier negative input	CBC current limit
27	CS_SET	I	Current limit setting	CBC current limit

LM5036 Pin Configuration (cont.)



Pin #	Name	I/O	Description	Associated Features
15	BST_AUX	I	Auxiliary supply high-side gate drive bootstrap	Integrated aux power
14	SW_AUX	I	Auxiliary supply switch node	Integrated aux power
17	VCC	I	Bias supply	Integrated aux power
12	FB_AUX	I	Auxiliary supply output voltage feedback	Integrated aux power
21	BST	I	Half-bridge high-side gate drive bootstrap	
22	HSG	O	Half-bridge high-side MOSFET output driver	
23	SW	I	High-side switch node	
18	LSG	O	Half-bridge low-side MOSFET output driver	
20	SR1	O	SR PWM control output	
19	SR2	O	SR PWM control output	
4	REF	O	5-V reference regulator output	REF
3	COMP	I	Control current input to half-bridge PWM comparator	
9	SSSR	I	SR soft-start input	Pre-bias start-up
29	PAD	G	Thermal pad	

LM5036 Integrated 100V Auxiliary Bias Supply

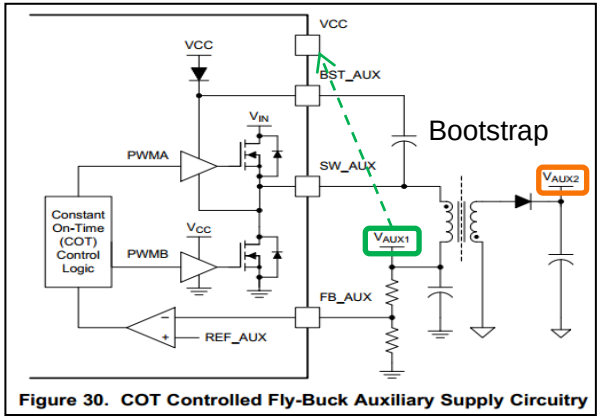
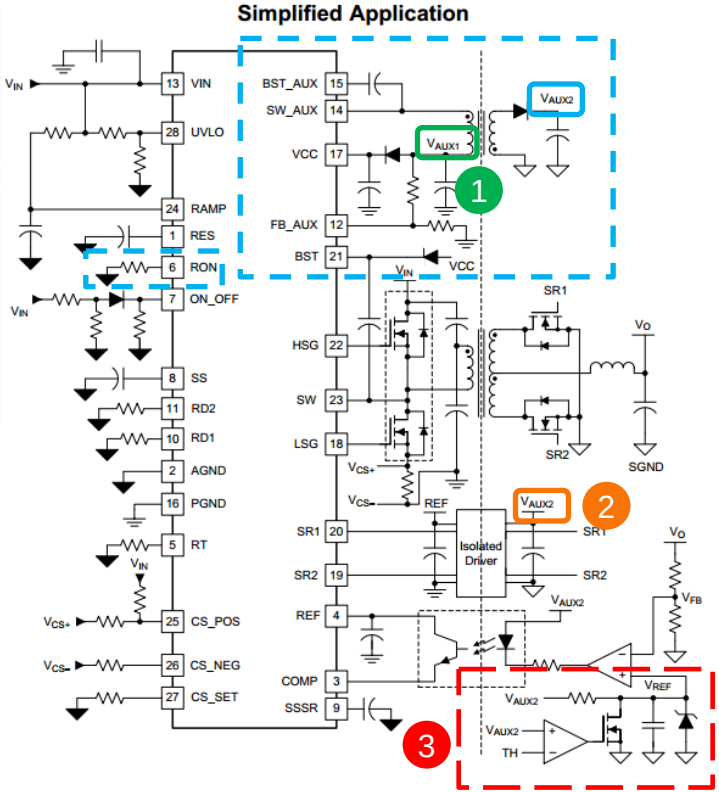
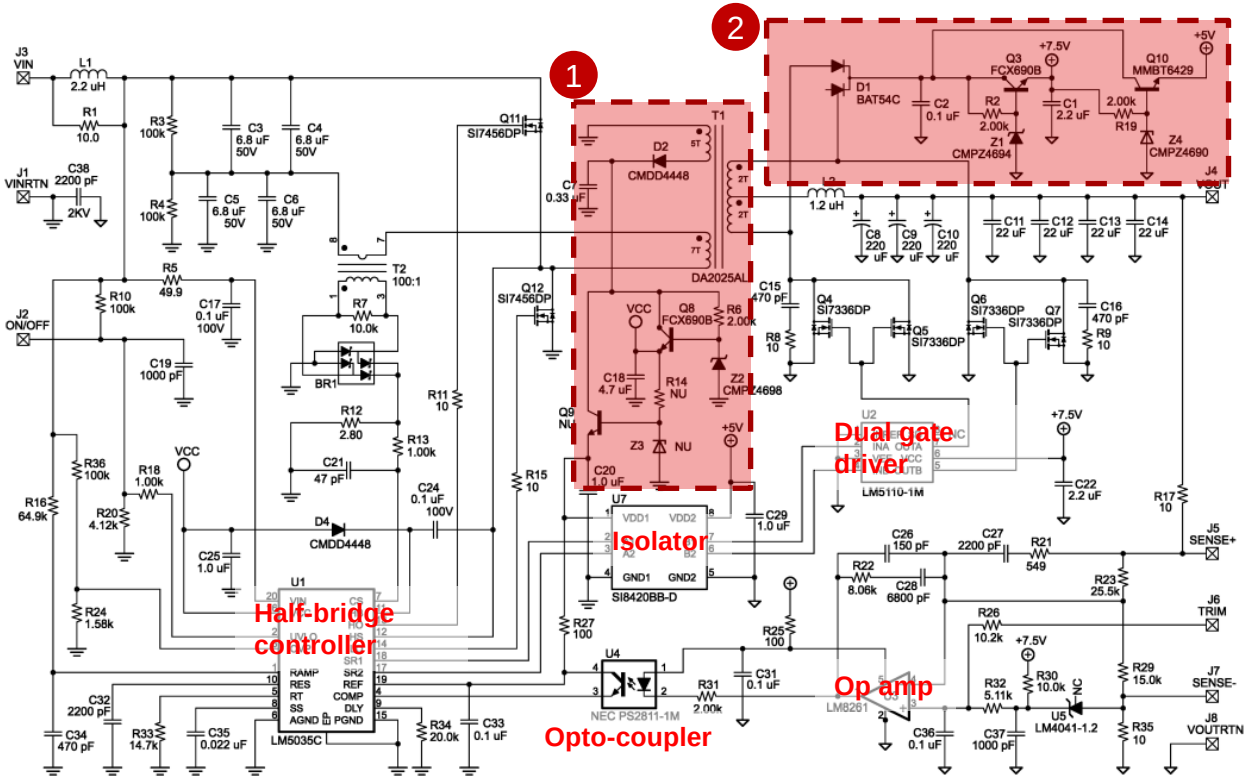


Figure 30. COT Controlled Fly-Buck Auxiliary Supply Circuitry



- Constant on-time (COT) fly-buck
- Integrated power switches, high + low side drivers and current sense
- ON time can be programmed by external resistor connected to RON (pin-6)
- Two resistors R_{FB1} and R_{FB2} set the value of V_{AUX1}. V_{AUX2}
- Small external transformer is all that is required to provide:
  1. LM5036 VCC at primary side
  2. Secondary aux power for isolated driver, opto-coupler, op amp, etc.
  3. Prebias ENABLE signal to release secondary side reference ramp for controlled soft-start to achieve regulated pre-bias.
- Use LM5036 Design Calculator to design the transformer and values of all other related components.

With and without Integrated Auxiliary Power

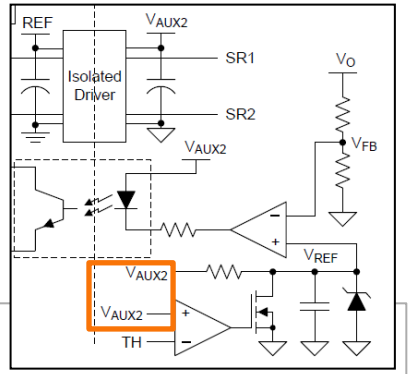


LM5035C EVM using external aux power (36-75VDC input, 3.3V/30A output)

Without integrated aux power feature, extra circuitries are needed:

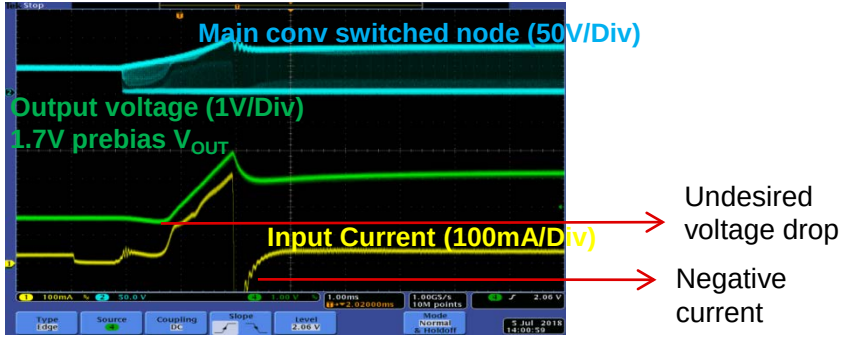
1. Transformer winding and circuity to generate VCC for controller.
2. Circuitry to power on isolator, SR driver, opto-coupler, op amp, etc.

Meanwhile, with LM5036, by using the modulation of the V_{AUX2}, the communication used for fully regulated pre-bias start-up between the primary and secondary side is established without the need of any additional opto-coupler.

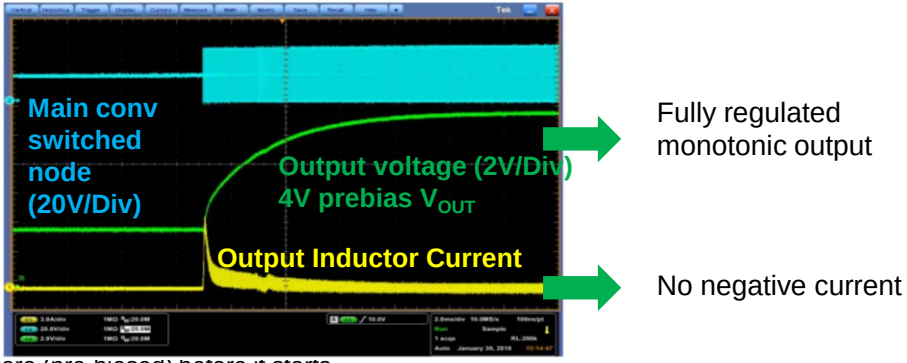


Pre-bias Start-up Issue and LM5036 Solution

Without full regulated pre-bias start-up design

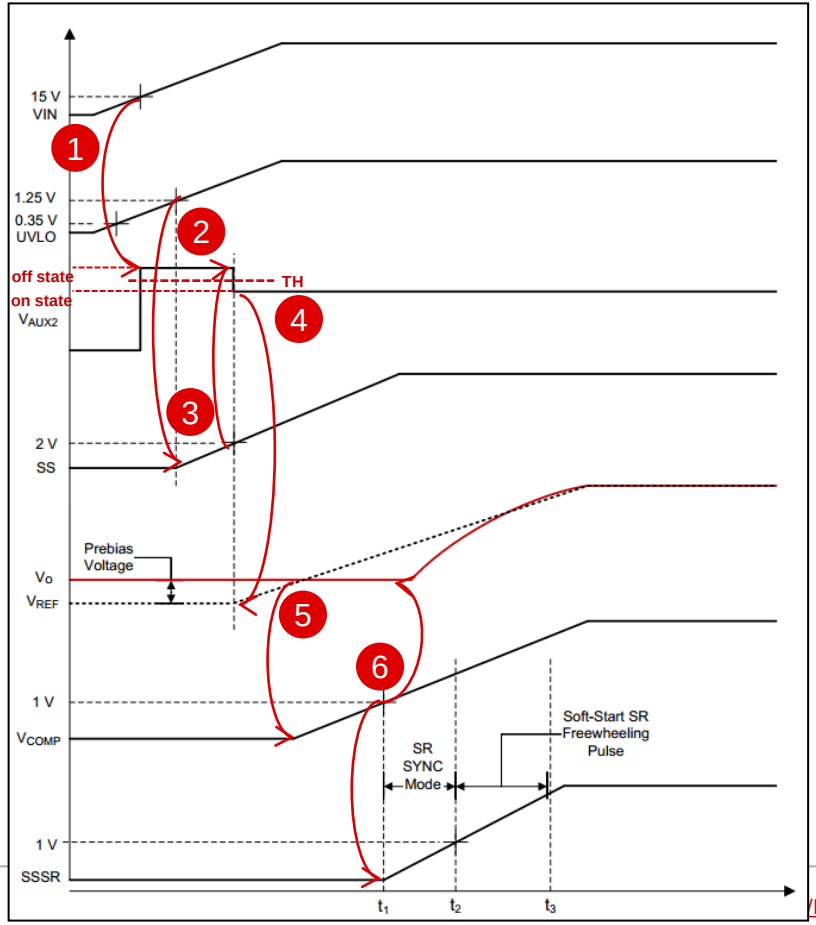


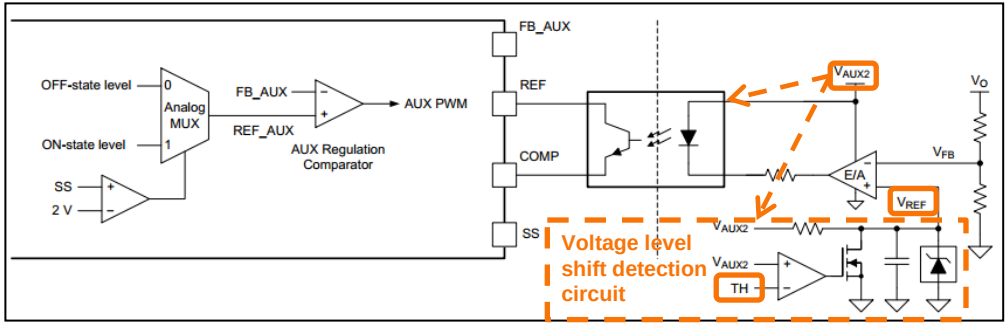
LM5036 based design



- **What is pre-biased start-up:** the DCDC converter output voltage is greater than zero (pre-biased) before it starts.
- **Why has pre-biased output:** it can happen in a few conditions, for example:
  - The output voltage is not fully discharged before DCDC re-start
  - Multiple DCDC converters connected together to provide higher power or redundancy. Some DCDC converters may start before other converters to pull up their output voltages.
- **Issue**: without fully regulated prebias start-up, when the output has voltage (pre-biased), the SR on the secondary side may engage prematurely to sink the current from pre-charged output capacitors back to the DCDC converter:
  - The reverse inrush current can cause undesired output voltage drop
  - May restart the load or even damage the converter
- **Solution**: LM5036 implements a new fully regulated prebias start-up scheme to ensure monotonic output voltage. It includes: 1) Primary FETs soft-start; 2) SR soft-start. Following two pages show the pre-bias start-up procedure for whom want to learn this in details.
- **Please note when design the DCDC converter with LM5036, it is not necessary for users to have consideration for this pre-bias start-up procedure as this is the function fully controlled by LM5036 itself.**

LM5036 Primary FETs Soft-start Process

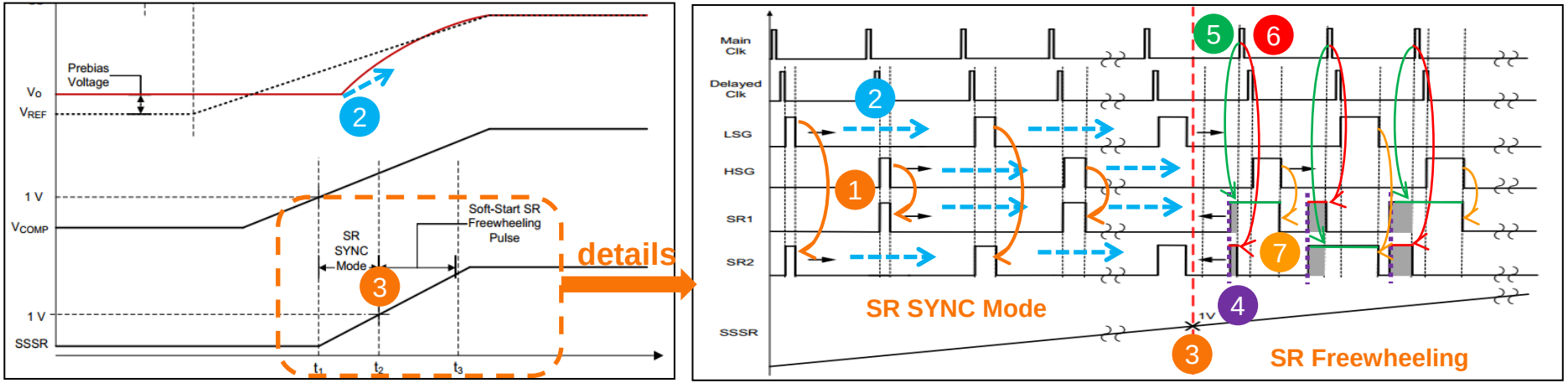




V_{AUX2} also serves as an ENABLE signal to initiate the soft-start sequence with using the voltage level shift detection circuitry.

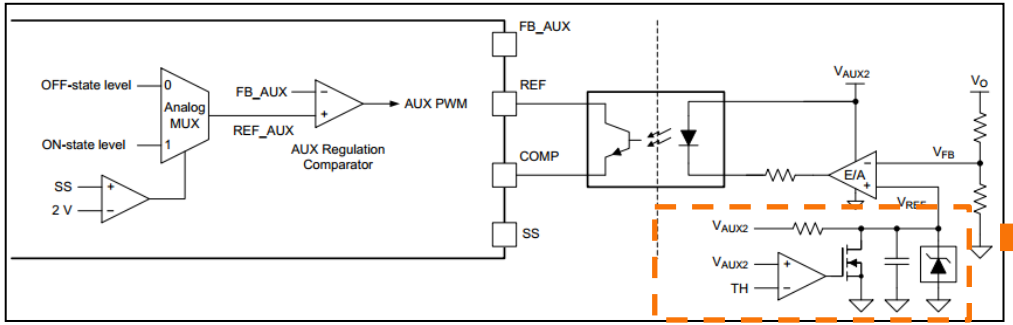
1. The V_{AUX2} starts as soon as VIN > 15V and VCC and REF are above their UV thresholds.
2. When UVLO exceeds 1.25V and VCC/REF are above their UV thresholds, soft-start capacitor starts to charge. When SS is < 2V, V_{AUX2} stays at “off state” (> TH) → Discharge V_{REF} (output voltage reference) → 0% duty-cycle.
3. When SS >= 2V, V_{aux2} will produce on state (< TH)
4. When V_{AUX2} is < TH, V_{REF} is released → Output voltage soft-starts. Duty-cycle is controlled by feedback loop but not SS capacitor voltage (because Vcomp < Vss).
5. When V_{REF} > Vo (prebias voltage), Vcomp starts to rise.
6. When Vcomp > 1V (corresponds to 0% duty-cycle), duty-cycle of primary FETs starts to increase (Vo to rise). In the meantime, SSSR capacitor starts to be charged.

LM5036 SR Soft-start Process



1. Before SSSR >= 1V, LM5036 operates at SR SYNC mode (SR sync to primary FETs) → 1) helps to reduce conduction loss of SR; 2) no risk of reverse current.
2. Primary FETs and SR pulse width gradually increases → 1) Vo rise, 2) the output voltage disturbance due to the difference in the voltage drop between the body diode and the SR Rdson is prevented.
3. When SSSR > 1V, LM5036 starts the soft-start of the SR freewheeling period.
4. SR1 and SR2 are turned on simultaneously during freewheeling period.
5. At the end of SR freewheeling period, at the rising edge of the Main Clk, the SR in phase with the next power transfer cycle remains on.
6. While at the rising edge of the Main Clk, the SR out of phase is turned off.
7. The in-phase SR remains on throughout the power transfer cycle. At the end of the power transfer cycle, both primary FETs and in-phase SR are turned off simultaneously. At the end of the soft-start, the SR pulses will become complementary to the respective primary FETs.

Example of Voltage Level Shift Detection Circuit



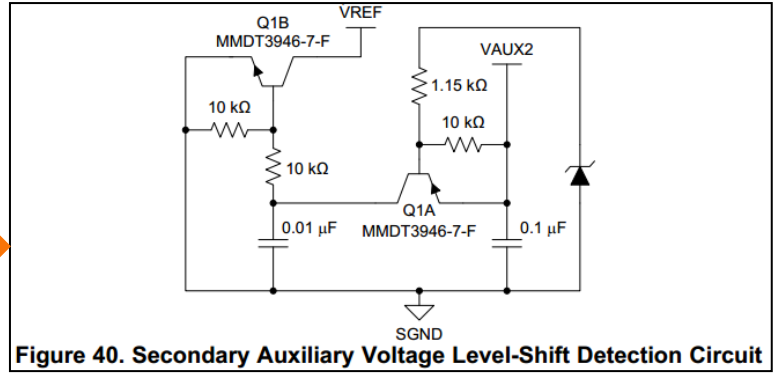
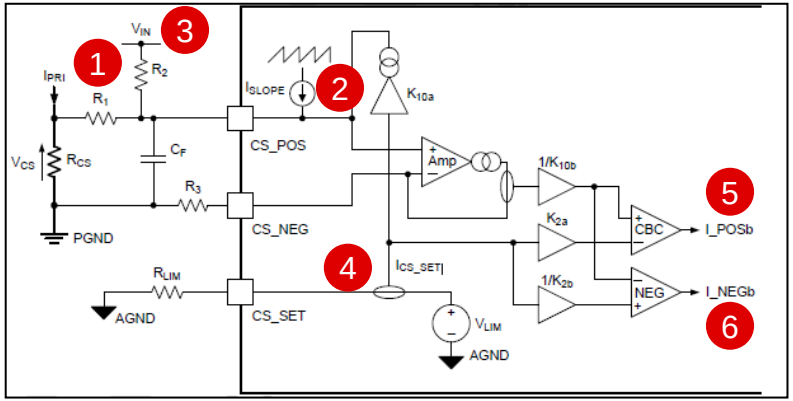
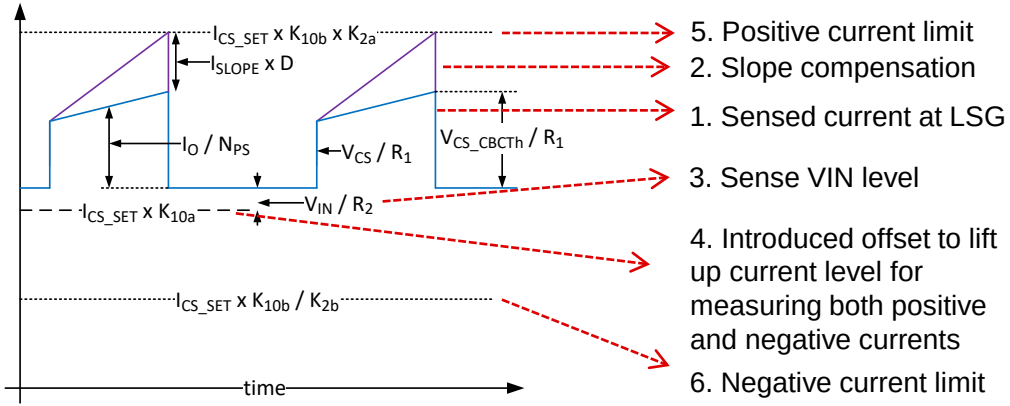


Figure 40. Secondary Auxiliary Voltage Level-Shift Detection Circuit

- The zener voltage needs to between off-stage and on-stage of V_{AUX2}.
- When V_{AUX2} > zener voltage, both Q1A and Q1B are on, V_{REF} is clamped to ground.
- When V_{AUX2} < zener voltage, both Q1A and Q1B are off, V_{REF} is released.
- LM5036EVM-294 is using this example circuity.

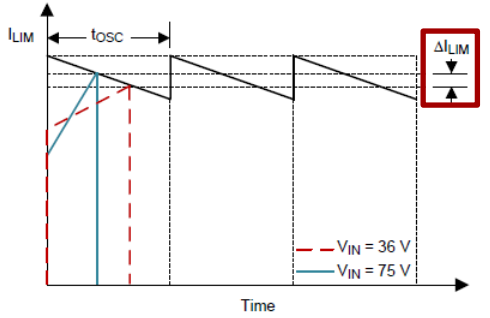
LM5036 Cycle-by-cycle Current Limit





- Both **positive current** and **negative current** (cause output voltage dip or even damaged) are sensed and limited.
- Constant current limit issue and solution:
  - **Issue**: during cycle-by-cycle operation, the controller behaves as peak current mode control which needs slope compensation to prevent sub-harmonic oscillation → current limit varies with input voltage range (see the right picture). This will cause inconstant output power limit (output power limit changes with VIN).
  - **Solution**: LM5036 fixes this issue by adding the VIN voltage as a variable of the function to **ensure reduced variation of output current limit vs input voltage.**
- All these functions are set by three CS pins and related external resistors. Use LM5036 design calculator to find the values of these resistors.

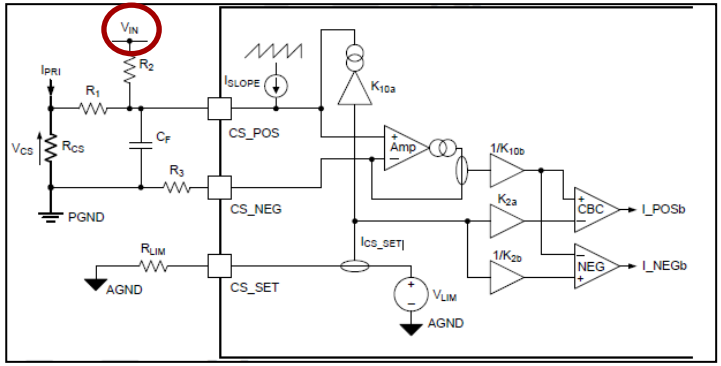
Example of without constant current limit

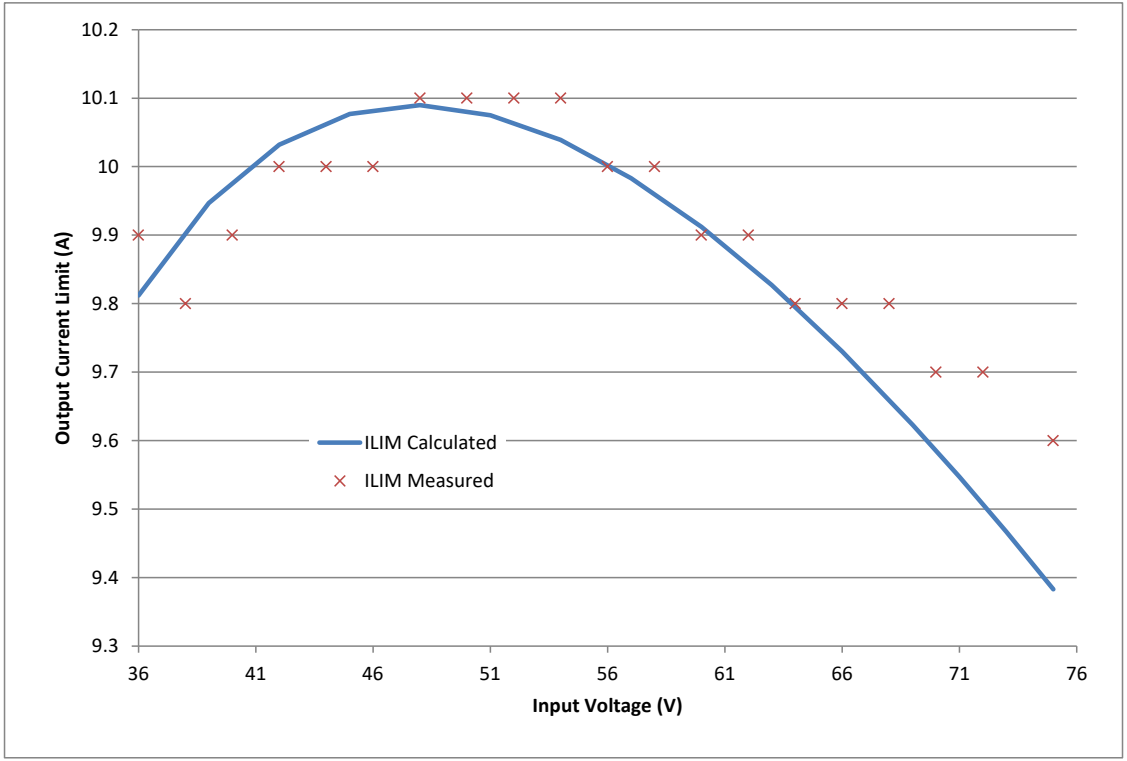


Nearly constant output current limit

CBC components are selected so that output current limit at maximum and minimum input voltage are same.

Output current limit is then nearly constant across Line
→ **enable almost constant output power limit across wide VIN range**





Use LM5036 Design Calculator to calculate the values of the components used in CBC Current Limit

Ilimit		10	A	Output current limit (greater than max load current)

CBC Resistor				
Islope_pk		50	µA	R3 is determined based on the slope compensation requirement
Inductor current slope	m2	9.57	mV/µs	
	Ratio	54.35		The ratio of the slope of the compensation ramp to the inductor current down-slope
Resistor R3	R3	478.72	Ω	R3 is determined based on the slope compensation requirement
Resistor R2	R2	3375.48	kΩ	
Resistor RLim	RLIM	54.35	kΩ	
Internal Current limit	ICS_SET	1.38E-05	A	Calculated Internal current set
Resistor R1	R1	478.79	Ω	

- LM5036 has intelligent control scheme to have constant current limit across wide VIN range in CBC.
- As explained in datasheet, complicated control scheme and equations are used to calculate the resisitor values used in CBC.
- In actual design, users can just simply use the LM5036 Design Calculator to calculate the resistor values (see above screenshot) without remembering this control scheme and calculation steps.
- All the equations used in CBC are embedded in this design calculator.

Pulse Matching

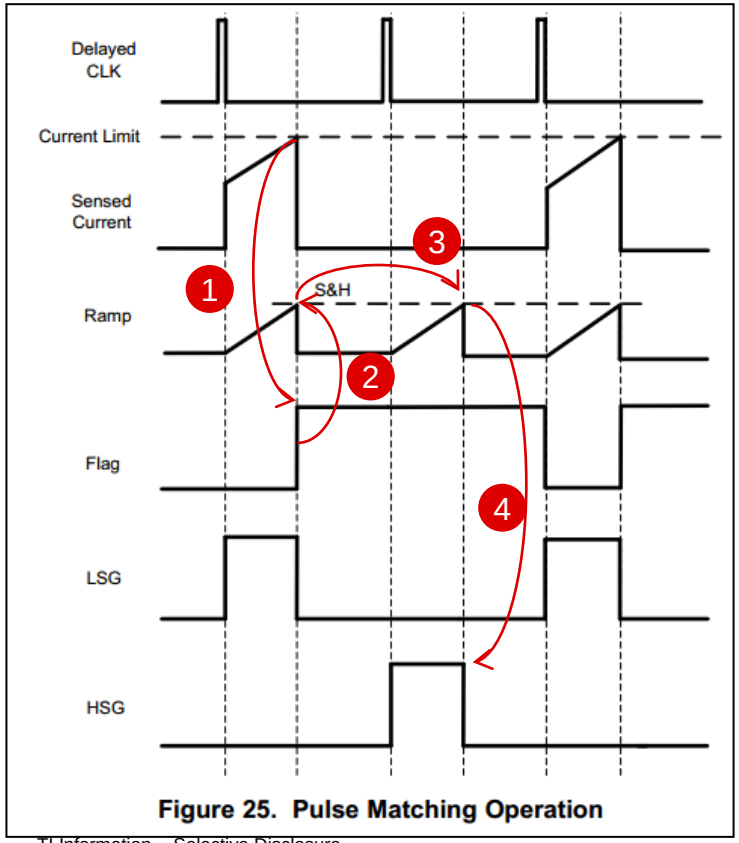


Figure 25. Pulse Matching Operation

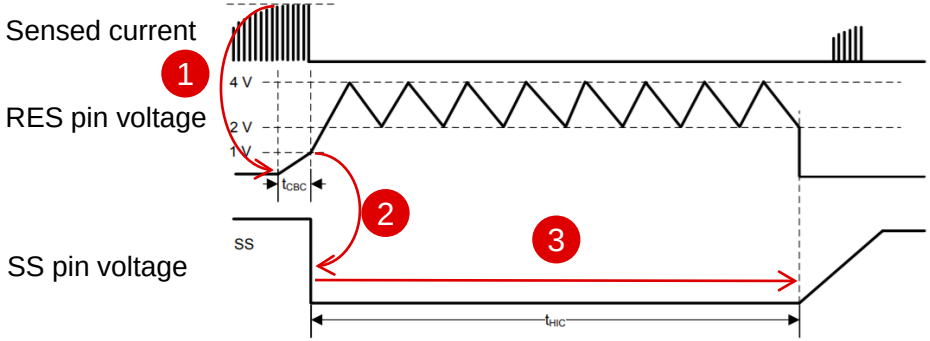
- LM5036 maintains the flux balance of the main transformer during CBC operation.
- **The duty cycles of the two primary FETs are always matched** to ensure the voltage-second balance which prevents transformer saturation.

Procedure:

1. When the current limit is reached during the low-side phase, a FLAG signal goes high.
2. The RAMP signal is samples during the rising edge of the FLAG.
3. The RAMP is held through the next half switching period for the high-side phase.
4. When the high-side phase ramp rises to the sampled RAMP value, the high-side PWM pulse is turned off so that the duty cycles are matched for both phases.

LM5036 Programmable Hiccup Mode OCP

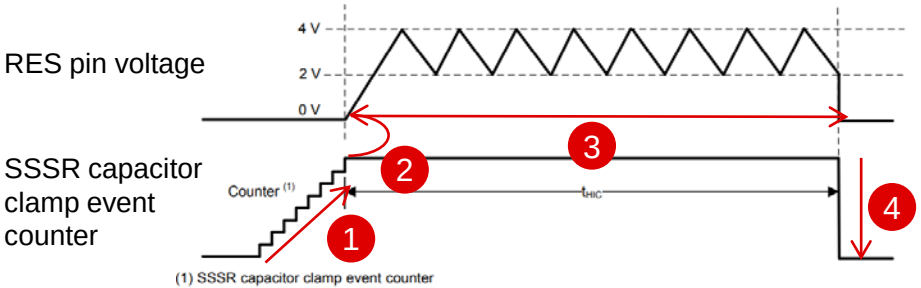
Condition A: repetitive CBC current limit



- CBC OCP will start when reaches current limit

1. When reach current limit, the capacitor connected at RES pin is charged by a 15μA current source.
2. Hiccup mode started when V_{RES} reaches 1V. SS and SSSR are discharged. The time for V_{RES} to reach 1V (t_{CBC}) is determined by the capacitor connected to RES pin.
3. Once V_{RES} > 1V, a 30 μA current source to charge RES capacitor to 4V, then a 5 μA current source to discharge it to 2V for 8 times (t_{HIC}).

Condition B (new in LM5036): repetitive negative current event

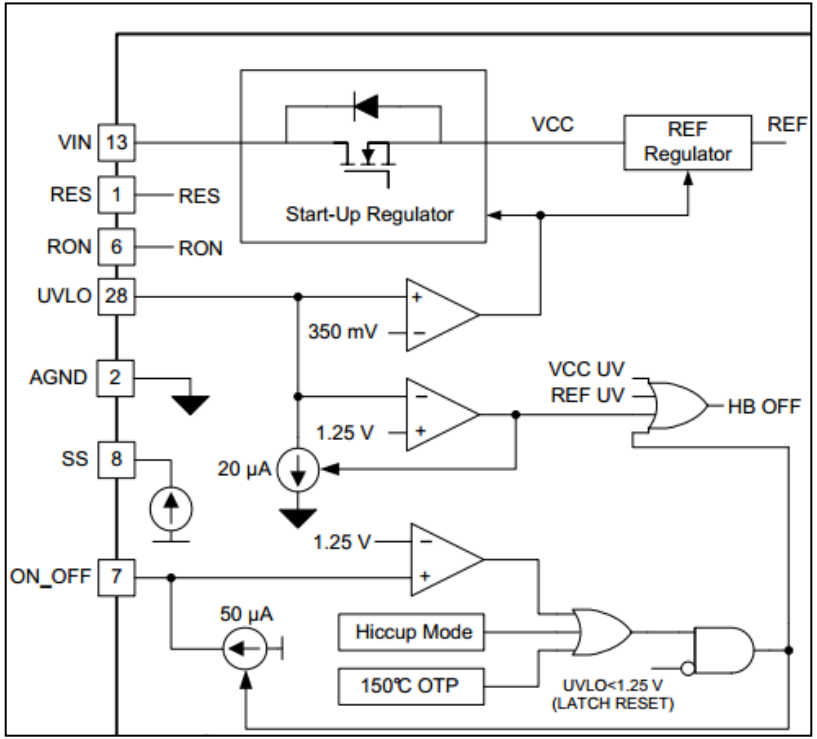


- SSSR capacitor will be clamped to ground when reverse current limit is exceeded twice → enter SR SYNC mode.

1. Enter hiccup mode if SSSR capacitor is clamped for 8 times.
2. RES capacitor is charged by a 30μA current source in the beginning of the hiccup mode.
3. The hiccup mode lasts t_{HIC}.
4. After t_{HIC}, SSSR capacitor clamp event counter will be reset.

Use LM5036 Design Calculator to set t_{CBC} to calculate RES pin capacitor value and t_{HIC}.

LM5036 High Voltage Start-up, and Undervoltage Lockout, and REF



- Integrated start-up regulator provides VCC power for start-up and fault conditions when the integrated auxiliary power supply is not operating
- Suitable for operation from V_{IN} 16V to 100 V with internally current limited $I_{CC(Lim)}$ = 81 mA.
- 5V REF output with 39mA current limit that can power on opto-coupler, primary side isolator/gate driver, and other housekeeping circuits.

Table 1. Device Functional Modes

CRITERIA	VCC AND REF REGULATORS	AUXILIARY SUPPLY	HALF-BRIDGE CONVERTER
UVLO < 0.35 V	OFF	OFF	OFF
(0.35 V < UVLO < 1.25 V) & (VIN < 15 V)	ON	OFF	OFF
(VCC & REF > UV) & (VIN > 15 V) & (UVLO < 1.25 V)	ON	ON at ASYNC Mode	OFF
(VCC & REF > UV) & (VIN > 15 V) & (UVLO > 1.25 V) & No Faults	ON	ON at SYNC Mode	ON
(VCC & REF > UV) & (VIN > 15 V) & (UVLO > 1.25 V) & Any Faults	ON	ON at ASYNC Mode	OFF
(VCC & REF > UV) & (VIN > 15 V) & AUX Current Limit	ON	ON at ASYNC Mode	NA

Applications with VIN > 100V

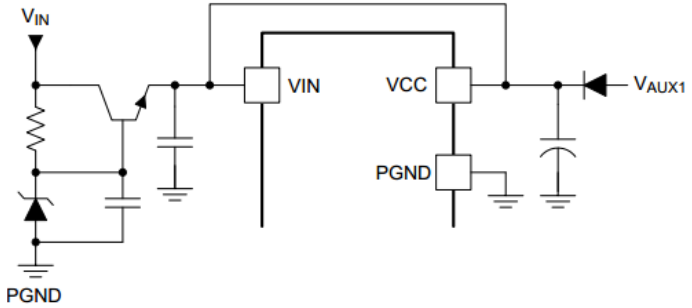


Figure 41. External Start-Up Regulator

LM5036 can be used for isolated DC/DC applications with input voltage > 100V. In this case:

- VCC start-up regulator, auxiliary supply, half-bridge gate drivers need to be bypassed, or powered from a reduced voltage.
- VIN pin can be powered from an external start-up regulator, as shown above.
- If pre-biased start-up is required the integrated flybuck aux circuit should be used from the reduced VIN pin voltage to supply the secondary control circuit.
- If pre-biased start-up is not required, the bias supply VAUX1, can be derived from an external auxiliary supply. An external gate driver with higher voltage rating should be used to drive the half bridge.

PWM and 5V SR Timing and Deadtime control

1. A delayed clock is derived by adding a delay t_D to the main clock. t_D is determined by the resistor value connected between RD1 and AGND pins.
2. Rising edge of the Main CLK is to turn off SRs.
3. LSG and HGS turn on at the falling edge of the delayed clock.

- Programmable delay (**t_1**) from falling edge of outgoing SR gate to rising edge of incoming MOSFET gate. Resistor value connected between pin **RD1** and GND programs this delay.
- Programmable delay (**t_2**) from falling edge of outgoing MOSFET gate to rising edge of incoming SR gate. Resistor value connected between pin **RD2** and GND programs this delay.
- Delays can be adjusted to suit propagation delays and switching speeds
- Enables maximum efficiency by minimizing body diode conduction → Minimize t_1 and t_2.
- 5V Synchronous rectifier outputs can directly drive cost effective isolated driver solutions.
- Use LM5036 Design Calculator to calculate RD1 and RD2 values based on desired t_1 and t_2.

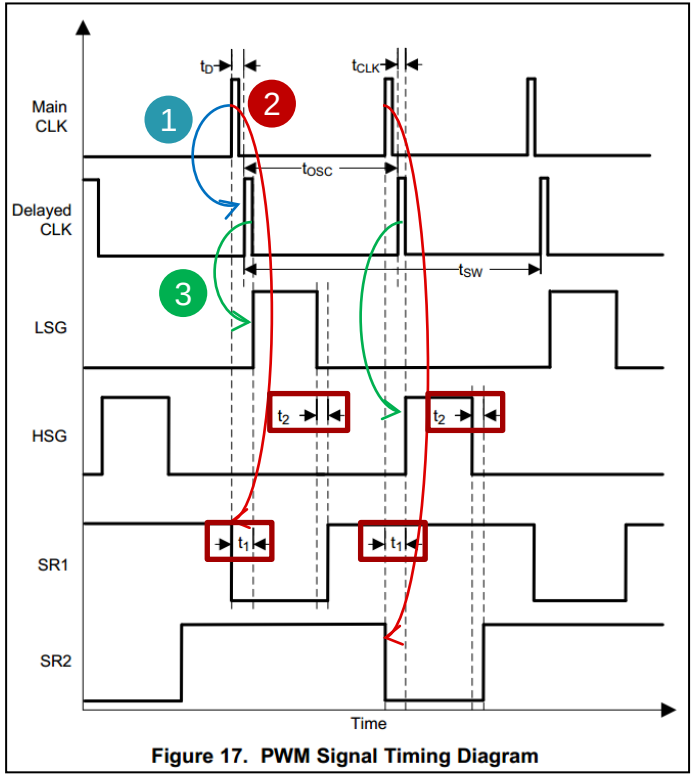


Figure 17. PWM Signal Timing Diagram

LM5036 Optimized Maximum Duty Cycle

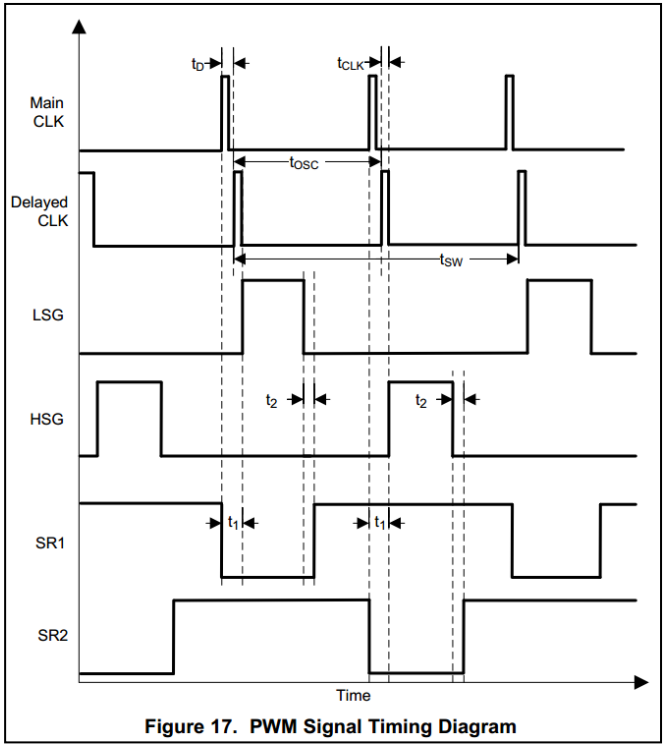


Figure 17. PWM Signal Timing Diagram

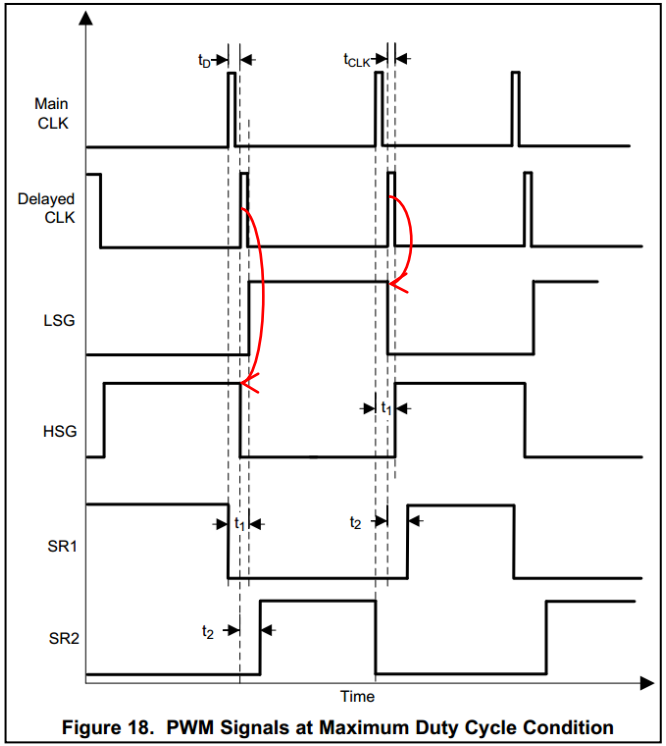


Figure 18. PWM Signals at Maximum Duty Cycle Condition

- Maximum duty cycle is achieved when the MOSFET's are turned off by the rising edge of the delayed clock, instead of the PWM comparator.
- **LM5036 maximum duty cycle is well controlled since it depends only upon the width of the internal delayed clock signal (t_{CLK} = 60ns) but not others (e.g., SR delay)**

$$D_{MAX} = \frac{\frac{1}{f_{OSC}} - t_{CLK}}{\frac{2}{f_{OSC}}}$$

- Maximum effective duty cycle close to unity.
- **Designs can operate with higher duty cycle for maximum efficiency without the risk of hitting duty cycle clamp.**

LM5036 OVP, Fault Latch

- ON_OFF pin can be configured as Latch or OVP pin to have LM5036 working in different protection configurations.

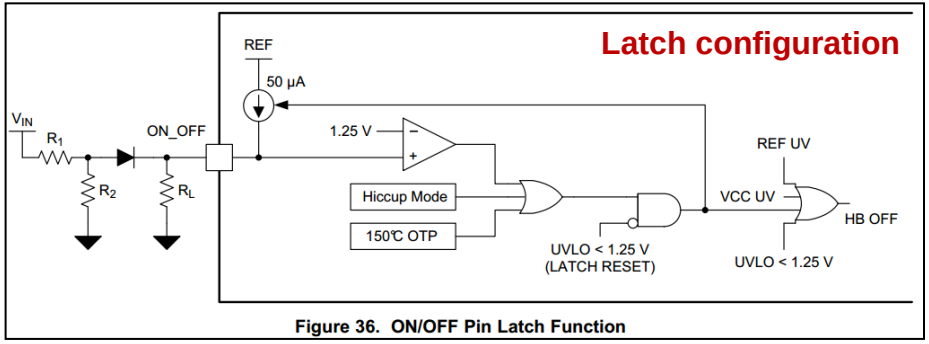


Figure 36. ON/OFF Pin Latch Function

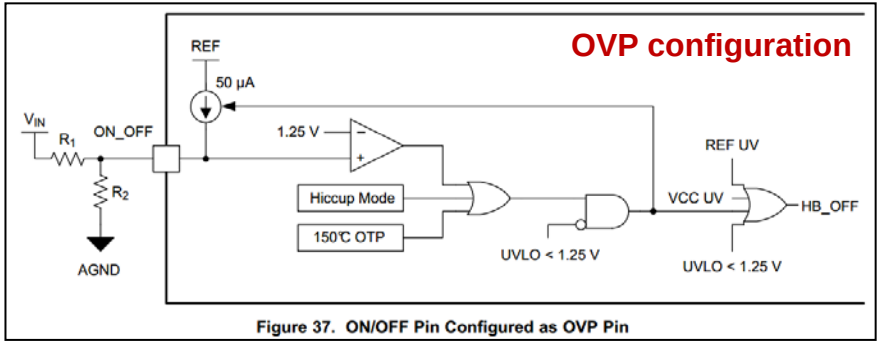


Figure 37. ON/OFF Pin Configured as OVP Pin

- In latch configuration, half-bridge converter remains off even faults (hiccup, OTP, OVP) are clear.
- When faults happen, a 50µA current source will raise ON_OFF pin voltage. The diode is reverse biased. ON_OFF voltage is above > 1.25V.
- Need to reset latch to initiate a new soft-start.
- Pull down UVLO to < 1.25V to reset latch.
- Soft-start will initiate when latch resets and faults are clear.

- In OVP configuration, the input voltage level, at which an OVP fault is triggered, can be programmed by an external resistor divider.
- The resistor divider should be designed such that ON_OFF pin voltage is > 1.25V when over-voltage condition occurs.
- Once a fault (include two level OTP, hiccup) is triggered, 50µA is sourced from this pin to provide OVP hysteresis.

Use LM5036 Design Calculator to calculate resistor values needed for desired hysteresis level and OVP rising threshold.

LM5036 Programmable Line UVLO

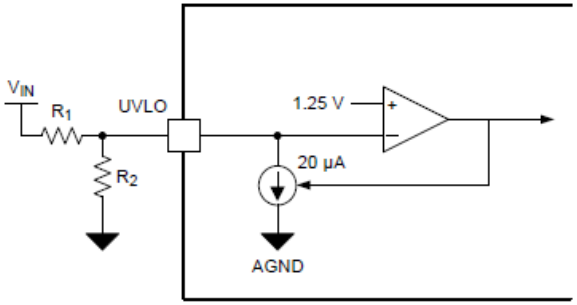


Figure 42. UVLO Configuration

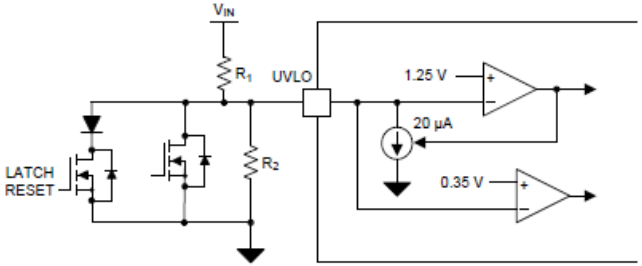


Figure 43. Latch Reset

UVLO Pin:

- The minimum input voltage level at which the main output is enabled can be programmed by an external resistor divider
- Fault latch (if configured) is reset by pulling this pin below 1.25V. Either by dropping V_{IN} or using an external switch to pull the pin down briefly
- Pulling this pin low will disable the part

Use LM5036 Design Calculator to calculate resistor values needed for UVLO.

Other Features

- LM5036 used in full bridge
  - May use external gate driver to support an additional pair of FETs
  - DC-blocking capacitor is needed to ensure voltage-second balance to prevent main transformer saturation.
- Synchronized clock input
  - RT (pin-5) is set oscillator frequency through an external resistor
  - When need LM5036 to be sync'ed with external clock, the clock signal need to be coupled into RT pin through a capacitor. Still need the external resistor and set lower/equal frequency than the external clock.
- Over Temperature Protection (OTP)
  - When junction temperature > 150°C, PWM and SR outputs are turned off.
  - When junction temperature > 160°C, integrated aux power is disabled. REF is still working to provide bias power for external house-keeping circuitry.
- Voltage mode control with input voltage feedforward
  - Improve line transient response
  - Less susceptible to noise

Layout Guideline

- The two ground planes (AGND and PGND) of LM5036 device should be tied together with a short and direct connection to avoid jitter due to relative ground bounce. The connection point could be at the negative terminal of the input power supply.
- The VIN, VCC, REF pin capacitors, and CS_NEG resistor should be tied to PGND plane. UVLO, ON_OFF, RT, RON, RD1 and RD2 resistors, RAMP, RES, SS and SSSR capacitors, and the thermal pad should all be tied to AGND plane.
- SW and SW_AUX are switching nodes which switch rapidly between VIN and GND every cycle which are sources of high dv/dt noise. Therefore, large SW/SW_AUX node area should be avoided.
- The differential current sense signals at CS_POS and CS_NEG pins should be routed in parallel and close to each other to minimize the common-mode noise.
- The area of the loop formed by the main feedback control signal traces (COMP and REF) should be minimized in order to reduce the noise pick up. This can be accomplished by placing the COMP and REF signal traces on top of each other in adjacent PCB layers. In addition, the main feedback control signal traces should be routed away from the SW_AUX switching node to avoid high dv/dt noise coupling.
- The gate drive outputs (LSG and HSG) should have short and direct paths to the power MOSFETs to minimize parasitic inductance in the gate driving loop.
- The VCC and REF decoupling capacitors should be placed close to their respective pins with short trace inductance. Low ESR and ESL ceramic capacitors are recommended for the boot-strap, VCC and the REF capacitors.
- A decoupling capacitor should be placed close to the IC, directly across VIN and PGND pins. The connections to these two pins should be direct to minimize the loop area which carries switching currents.
- The boot-strap capacitors required for the high-side gate drivers of the half-bridge converter and auxiliary supply should be located close to the IC and connected directly to the BST/BST_AUX and SW/SW_AUX pins.
- The area of the switching loop of the power stage consisting of input capacitor, capacitive divider, transformer, and the primary MOSFETs should be minimized.

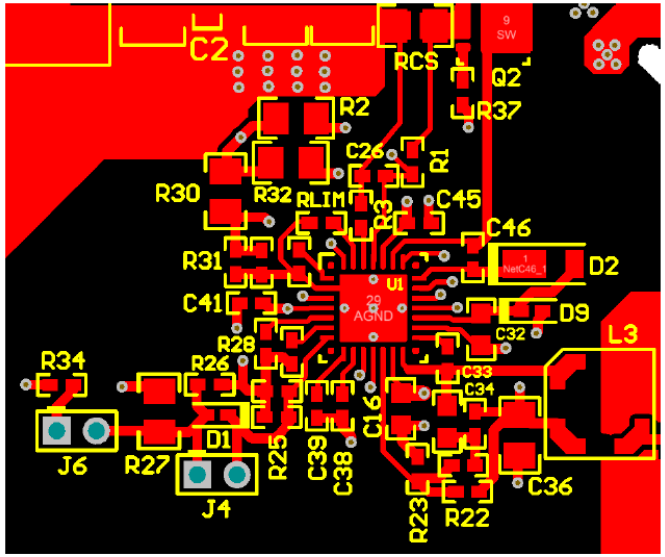


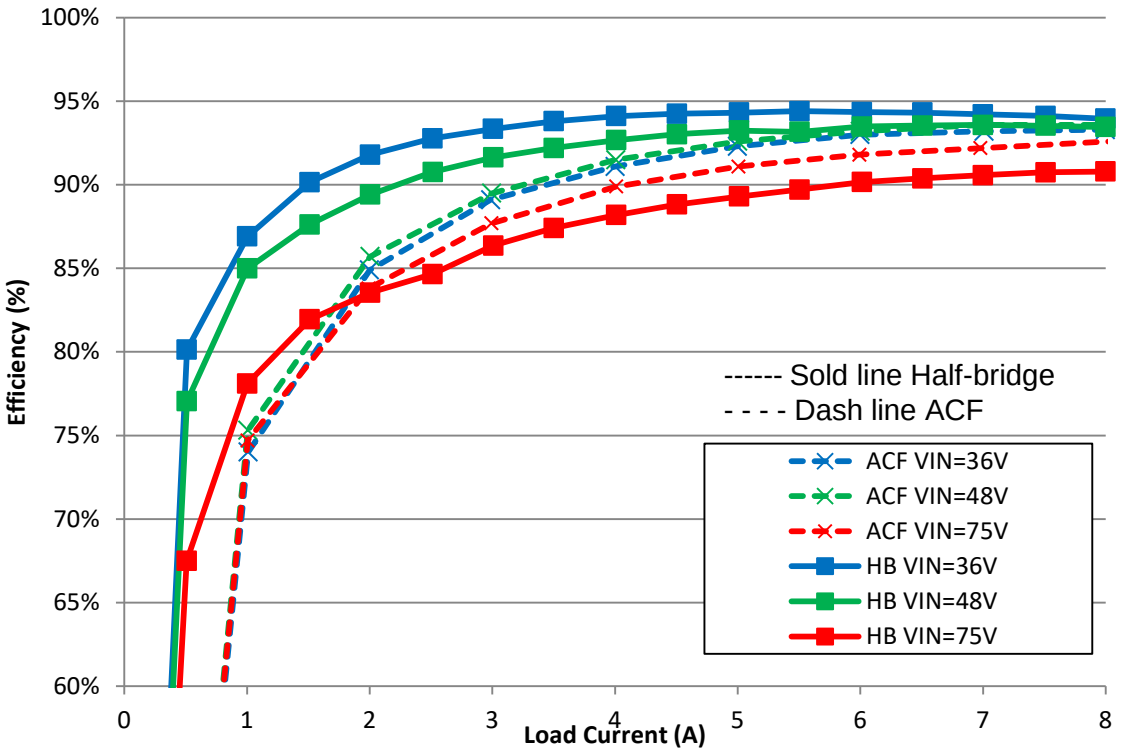
Figure 50. LM5036 PCB Layout Example

HALF BRIDGE &
ACTIVE CLAMP FORWARD

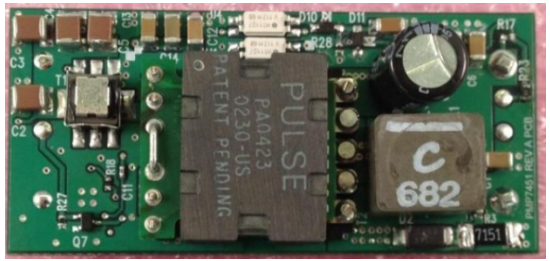
Active Clamp Forward or Half-Bridge

	Active Clamp Forward	Half-Bridge
BOM	+ larger output inductor + clamp capacitor	+ HS drive (LM5036 included) + Splitter capacitors + SR control needed (LM5036 included)
Efficiency	+ Partial ZVS operation gives efficiency advantage at VIN(max)	+ Higher max duty gives efficiency advantage at VIN(min)
Power Density	Good	Better (if not thermally limited at VIN(max))
SR	Direct SR drive is possible	Direct SR drive is not possible. (LM5036 includes SR output)
Regulated Pre-biased	Possible	Possible (LM5036 included)
Protection	Good (Peak CM control)	Pulse matching needed during Peak CM control (LM5036 included)
Transient Response	Good (due to clamp cap charging)	Better

Active Clamp Forward vs Half-Bridge



LM5036 EVM fsw = 400kHz
36V-75V / 12V 100W design



UCC2897A ACF PMP7451 fsw=300kHz
36V-75V / 12V 120W design

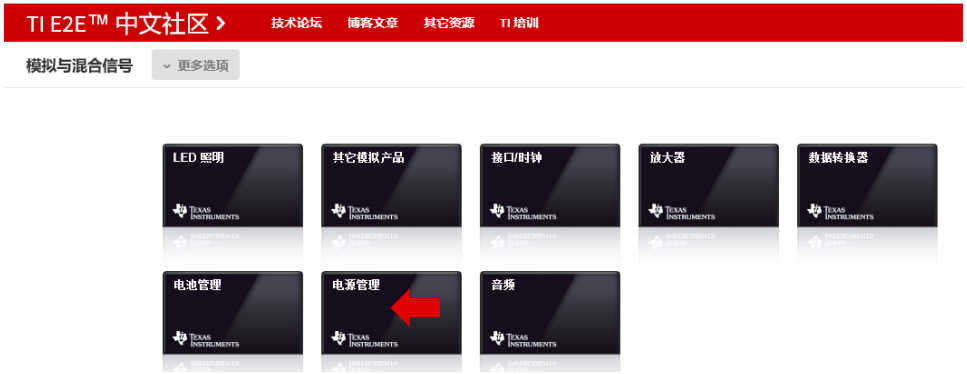
TI Half-Bridge and Active Clamp Controller Positioning

	Hard-switched Half-bridge/Full-Bridge					Active Clamp Forward			
Features/Standards	LM5036	LM5039	LM5035/B/C	UCC28250 UCC28251	LM5045 (Full-Bridge)	UCC2897A	LM5025	LM5026	LM5034 (Interleaved)
Typical supporting power range	Half-bridge: 100W – 500W Full-bridge: 500W+					30W – 200W			200W+
Integrated 100V Auxiliary Bias Supply to power on IC/components at primary and secondary sides	YES	NO							
Fully Regulated Soft Start (FRSS) into Pre-biased Load (PBL)	YES	NO	NO	~~FRSS~~/PBL assumes on primary side	~~FRSS~~/PBL	NO	NO	NO	NO
Enhanced Cycle by Cycle Current Limiting with Pulse Matching	YES	CBC + Avg Current Limit	CBC/ ~~PulseMatch~~	YES	NA (Full Bridge)	NA	NA	NA	NA
High Voltage Startup	100V	105V	105V	NO	100V	110V	90V	100V	100V
Control Mode	Voltage	Voltage	Voltage	Voltage or Current	Voltage or Current	Current	Voltage	Current	Current
Integrated MOSFET Drivers	2A	2A	2A	NO	2A	2A	3A	2A	3A
5V Synchronous Rectifier Outputs	YES	NO	Only LM5035C	NO	YES	NA	NA	NA	NA
Programmable Hiccup Mode OCP	YES	YES	YES	YES	YES	CM	CM	CM	CM
Programmable Line UVLO and OVP	YES	UVLO/~~OVP~~	YES	~~UVLO~~/OVP	YES	YES	UVLO/~~OVP~~	UVLO/~~OVP~~	UVLO/~~OVP~~
Resistor Programmable Oscillator Frequency up to 2MHz	YES	YES	YES	NO, up to 1.4MHz Only	YES	NO (1MHz)	NO (1MHz)	NO (1MHz)	YES

MORE INFORMATION

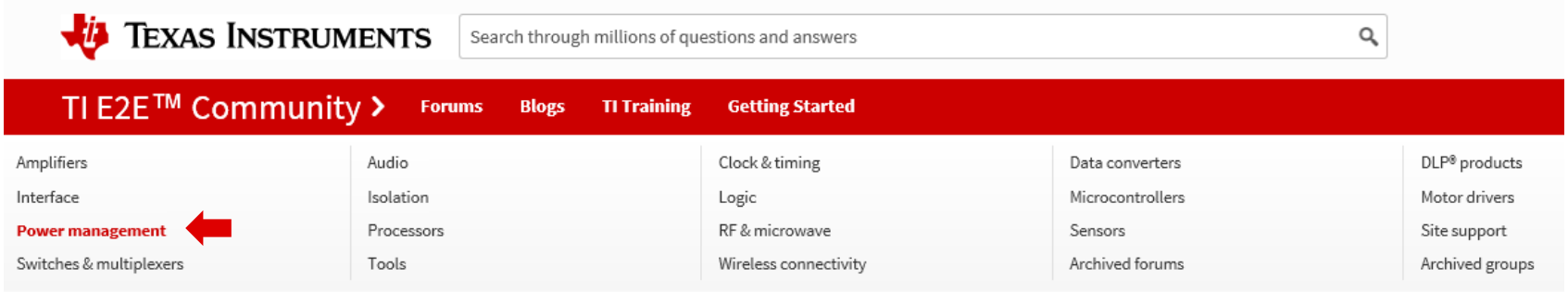
TI China E2E 中文社区

- LM5036 技术博客
  - 基于LM5036“智能”型半桥DC/DC电源设计方案
  - 基于LM5036 的半桥DC/DC电源——辅助电源篇
  - 基于LM5036的半桥DC/DC电源——预偏置启动篇
  - 基于LM5036的半桥DC/DC电源——电流保护篇
- 电源管理技术论坛
  http://e2echina.ti.com/question_answer/analog/power_management/

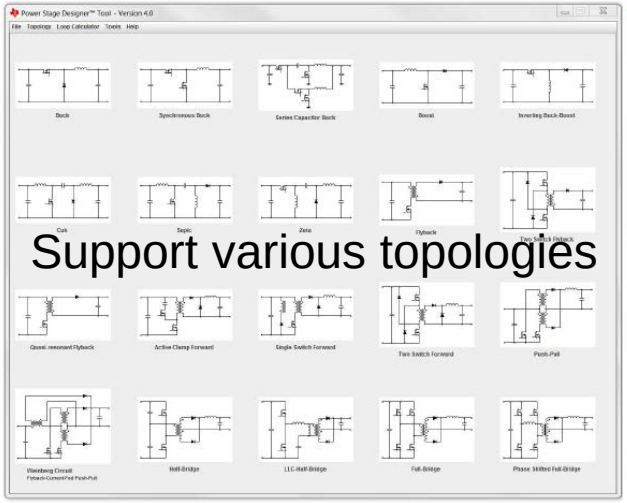


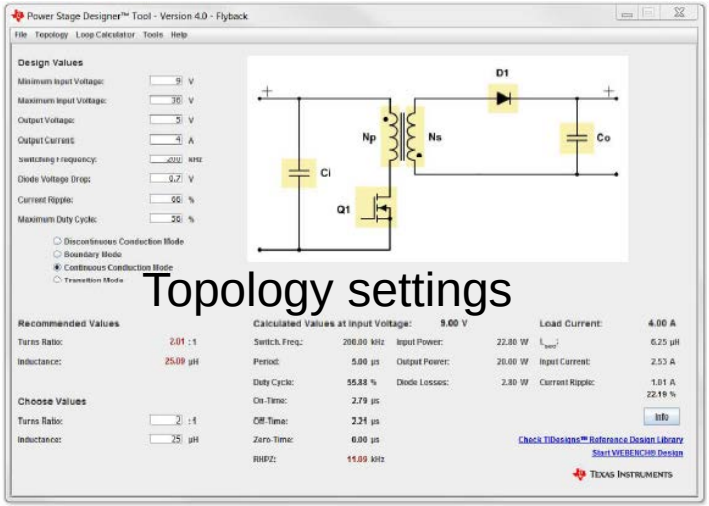
Support

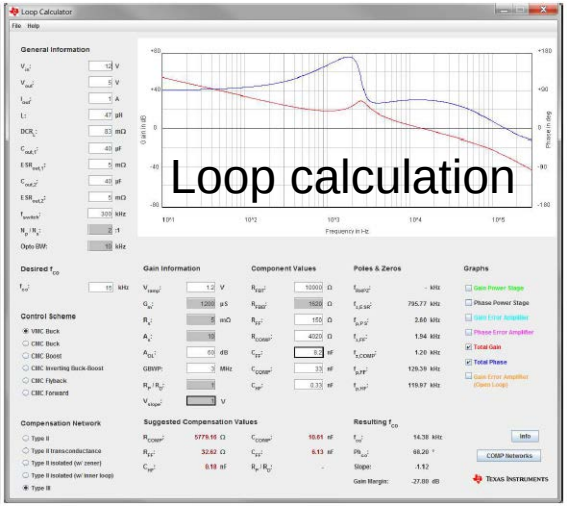
- 24 hour reply at TI E2E Forum: **Power management forum**



Power Stage Designer

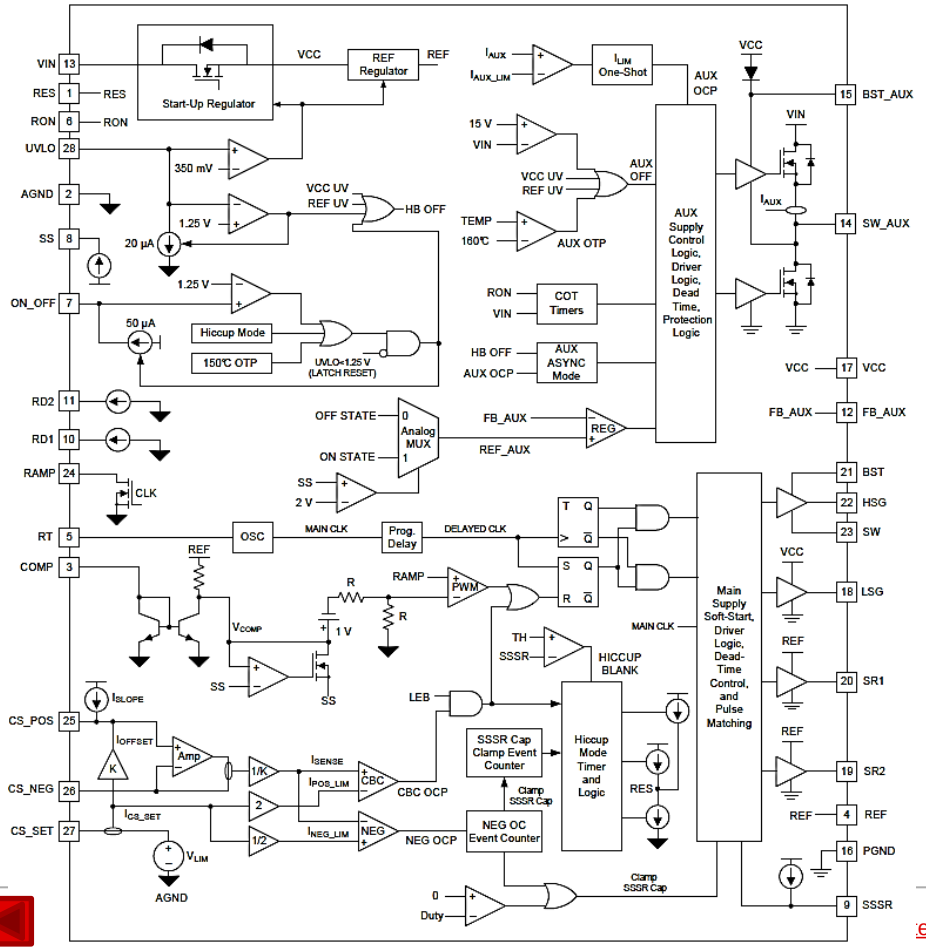


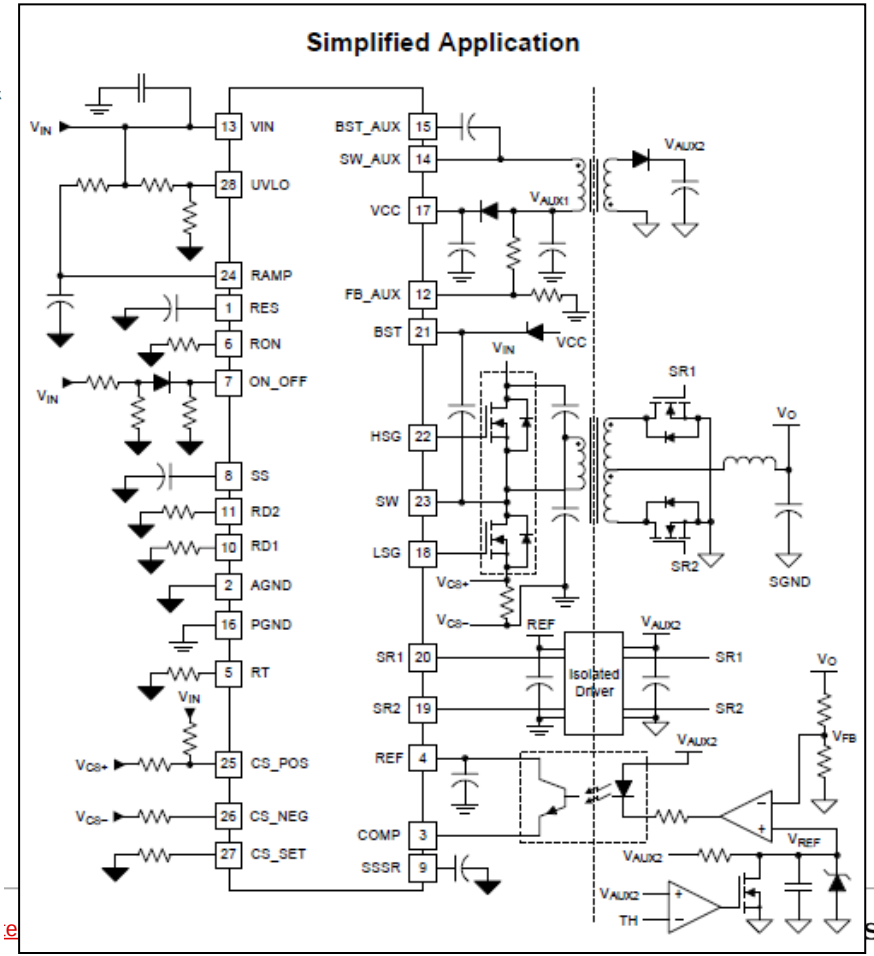




- Power Stage Designer™ is a Java® based *free tool* that helps engineers speed up their power supply designs as it calculates voltages and currents of 20 topologies according to the user's inputs.
- Additionally, PowerStage Designer contains a Bode plotting tool and a helpful toolbox with various functions for power supply design.
- More info: http://www.ti.com/tool/POWERSTAGE-DESIGNER

Function Block Diagram



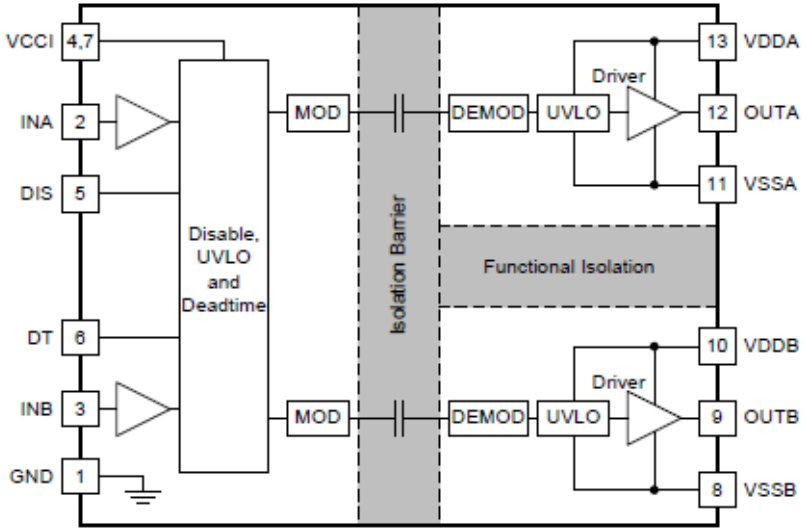


UCC21225A Overview

A closer look at the UCC21225A

- Universal: Dual Low-Side, Dual High-Side or Half-Bridge driver
- 5 x 5 mm, Space-Saving LGA-13 Package
- 6A/4A Sink/Source current capability
- 19ns propagation delay typ.
- Typical over 100V/ns CMTI
- Up to 5MHz operation
- 2.5kV basic isolation
- 700V channel to channel isolation
- <1ns pulse width
- distortion and delay matching, typ.
- 3~18V wide input range, and 6.5~25V wide output voltage range
- Programmable overlap, and interlock/delay time from 0ns~5us
- Fail safe with output low
- Isolation Barrier Life >40 Years
- UVLO options: 5V, 8V
- Pin-2-Pin compatible to industry standard

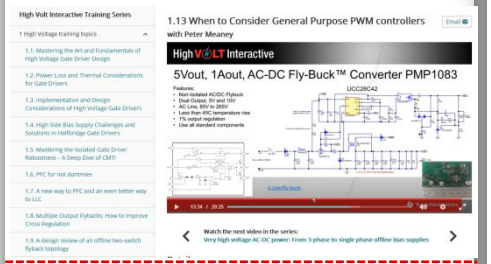
Functional Block Diagram



More Technical Resources

Training Videos

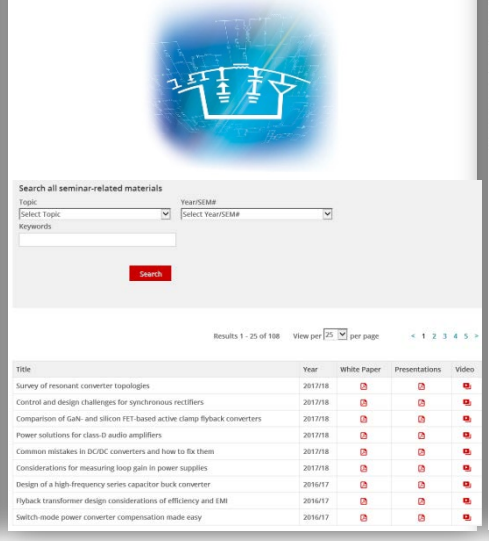
High Volt Interactive Training Series



Offline and Isolated DC/DC Controllers and Converters

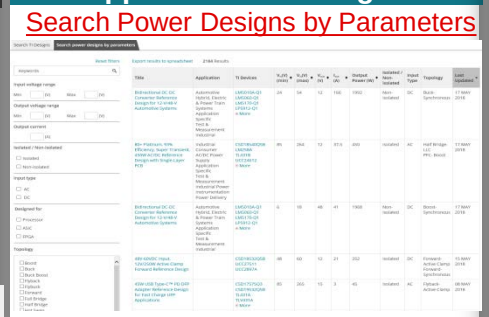
Power Supply Design Seminar

TI Power Supply Design Seminar Resources

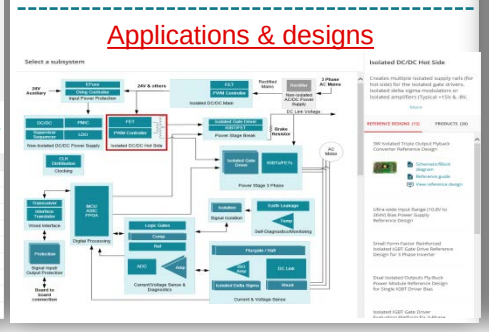


Reference Designs Applications & designs

Search Power Designs by Parameters

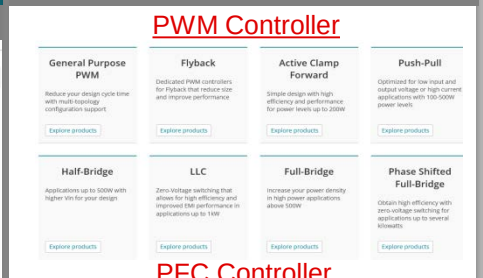


Applications & designs



PWM, PFC controllers at ti.com E2E Forum

PWM Controller



PFC Controller

E2E AC/DC and Isolated DC/DC Power Forum

Support: E2E AC/DC and Isolated DC/DC Power Forum

Texas Instruments

Thank you