

DESIGN NOTE:
 Vin Min = 5.5 Volts | Vin Max = 65 Volts
 Input Quiescent Current: 1.4 mA (Typ) | 1.7 mA (Max)
 Input Shutdown Current: 9 µA (Typ) | 15 µA (Max)
 OVP_{TH} (OVP threshold): 1.68 V (Min) | 2.0 V (Typ) | 2.12 V (Max)
 OVP_{HYS} (OVP hysteresis): 240 mV (Typ)
 UVLO_{TH} (UVLO threshold): 1.45 V (Min) | 1.6 V (Typ) | 1.75 V (Max)
 UVLO_{HYS} (UVLO hysteresis): 120 mV (Min) | 150 mV (Typ) | 230 mV (Max)

DESIGN NOTE: Program OVP and UVLO Thresholds
 • V_{OVP} = 2V and V_{in} = 50V → R18 = 15kΩ | R11 = 360kΩ
 • V_{UVLO} = 1.6V and V_{in} = 8V → R19 = 15kΩ | R12 = 57.1kΩ → 57.6kΩ

DESIGN NOTE:
 To slow down the output rise time a capacitor from the GATE pin to GND may be added. The turn on time depends on the threshold level of the N-Channel MOSFET, the gate capacitance of the MOSFET as well as the optional capacitance from the GATE pin to GND.

DESIGN NOTE:
 1. Pin 3: OVP - Over-voltage protection comparator input: The GATE pin is pulled low when OVP exceeds the typical 2.0-V threshold, but the controller is not latched off. Normal operation resumes when the OVP pin falls below typically 1.75 V.
 2. Pin 4: UVLO - Under-voltage lock-out comparator input: The UVLO comparator is activated when EN is high. A voltage greater than typically 1.6 V at the UVLO pin will release the pull down devices on the GATE pin and allow the output to gradually rise.
 3. Pin 5: EN - Enable input: A voltage greater than 2.0 V on the EN pin enables the internal bias circuitry and the UVLO comparator. The GATE pin pull-up bias is enabled when both EN and UVLO are in the high state.

DESIGN NOTE: Program OVP and UVLO Thresholds

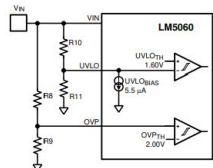


Figure 30. Programming the Thresholds with Resistors R8-R11

Choose the upper UVLO thresholds to ensure operation down to the lowest required operating input voltage (V_{INMIN}). Select R11 based on resistive divider current consumption and noise sensitivity. A value less than 100 kΩ is recommended, with lower values providing improved immunity to variations in UVLO_{BIAS}.

$$R10 = \frac{V_{INMIN} - UVLO_{TH}}{UVLO_{BIAS} + \frac{UVLO_{TH}}{R11}} \quad (12)$$

To calculate the UVLO low threshold including its hysteresis, use (UVLO_{TH}-UVLO_{HYS}) instead of UVLO_{TH} in the formula above. Choose the lower OVP threshold to ensure operation up to the highest VIN voltage required (V_{INMAX}). Select R9 based on resistive divider current consumption. A value less than 100 kΩ is recommended.

$$R8 = R9 \times \left(\frac{V_{INMAX} - OVP_{TH}}{OVP_{TH}} \right) \quad (13)$$

To calculate the OVP low threshold including hysteresis, use (OVP_{TH}-OVP_{HYS}) instead of OVP_{TH}. Where the R9-R11 resistor values are known, the threshold voltages are calculated from the following:

$$V_{INMAX} = OVP_{TH} + \frac{R8 \times OVP_{TH}}{R9} \quad (14)$$

$$V_{INMIN} = UVLO_{TH} + \left[R10 \times \left(UVLO_{BIAS} + \frac{UVLO_{TH}}{R11} \right) \right] \quad (14)$$

Also in these two formulas, the respective low value including the threshold hysteresis is calculated by using (UVLO_{TH}-UVLO_{HYS}) instead of UVLO_{TH} and (OVP_{TH}-OVP_{HYS}) instead of OVP_{TH}. The worst case thresholds, over the operating temperature range, can be calculated using the respective minimum and maximum values in bold font in the *Electrical Characteristics*.

Option C: The OVP function can be disabled by grounding the OVP pin. The UVLO thresholds are set as described in Figure 30.

LAYOUT NOTE:
 Review layout notes in the TI Designs: TIDA-01167 (TIDUC414) on the page 33.

DESIGN NOTE:
 Review different tests in the TI Designs: TIDA-01167 (TIDUC414) application note.

LAYOUT NOTE:
 Review layout notes in the data sheet on the page 31.

DESIGN NOTE: LM5060 Operating Conditions

Table 1. Overview of Operating Conditions

EN	UVLO	INPUTS			OUTPUTS				STATUS		
		OVP (typ)	VIN (typ)	SENSE-OUT	GATE -OUT	VIN Current (typ)	GATE Current (typ)	TIMER		GATE after TIMER > 2 V	nPGD
L	L	-	>5.10 V	-	-	0.009 mA	2.2 mA sink	Low	-	-	Disabled
L	H	-	>5.10 V	-	-	0.009 mA	2.2 mA sink	Low	-	-	Disabled
H	L	<2 V	>5.10 V	SENSE>OUT SENSE<OUT	-	0.56 mA	2.2 mA sink	Low	-	H L	Standby
H	L	>2 V	>5.10 V	SENSE>OUT SENSE<OUT	-	0.56 mA	80 mA sink	Low	-	H L	Standby
H	H	<2 V	>5.10 V	SENSE>OUT SENSE<OUT	<5 V	1.4 mA	24-µA source	6-µA source Low	80 mA sink -	H L	Enabled
H	H	<2 V	>5.10 V	SENSE>OUT SENSE<OUT	>5 V	1.4 mA	24-µA source	11-µA source Low	80 mA sink -	H L	Enabled
H	H	>2 V	>5.10 V	SENSE>OUT SENSE<OUT	-	1.4 mA	80 mA sink	Low	-	H L	Over-voltage
H	H	<2 V	<5.10 V	-	-	1.4 mA	2.2 mA sink (see ⁽¹⁾)	Low	-	H	Power on reset

(1) The 2.2 mA sink current is valid for with the VIN pin ≥ 5.1 V. When the VIN pin < 5.1 V the sink current is lower. See 'GATE Pin Off Current vs. VIN' plot in *Typical Characteristics*.