LM5067 reverse current surge – restart issue

Engineer: Artem Rogachev

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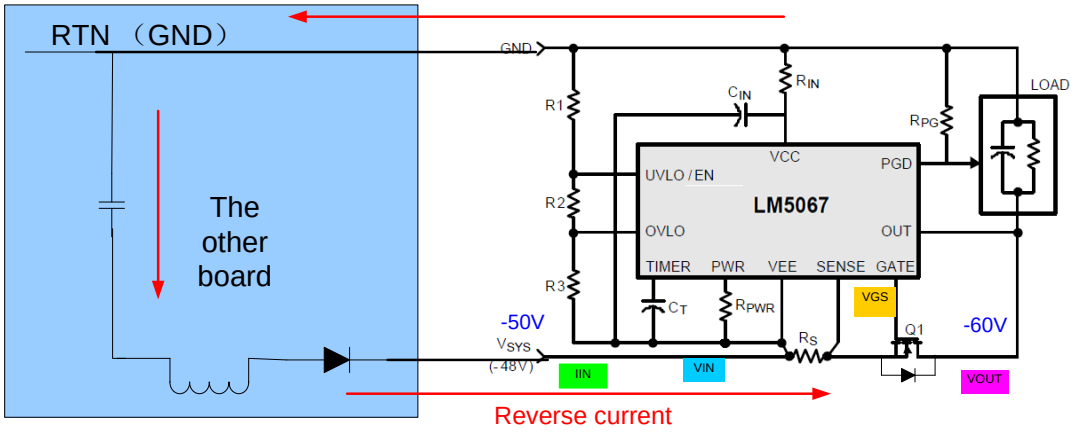
Issue Summary: During Differential Mode test, there is a lot of reverse current going through the sense resistor and FET and it was noticed that this triggered the insertion timer in the part.

Cause: The large reverse current causes a reverse voltage across Rsns and Vout. This causes OUT and SENSE to go significantly below VEE (IC ground), which causes minority carrier injection and interferes with the IC's circuitry. This effect was experimentally quantified to ensure that the proposed solution is robust.

Solution: Add a series resistor to the Vout pin and consider adding a series resistor/Shottkey combo to the Sense pin. More details on the solution is provided further in the report.



1) Pin Voltage during negative surge.

Note that both the sense resistor and FET have parasitic inductance. Thus during a large dI/dT the voltage across these elements can be a lot larger than I*R.

The following equations can be used:

Vsense – VEE = I_rev * Rsns + di_rev/dt *Lsns

Vout – Vee = -I_rev * (Rsns + Rfet) – di_rev/dt*(Lsns + Lfet+Ltrace)

Based on waveform below & schematic assume:

Rsns = 2.5 mili-ohm; Rfet = 10 mili-ohm, I_rev = 50A, dI_rev/dt ~ 25 A / us.

Also assume that Lsns ~ 3 nH, Lfet ~ 12nH, Ltrace ~ 5 nH. This implies:

Vout – Vee = -(10+2.5)mili-ohm*50A – (3nH+5nH+12nH)*25A/us = -750mV – 500 mV ~ -1.25V

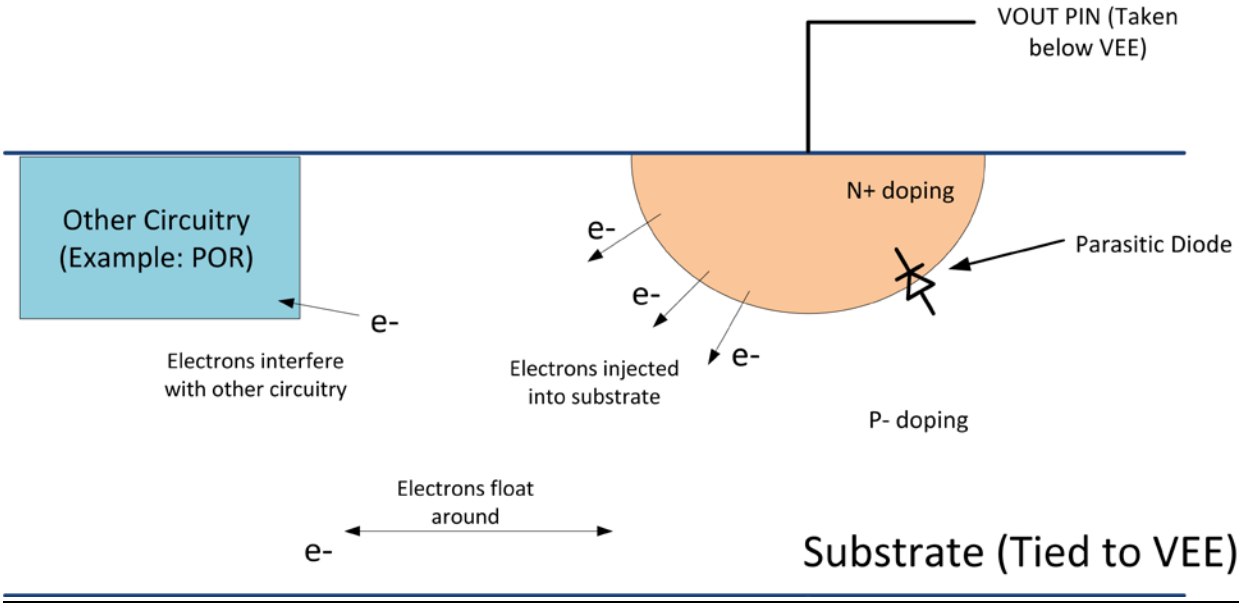
If Vout is taken -1.25V below Vee , IC's operation will be compromised!!

2) Consequence of taking pins below GND.

The diagram below gives a high level view of how the IC is affected when one of the pins is taken below VEE.

- In the IC the substrate is connected to VEE (often referred to IC gnd)
- All pins are connected to an N+ doped reservoir, while the substrate is a lightly P doped.
- This results in a parasitic diode. When VOUT pin is taken below VEE the diode is forward biased and electrons are injected into the substrate.
- Many of them will be collected at the VEE pin, recombine, or get caught by a guard ring.
- However, some electrons will float to other circuitry and interfere with its operation. In general the more electrons are injected; the more likely it is for other circuitry to be affected.
- A series resistor with Vout will limit the current and hence the # of electrons being injected
- A resistor / Shottkey diode combination will clamp the voltage at the pin and prevent the parasitic diode from turning on.

It's hard to quantify the current injection threshold where the IC will start to malfunction based on simulation or theory. The best approach is to take some lab measurements.



3) Quantifying the Breaking Point for I_{OUT}

The following sets of experiments were performed to quantify how much current the pins can take before improper operation is observed.

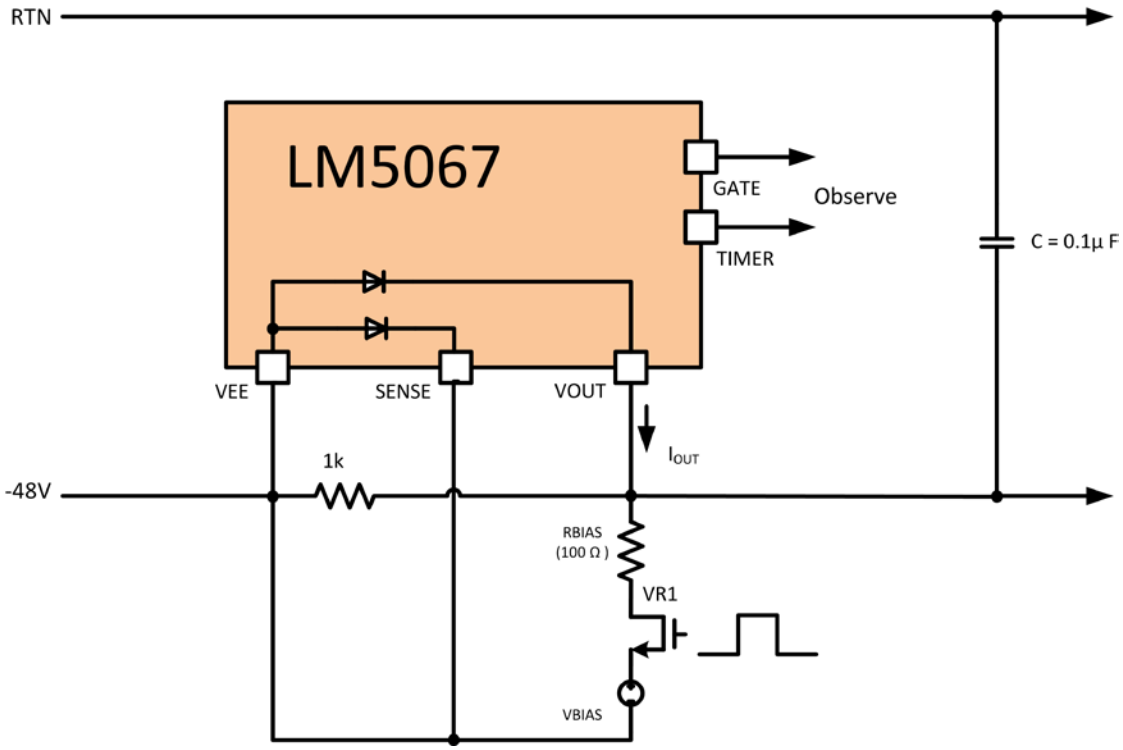
The diagram below shows the set-up for quantifying how much I_{OUT} current the part can handle. VBIAS is gradually increased and GATE and TIMER are observed. Both the threshold that causes the Gate to come down and the threshold that causes an insertion delay are recorded. For these tests the pulse width was 100µs.

Both VR1 and VOUT are recorded so I_{OUT} can be computed as follows:

I_{OUT} = (VOUT – VR1)/100Ω + VOUT / 1kΩ

For example if VOUT = -0.684V and VR1 = -0.9V:

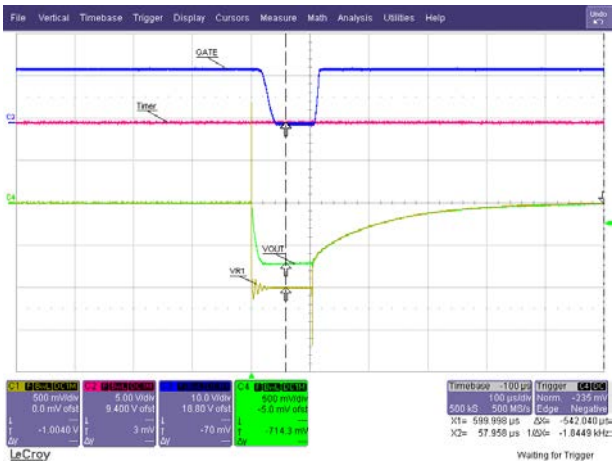
I_{OUT} = (-0.684V - (-0.9V))/ 100Ω - 0.684 / 1kΩ = 2.16mA – 0.684mA = 1.476mA.



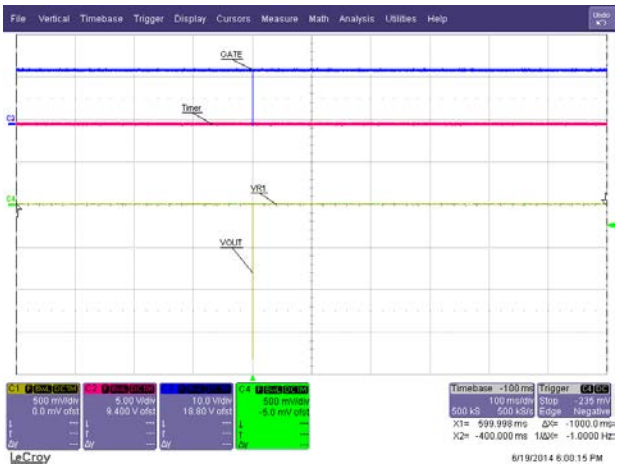
With the set-up above, the following data was collected. Note that it takes about 2mA of I_{OUT} current to make the gate go down. However it takes ~17mA to trigger an insertion delay.

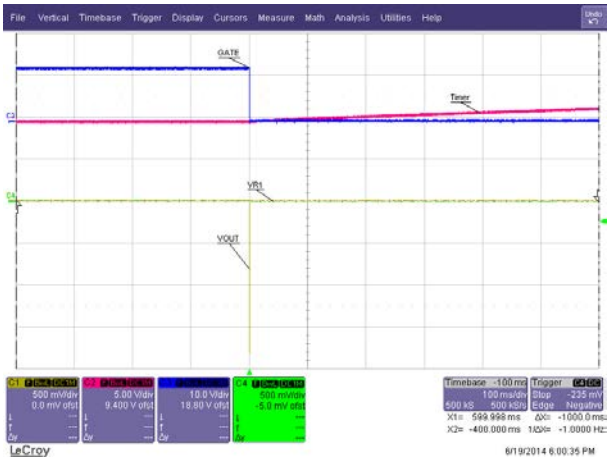
VBIAS (V)	VR1(V)	VOUT (V)	IOUT (mA)	GATE TRIPS	Insertion Delay Triggered?
0.9	-0.9	-0.684	1.476	N	N
0.95	-0.962	-0.7	1.92	partial	N
1	-1	-0.714	2.146	Y	N
2.65	not measured			Y	N
2.7	-2.7	-0.92	16.88	Y	Y

The waveform below show the response of the LM5067 with a VBIAS of 0.9V, 0.95V and 1V respectively. Note that at 0.95V the gate comes down, but then returns immediately. Most likely there is some overshoot on VOUT during the transition that originally trips the gate, but it's able to recover.

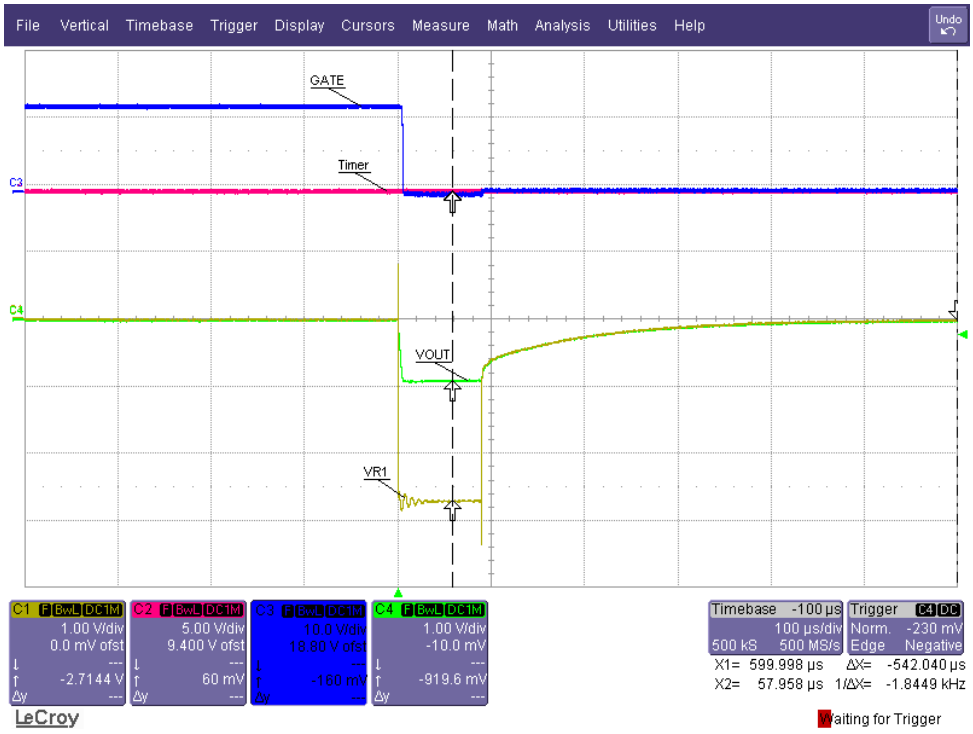


To find the threshold for triggering the insertion delay, VBIAS was raised until the insertion delay was observed. The left waveform was with a VBIAS of 2.65V and an insertion delay wasn't observed. The right waveform was with a VBIAS of 2.7V and an insertion delay was observed.





Once it was concluded that a VBIAS of 2.7V triggers an insertion delay, we zoomed in to find the corresponding VOUT and VR1 and t compute the IOUT.



4) Quantifying the Breaking Point for I_{SENSE}

A similar set-up was used to quantify the breaking point of the sense pin. The picture below shows the set-up and the table summarizes the findings. Note that the SENSE pin is able to handle a larger amount of current then the OUT pin. Also pulling current out of sense (up to 87mA) didn't result in the triggering of the insertion delay.

VBIAS (V)	VR1(V)	VSENSE (V)	IOUT (mA)	GATE TRIPS	Insertion Delay Triggered?
1.5	-1.49	-0.8	6.1	N	N
1.6	-1.59	-0.813	6.957	partial	N
1.7	-1.69	-0.822	7.858	Y	N
10	-10	-1.1	87.9	Y	N

5) Proposed Solution

The diagram below shows a proposed solution. If Rout is sufficiently large it will limit the current into the VOUT_IC pin and ensure proper operation. Note that there is some leakage current on the VOUT_IC and that will cause some offset. However, VOUT_IC is used for power limiting (sensing Vds) and to measure the PGd threshold (1.2V), hence an offset less than 0.25V shouldn't cause any issues.

When adding R1, the effect of the offset is much more significant, because the controller uses SENSE_IC for current limiting and power limiting. Thus adding R1 has some inherent risk and the offset should be carefully computed.

Based on test results, a Rout of 1.5kΩ without R1 or D1 should be sufficient to avoid all issues. However, if further protection is desired adding a 5 ohm for R1 and a Shottkey diode for D1 will result in a more "bullet-proof" solution. A calculator is attached with the report to help crunch the numbers.