

## N-Channel 100 V (D-S) MOSFET

### DESCRIPTION

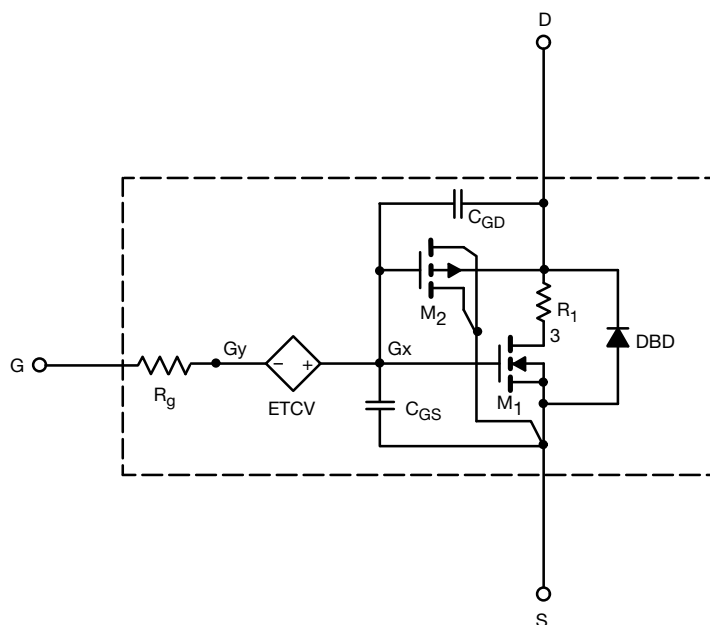
The attached SPICE model describes the typical electrical characteristics of the n-channel vertical DMOS. The subcircuit model is extracted and optimized over -55 °C to 125 °C temperature ranges under the pulsed 0 V to 10 V gate drive. The saturated output impedance is best fit at the gate bias near the threshold voltage.

A novel gate-to-drain feedback capacitance network is used to model the gate charge characteristics while avoiding convergence difficulties of the switched  $C_{gd}$  model. All model parameter values are optimized to provide a best fit to the measured electrical data and are not intended as an exact physical interpretation of the device.

### CHARACTERISTICS

- N-channel vertical DMOS
- Macro model (subcircuit model)
- Level 3 MOS
- Apply for both linear and switching application
- Accurate over -55 °C to +125 °C temperature range
- Model the gate charge

### SUBCIRCUIT MODEL SCHEMATIC



### Note

- This document is intended as a SPICE modeling guideline and does not constitute a commercial product datasheet. Designers should refer to the appropriate datasheet of the same number for guaranteed specification limits.



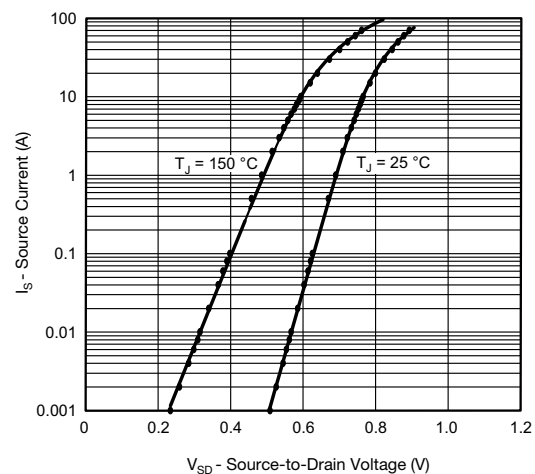
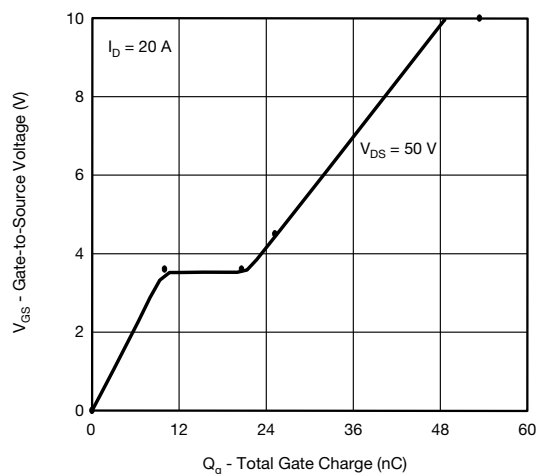
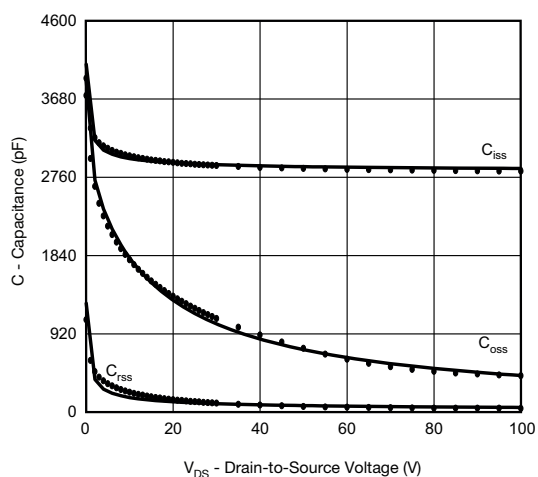
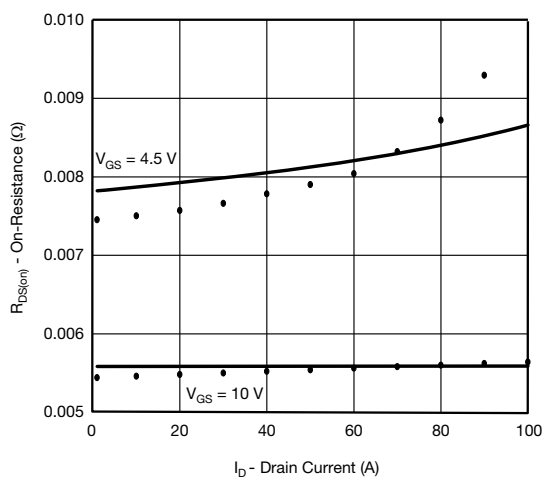
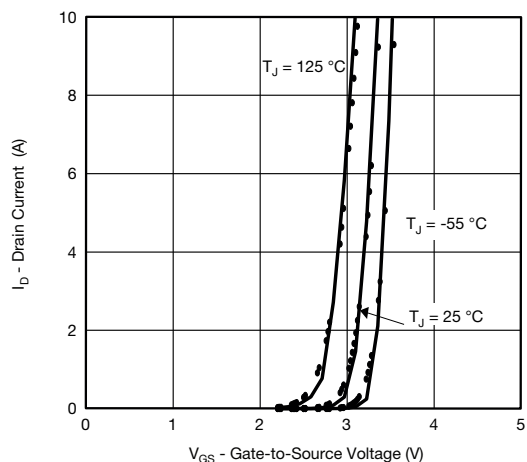
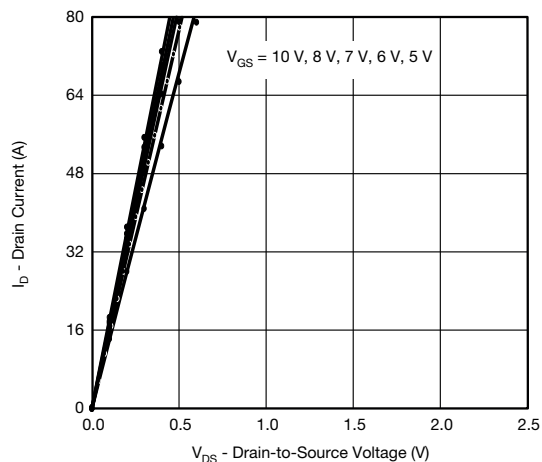
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)					
PARAMETER	SYMBOL	TEST CONDITIONS	SIMULATED DATA	MEASURED DATA	UNIT
<b>Static</b>					
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	2.3	-	V
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	0.0056	0.0055	Ω
		V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 15 A	0.0078	0.0075	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 20 A	72	68	S
Diode forward voltage	V <sub>SD</sub>	I <sub>S</sub> = 5 A	0.74	0.74	V
<b>Dynamic <sup>b</sup></b>					
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 0 V, f = 1 MHz	2890	2866	pF
Output capacitance	C <sub>oss</sub>		733	719	
Reverse transfer capacitance	C <sub>rss</sub>		76	66	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A	55	53.5	nC
		V <sub>DS</sub> = 50 V, V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A	26	25.2	
Gate-source charge	Q <sub>gs</sub>		10	10	
Gate-drain charge	Q <sub>gd</sub>		10.6	10.6	

**Notes**

- a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %  
b. Guaranteed by design, not subject to production testing



## COMPARISON OF MODEL WITH MEASURED DATA ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)



### Note

- Dots and squares represent measured data.

Copyright: Vishay Intertechnology, Inc.