WIDE $V_{IN}$ DC/DC Power Solutions
Reliable Power for Demanding Systems

# LM(2)5143/-Q1 Synchronous Buck Controller Design Tool

About | = Input Box | TERMS OF USE

## Step 1: Operating Specifications

LM5143A-Q1

Single Output – 4 Phases

| | | |
|---|---|---|
| **Input Voltage – Min, $V_{IN(min)}$** | **30** | V |
| **Input Voltage – Nom, $V_{IN(nom)}$** | **49** | V |
| **Input Voltage – Max, $V_{IN(max)}$** | **50** | V |
| **Output Voltage, $V_{OUT}$** | **15** | V |
| **Full Load Output Current, $I_{OUT}$** | **70** | A |
| **Switching Frequency, $F_{SW}$** | **2200** | kHz |
| Frequency Set Resistor, $R_T$ | 10 | kΩ |
| **Ambient Temperature, $T_A$** | **25** | °C |

## Step 2: Current Sense Resistors

Shunt current sensing

| | | |
|---|---|---|
| **Required $I_{OCP}$ Setpoint at $V_{IN(nom)}$** | **30** | A |
| Recommended Sense Resistance | 7.4 | mΩ |
| **Sense Resistance, $R_S$** | **2** | mΩ |
| Min Inductor Sat Current, $I_{LO(SAT)}$ | 36.5 | A |
| Max power loss in shunt | 2.42 | W |
| $I_{OUT(typ)}$ at OCP Inception: $V_{IN(min)}$ | 139.2 | A |
| $V_{IN(nom)}$ | 136.5 | A |
| $V_{IN(max)}$ | 136.4 | A |

## Step 3: Buck Inductances

| | | |
|---|---|---|
| Ch1 Recommended Inductance | 0.57 | µH |
| **Ch1 Inductance, $L_{O1}$** | **1** | **µH** |
| **Ch1 Inductor DCR** | **2** | **mΩ** |
| $\Delta I_L$ as a % at $V_{IN(nom)}$ | 27 | % |

## Step 4: Output Capacitors

| | | |
|---|---|---|
| **Output Voltage Ripple Spec** | **400** | **$mV_{pk-pk}$** |
| Minimum Output Capacitance | 2.2 | µF |
| **Output Capacitance (derated), $C_{OUT}$** | **264** | **µF** |
| Maximum Permitted ESR | 84 | mΩ |
| **Output Capacitor ESR** | **3** | **mΩ** |
| Resulting Output Voltage Ripple (max) | 14 | $mV_{pk-pk}$ |
| Output Capacitor RMS Current (max) | 1.38 | A (rms) |

## Step 5: Input Capacitors

| | | |
|---|---|---|
| **Input Voltage Ripple Spec** | **2500** | **$mV_{pk-pk}$** |
| Minimum Input Capacitance | 10 | µF |
| **Input Capacitance, $C_{IN}$** | **20.047** | **µF** |
| Maximum Permitted ESR | 120.7 | mΩ |
| **Input Capacitor ESR** | **1** | **mΩ** |
| Resulting Input Voltage Ripple (max) | 119 | $mV_{pk-pk}$ |
| Input Capacitor RMS Current (max) | 8.75 | A (rms) |

## Step 6: Soft-start, Hiccup, Dither, DEMB, MODE

| | | |
|---|---|---|
| **Soft-Start Time, $t_{SS}$** | **3** | **ms** |
| Soft-Start Capacitance, $C_{SS}$ | 100 | nF |
| **Hiccup Fault Time, $t_{RES}$** | **12** | **ms** |
| RES Capacitance, $C_{RES}$ | 220 | nF |

DITHER Disable

FPWM

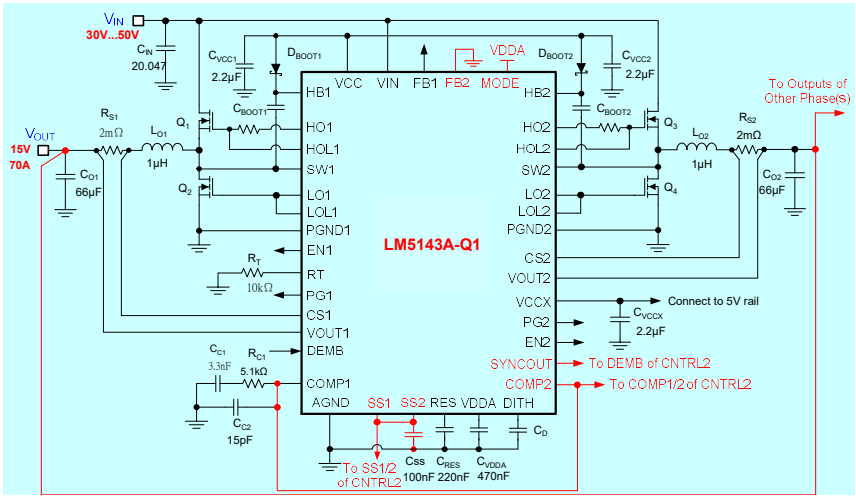
*Tie DITH to VDDA
* Tie DEMB to VDDA
* Tie MODE to VDDA

## Step 7: Compensation Design

| | | |
|---|---|---|
| Load Pole Frequency | 3620 | Hz |
| ESR Zero Frequency | 201 | kHz |
| **Desired Crossover Frequency** | **60** | **kHz** |
| Error Amp Pole Frequency | 0.8 | Hz |
| **Upper Feedback Resistor** | **240** | **kΩ** |
| Lower Feedback Resistor | 10 | kΩ |

**Compensation Components**

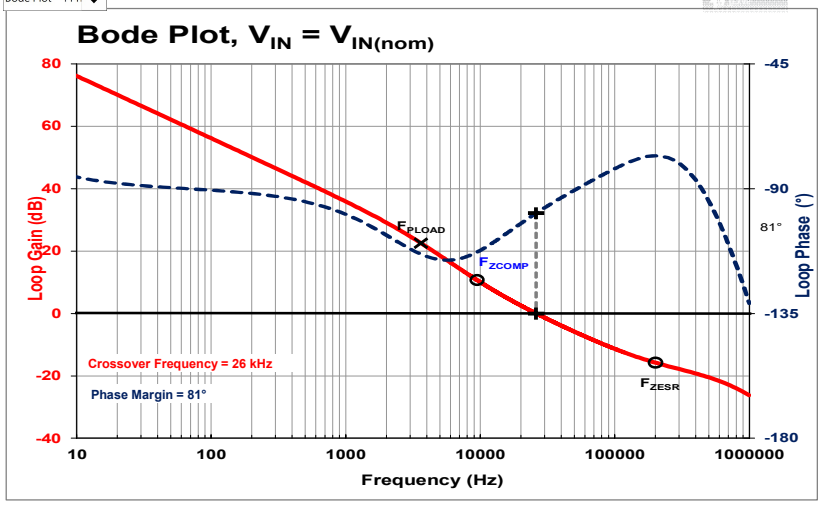
| | Calculated / | Std Values | Std Values | | Actual P/Z Frequencies |
|---|---|---|---|---|---|
| $R_{C1}$ | 12.4 | 12.4 | **5.1** | **kΩ** | 1 Hz ($F_{PEA}$) |
| $C_{C1}$ | 2.1 | 2.2 | **3.3** | **nF** | 9.5 kHz ($F_{ZCOMP}$) |
| $C_{CZ}$ | 57 | 56 | **15** | **pF** | 1461 kHz ($F_{PCOMP}$) |




** For Single-Output Operation in 4-Phase Mode, tie both MODE pins to VDDA. Use FB1 of master IC to set VOUT. Connect FB2 of master IC to AGND. Connect FB2 of slave IC to VDDA to configure it as a slave **
** Slave controller (CNTRL2) not shown **
** Tie VCCX to GND if not used **

Wide Input Voltage

Bode Plot - 4 Ph




** Specify Inductor Core Loss ** 0.3 W

## Efficiency / Power Loss Analyzer

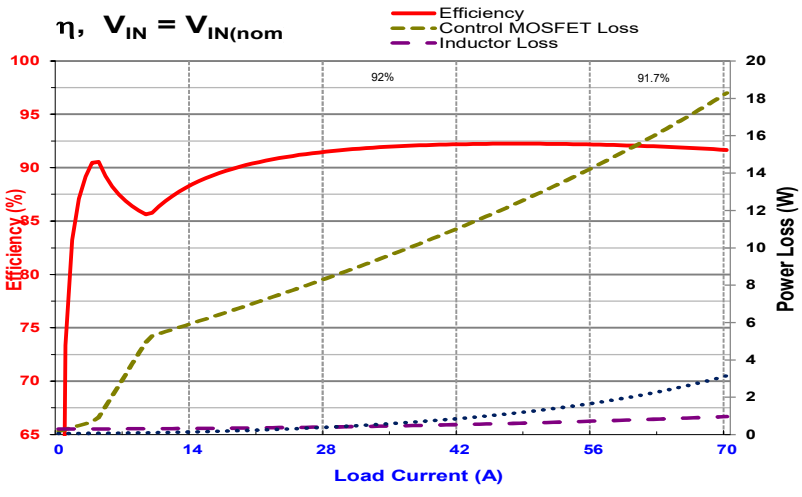
### Step 8: Efficiency

| | Power MOSFETs ISC0805NLS, ISC0805NLS High-side | Low-side | |
|---|---|---|---|
| **On-State Resistance, $R_{DS(on)}$** | **9.0** | **9.0** | mΩ |
| **Total Gate Charge, $Q_G$** | **13** | **13** | nC |
| **Gate-Drain Charge, $Q_{GD}$** | **4.7** | **4.7** | nC |
| **Gate-Source Charge, $Q_{GS}$** | **6** | **6** | nC |
| **Output Charge, $Q_{OSS}$** | | **34** | nC |
| **Output Capacitance, $C_{OSS}$** | **280** | **280** | pF |
| **Gate Resistance, $R_G$** | **1** | **1** | Ω |
| **Transconductance, $g_{FS}$** | **73** | **73** | S |
| **Gate-Source Threshold Voltage, $V_{TH}$** | **1.6** | **1.6** | V |
| **Body Diode Forward Voltage, $V_{BD}$** | **0.92** | **0.92** | V |
| **Body Diode Rev Recovery Charge, $Q_{RR}$** | | **28** | nC |
| **Thermal Resistance, $\theta_{JA}$** | **50** | **50** | °C/W |

**External Schottky Diode (if applicable)**

| | | |
|---|---|---|
| **Schottky Fwd Voltage, $V_{FWDsch}$** | **0.46** | V |
| **Schottky Rev Recovery Charge, $Q_{RRsch}$** | **1.5** | nC |

Efficiency vs. IOUT - 4 Ph




### Step 9: IC Power Loss

VCCX Connected

| | | |
|---|---|---|
| IC Power Dissipation | 0.57 | W |
| IC Junction Temperature (estimate) | 44.9 | °C |