WIDE V_{IN} DC/DC Power Solutions
Reliable Power for Demanding Systems

LM5146-Q1 DC-DC Controller Design Tool

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Step 1: Operating Specifications

Input Voltage – Min, $V_{IN(min)}$	**40**	**V**
Input Voltage – Nom, $V_{IN(nom)}$	**48**	**V**
Input Voltage – Max, $V_{IN(max)}$	**60**	**V**
Output Voltage, V_{OUT}	**12**	**V**
Maximum Output Current, I_{OUT}	**8**	**A**
Free-running Switching Frequency, F_{SW}	**540**	**kHz**
SYNC Frequency (if used), $F_{SW-SYNC}$	**540**	**kHz**
Frequency Set Resistor, R_{RT}	18.7	kΩ

Step 2: Filter Inductor

Recommended Filter Inductance	6.3	µH
Inductance, L_F	**4.7**	**µH**
Inductor DCR	**15**	**mΩ**
Pk-to-Pk Ripple Current at $V_{IN(nom)}$, ΔI_L	3.6	A_{pk-pk}
Inductor Ripple Current as a % of Max I_{OUT}	45	%

Step 3: $R_{DS(on)}$ or Shunt-Based Current Limit

Shunt, R_S	**4.4**	**mΩ**
Required Current Limit Setpoint	**8**	**A**
Current Limit Set Resistor, R_{ILIM}	274	Ω
Min Inductor Sat Current, $I_{L(SAT)}$	12.0	A
Power Loss in R_S at Full Load, Max V_{IN}	0.18	W

Step 4: Output Capacitance

Output Voltage Ripple Specification	**100**	**mV_{pk-pk}**
Minimum Ideal Output Capacitance	8	µF
Total Output Capacitance (Derated), C_{OUT}	**100**	**µF**
Maximum Permitted ESR	28	mΩ
Output Capacitor ESR	**5**	**mΩ**
Resulting Output Voltage Ripple	20	mV_{pk-pk}
Output Capacitor Ripple Current	1.0	A (rms)

Step 5: Input Capacitance

Input Voltage Ripple Specification	**500**	**mV_{pk-pk}**
Minimum Ideal Input Capacitance	6	µF
Total Input Capacitance (Derated), C_{IN}	**10**	**µF**
Maximum Permitted ESR	22	mΩ
Input Capacitor ESR	**3**	**mΩ**
Resulting Input Voltage Ripple	310	mV_{pk-pk}
Input Capacitor Ripple Current	3.5	A (rms)

Step 6: Soft-start, UVLO

Soft-Start Time, t_{SS}	**4**	**ms**
Soft-Start Capacitance, C_{SS}	47	nF
Input Voltage UVLO Turn-On	**14**	**V**
Input Voltage UVLO Turn-Off	**13**	**V**
UVLO Upper Resistor, R_{UV1}	100	kΩ
UVLO Lower Resistor, R_{UV2}	9.31	kΩ

If the SYNC feature is not required, connect SYNCIN to GND or VCC for DCM or CCM operation, respectively

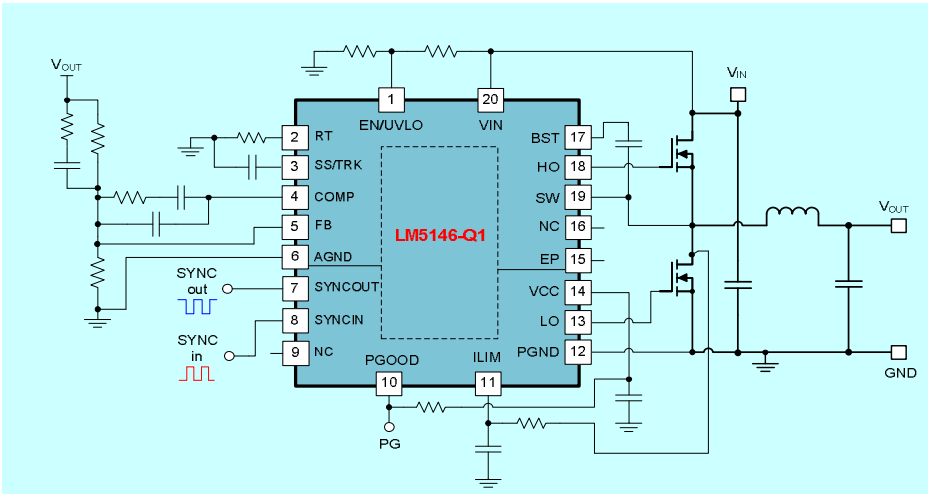
Step 7: Compensation Design

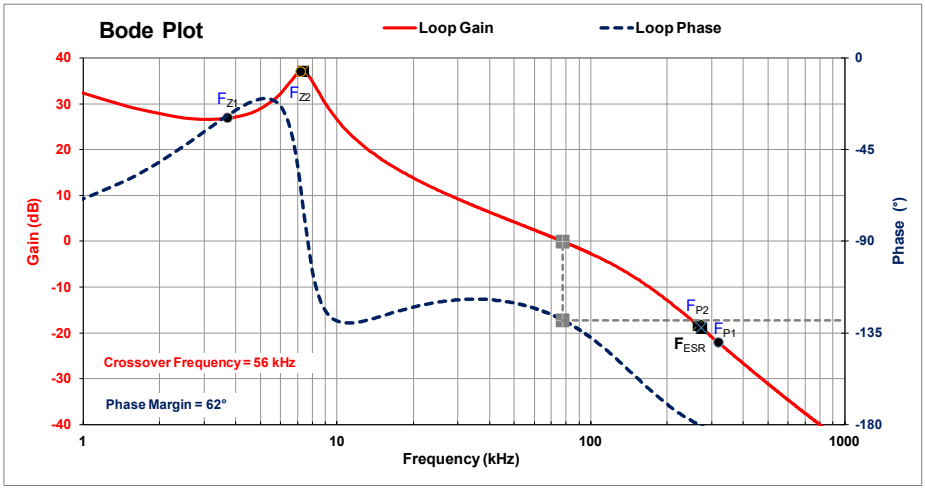
LC Complex Pole Frequency	7.4	kHz
ESR Zero Frequency	318	kHz
Desired Crossover Frequency	**63**	**kHz**
Appropriate Midband Gain	0.57	V/V
Upper Feedback Resistor, R_{FB1}	**18**	**kΩ**
Lower Feedback Resistor, R_{FB2}	1.3	kΩ
Actual Output Voltage, V_{OUT}	11.877	V

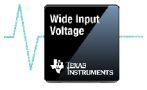
Pole & Zero Placement	F_{Z1}	**5.2**	**kHz**
Baseline P/Z Frequencies:	F_{Z2}	**6.6**	**kHz**
	F_{P1}	**318**	**kHz**
	F_{P2}	**270**	**kHz**

Compensation Components

	Calculated	Std Values	Selected	Actual P/Z Frequencies
R_{C1}	10.3	10.2	**13 kΩ**	**3.7 kHz (F_{Z1})**
C_{C1}	3007	3300	**3300 pF**	**7.2 kHz (F_{Z2})**
C_{C2}	59	56	**47 pF**	**272 kHz (F_{P1})**
R_{C2}	383	383	**487 Ω**	**264 kHz (F_{P2})**
C_{C3}	1306	1200	**1200 pF**	







** Specify Inductor Core Loss ** **0.4** W

Efficiency / Power Loss Analyzer

Step 8: Efficiency

High-Side MOSFET (Q_1) Specifications	CSD19534Q5A	
On-State Resistance, $R_{DS(on)}$	**13**	mΩ
Total Gate Charge, Q_G	**20**	nC
Gate-Drain Charge, Q_{GD}	**3.2**	nC
Gate-Source Charge, Q_{GS}	**5.1**	nC
Output Capacitance, C_{OSS}	**300**	pF
Gate Resistance, R_G	**1.5**	Ω
Transconductance, g_{FS}	**47**	S
Gate-Source Threshold Voltage, $V_{GS(TH)}$	**2.8**	V
Body Diode Forward Voltage, V_{SD1}	**0.9**	V
Thermal Resistance, θ_{JA}	**50**	°C/W

Low-Side MOSFET (Q_2) Specifications	BSC037N08NS5	
On-State Resistance, $R_{DS(on)}$	**4.4**	mΩ
Total Gate Charge, Q_G	**50**	nC
Output Charge, Q_{OSS}	**65**	nC
Output Capacitance, C_{OSS}	**600**	pF
Body Diode Forward Voltage, V_{SD2}	**1**	V
Body Diode Recovery Charge, Q_{RR}	**55**	nC
Thermal Resistance, θ_{JA}	**50**	°C/W
Antiparallel Schottky Diode (if applicable)		
Schottky Diode Forward Voltage, V_{SD}	**0**	V
Schottky Diode Recovery Charge, Q_{RR2}	**0**	nC