



About = Input Box TERMS OF USE

Step 1: Operating Specifications

Input Voltage - Min, $V_{IN(min)}$	24 V
Input Voltage - Nom, $V_{IN(nom)}$	48 V
Input Voltage - Max, $V_{IN(max)}$	55 V
Output Voltage, V_{OUT}	21.5 V
Full Load Output Current, I_{OUT}	3 A
Switching Frequency, F_{SW}	320 kHz
Frequency Set Resistor, R_T	68.1 kΩ
Ambient Temperature, T_A	40 °C

Step 2: Current Sense Resistor

Required I_{OCP} Setpoint at $V_{IN(nom)}$	4.5 A
Recommended Shunt Resistance	11.8 mΩ
Shunt Resistance, R_S	12 mΩ
Min Inductor Sat Current, $I_{L(SAT)}$	5.0 A
Max Power Loss in Shunt	0.29 W
V_{OUT} at OCP Inception: $V_{IN(min)}$	4.9 A
$V_{IN(nom)}$	4.4 A
$V_{IN(max)}$	4.4 A

Step 3: Buck Inductance

Inductance for Ideal Slope Comp	35.49 μH
Inductance, L_O	33 μH
Inductor DCR	40 mΩ
ΔI_L as a % at $V_{IN(nom)}$	38 %
Estimate Core Loss at $V_{IN(nom)}$	0.2 W

Step 4: Output Capacitors

Output Voltage Ripple Spec	50 mV _{PK-PK}
Minimum Output Capacitance	8.8 μF
Output Capacitance (derated), C_{OUT}	122 μF
Maximum Permitted ESR	44 mΩ
Output Capacitor ESR	1 mΩ
Resulting Output Voltage Ripple (max)	4 mV _{PK-PK}
Output Capacitor RMS Current (max)	0.36 A _{RMS}

Step 5: Input Capacitors

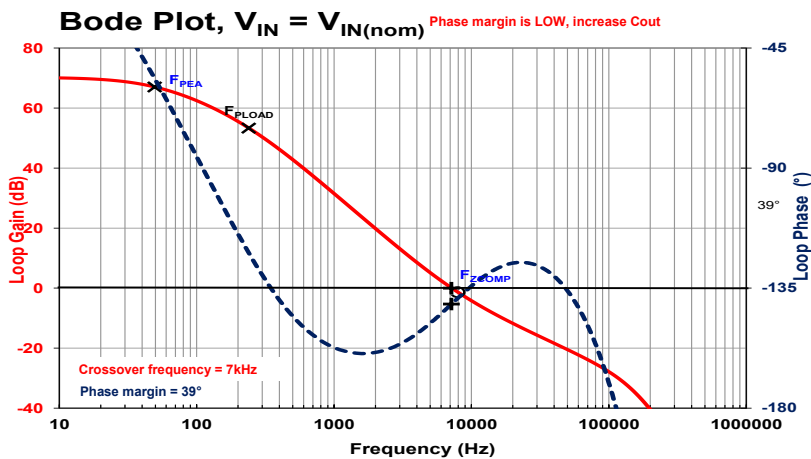
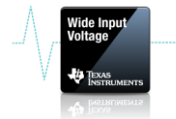
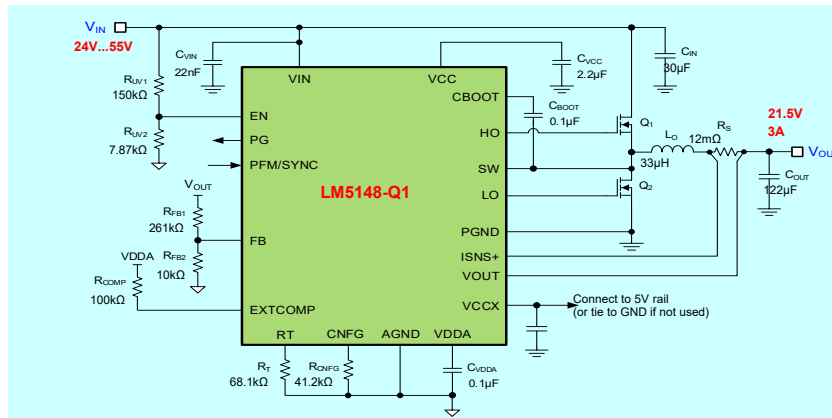
Input Voltage Ripple Spec	200 mV _{PK-PK}
Minimum Input Capacitance	12 μF
Input Capacitance (derated), C_{IN}	30 μF
Maximum Permitted ESR	33.6 mΩ
Input Capacitor ESR	1 mΩ
Resulting Input Voltage Ripple (max)	82 mV _{PK-PK}
Input Capacitor RMS Current (max)	1.5 A _{RMS}

Step 6: Precision Enable, DRSS, FPWM / PFM

UVLO Divider	DRSS Enabled	FPWM
Input Voltage UVLO Turn On	20 V	
Input Voltage UVLO Turn Off	18.5 V	
Upper Enable Resistor, R_{UV1}	150 kΩ	
Lower Enable Resistor, R_{UV2}	7.9 kΩ	
Configuration Resistor, R_{CNFG}	41.2 kΩ	
* Tie PFM to GND		

Step 7: Compensation Design

Internal Compensation	
Upper Feedback Resistor	261 kΩ
Lower Feedback Resistor	10 kΩ
Actual Output Voltage Setpoint	21.680 V



Efficiency / Power Loss Analyzer

Step 8: Efficiency

Power MOSFETs (Q_1, Q_2)		
	'852, '824	
	High-side	Low-side
On-State Resistance, $R_{DS(on)}$	8.8 mΩ	8.8 mΩ
Total Gate Charge, Q_G	25 nC	25 nC
Gate-Drain Charge, Q_{GD}	4.3 nC	4.3 nC
Gate-Source Charge, Q_{GS}	4.6 nC	4.6 nC
Output Charge, Q_{OSS}	12 nC	12 nC
Output Capacitance, C_{OSS}	192 pF	192 pF
Gate Resistance, R_G	1.2 Ω	1.2 Ω
Transconductance, g_{FS}	84 S	84 S
Gate-Source Threshold Voltage, V_{TH}	1.7 V	1.7 V
Body Diode Forward Voltage, V_{BD}	1.2 V	1.2 V
Body Diode Rev Recovery Charge, Q_{RR}	14 nC	14 nC
Thermal Resistance, θ_{JA}	41 °C/W	41 °C/W

External Schottky Diode (if applicable)	
Schottky Fwd Voltage, V_{FWDsch}	0 V
Schottky Rev Recovery Charge, Q_{RRsch}	0 nC

Step 9: IC Power Loss

VCCX Connected	IC Power Dissipation	0.08 W
	IC Junction Temperature (estimate)	42.7 °C

