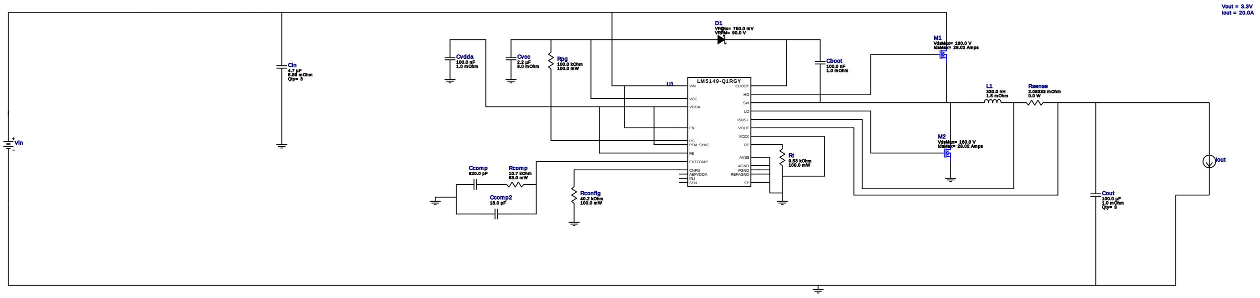
VinMin = 9.0V
VinMax = 60.0V
Vout = 3.3V
Iout = 20.0A

Device = LM5149RGYQ1
Topology = Buck
Created = 2023-05-31 07:37:07.605
BOM Cost = NA
BOM Count = 21
Total Pd =

WEBENCH ® Design Report

Design : 74 LM5149RGYQ1
LM5149RGYQ1 9V-60V to 3.30V @ 20A



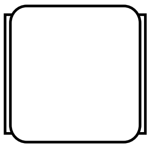
Design Alerts

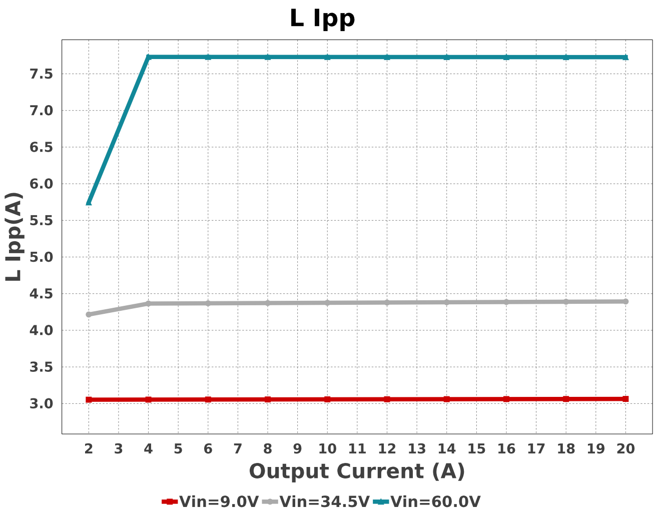
Component Selection Information

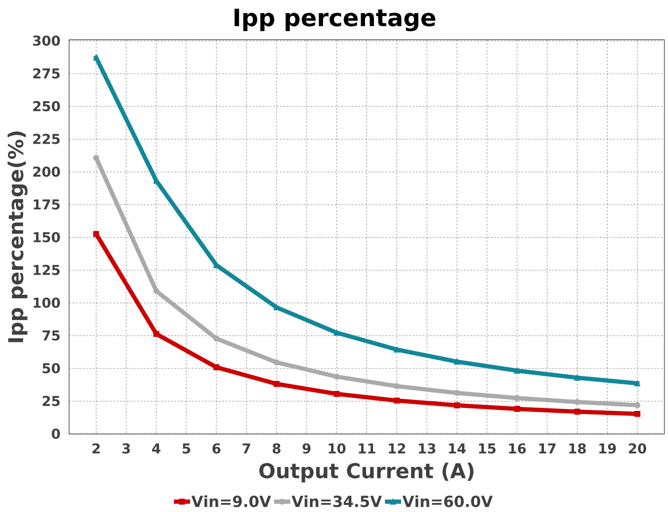
The LM5149-Q1 is qualified for Automotive applications. All passives and other components selected in this design may not be qualified for Automotive applications. The user is required to verify that all components in the design meet the qualification and safety requirements for their specific application.With the design conditions, either the IC or the selected FET junction temperature is exceeded above the maximum rating. Hence, this design is created using an ideal FET. Please note that the resulting FET parameters are ideal, so the efficiency/loss opvals have been disabled. Also, the schematic/PCB export and Thermal simulations will not work with the ideal FET.

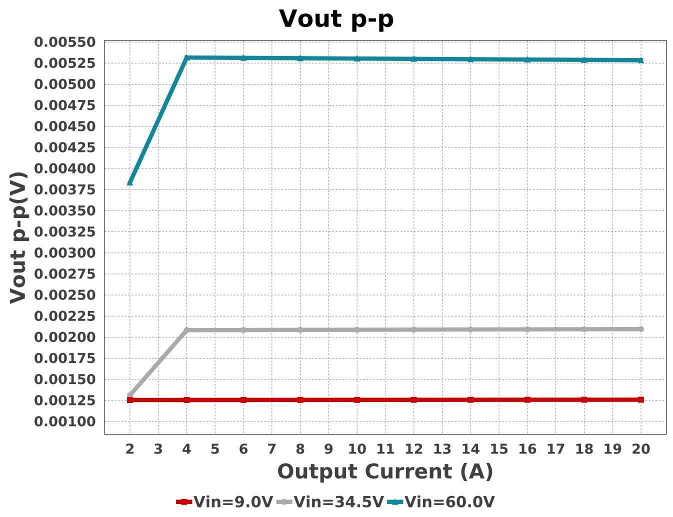
Electrical BOM

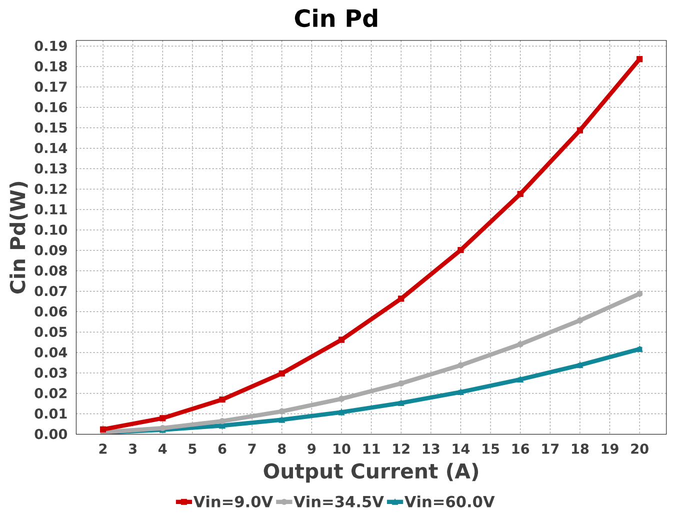
Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
Cboot	MuRata	GRM155R71A104KA01D Series= X7R	Cap= 100.0 nF ESR= 1.0 mOhm VDC= 10.0 V IRMS= 0.0 A	1	$0.01	0402 3 mm^2
Ccomp	Samsung Electro-Mechanics	CL05C821JB5NNNC Series= C0G/NP0	Cap= 820.0 pF VDC= 50.0 V IRMS= 0.0 A	1	$0.01	0402 3 mm^2
Ccomp2	Yageo	CC0805JRNPO9BN180 Series= C0G/NP0	Cap= 18.0 pF VDC= 50.0 V IRMS= 0.0 A	1	$0.01	0805 7 mm^2
Cin	TDK	C3225X7S2A475M200AB Series= X7S	Cap= 4.7 uF ESR= 5.89 mOhm VDC= 100.0 V IRMS= 6.7739 A	3	$0.45	1210 15 mm^2
Cout	MuRata	GRM32EC80J107ME20L Series= X6S	Cap= 100.0 uF ESR= 1.0 mOhm VDC= 6.3 V IRMS= 6.0 A	3	$0.17	1210_270 15 mm^2
Cvcc	MuRata	GRM188R71A225KE15D Series= X7R	Cap= 2.2 uF ESR= 9.0 mOhm VDC= 10.0 V IRMS= 3.3 A	1	$0.02	0603 5 mm^2
Cvdda	MuRata	GRM155R71A104KA01D Series= X7R	Cap= 100.0 nF ESR= 1.0 mOhm VDC= 10.0 V IRMS= 0.0 A	1	$0.01	0402 3 mm^2
D1	Vishay-Semiconductor	BYS12-90-E3/TR	VF@Io= 750.0 mV VRRM= 90.0 V	1	$0.12	SMA 37 mm^2

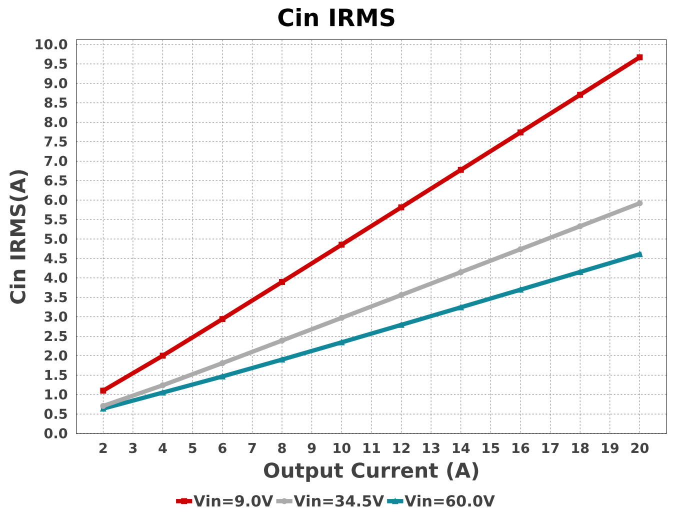
Name	Manufacturer	Part Number	Properties	Qty	Price	Footprint
L1	Vishay-Dale	IHLP5050CEERR33M01	L= 330.0 nH 1.5 mOhm	1	$0.72	 IHLP-5050CE 226 mm²
M1	NA	IdealFET	VdsMax= 160.0 V IdsMax= 28.02 Amps	1	NA	KCS0003B 80 mm²
M2	NA	IdealFET	VdsMax= 160.0 V IdsMax= 28.02 Amps	1	NA	KCS0003B 80 mm²
Rcomp	Vishay-Dale	CRCW040210K7FKED Series= CRCW..e3	Res= 10.7 kOhm Power= 63.0 mW Tolerance= 1.0%	1	$0.01	0402 3 mm²
Rconfig	Vishay-Dale	CRCW060340K2FKEA Series= CRCW..e3	Res= 40.2 kOhm Power= 100.0 mW Tolerance= 1.0%	1	$0.01	0603 5 mm²
Rpg	Vishay-Dale	CRCW0603100KFKEA Series= CRCW..e3	Res= 100.0 kOhm Power= 100.0 mW Tolerance= 1.0%	1	$0.01	0603 5 mm²
Rsense	CUSTOM	CUSTOM Series= ?	Res= 2.08333 mOhm Power= 0.0 W Tolerance= 0.0%	1	NA	CUSTOM 0 mm²
Rt	Yageo	RC0603FR-079K53L Series= ?	Res= 9.53 kOhm Power= 100.0 mW Tolerance= 1.0%	1	$0.01	0603 5 mm²
U1	Texas Instruments	LM5149RGYQ1	Switcher	1	$1.99	RNP0030B 48 mm²

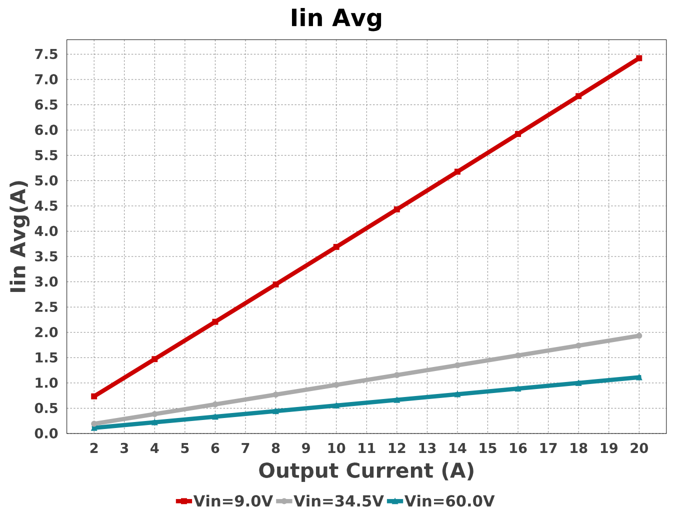


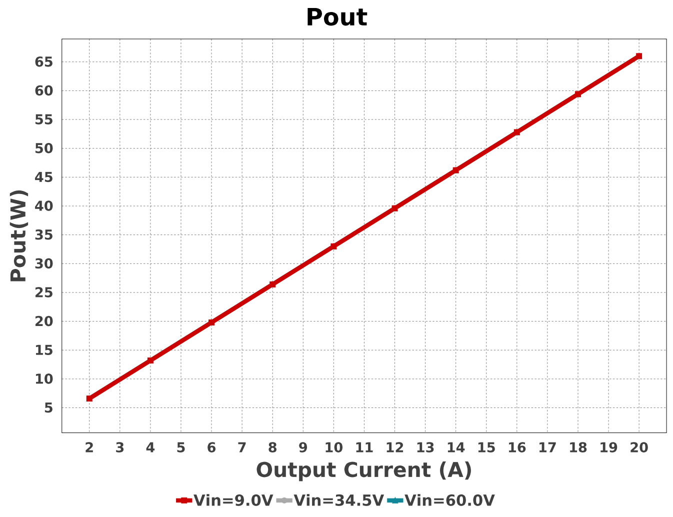


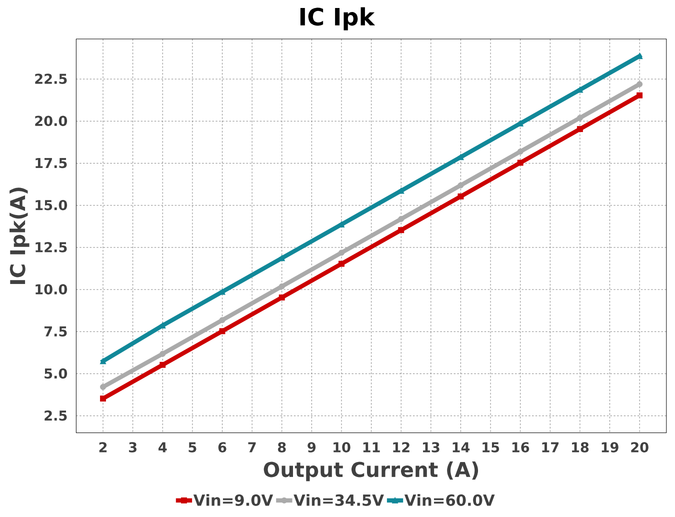

Vout p-p
Vout p-p(V)
0.00550
0.00525
0.00500
0.00475
0.00450
0.00425
0.00400
0.00375
0.00350
0.00325
0.00300
0.00275
0.00250
0.00225
0.00200
0.00175
0.00150
0.00125
0.00100
2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Output Current (A)
Vin=9.0V Vin=34.5V Vin=60.0V

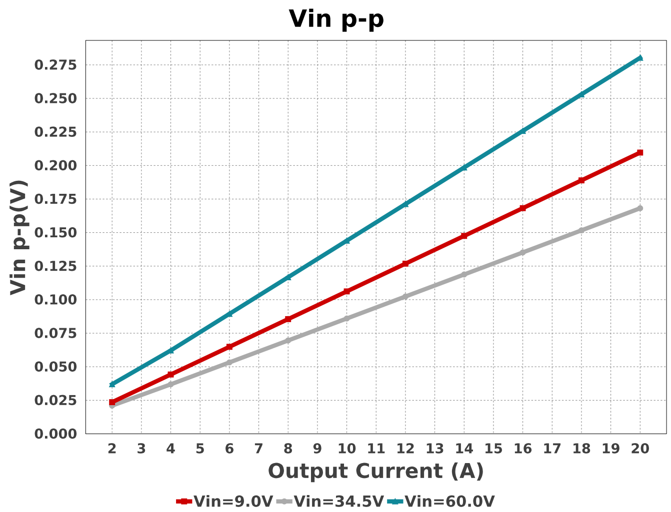

Cin Pd
Cin Pd(W)
0.19
0.18
0.17
0.16
0.15
0.14
0.13
0.12
0.11
0.10
0.09
0.08
0.07
0.06
0.05
0.04
0.03
0.02
0.01
0.00
2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Output Current (A)
Vin=9.0V Vin=34.5V Vin=60.0V

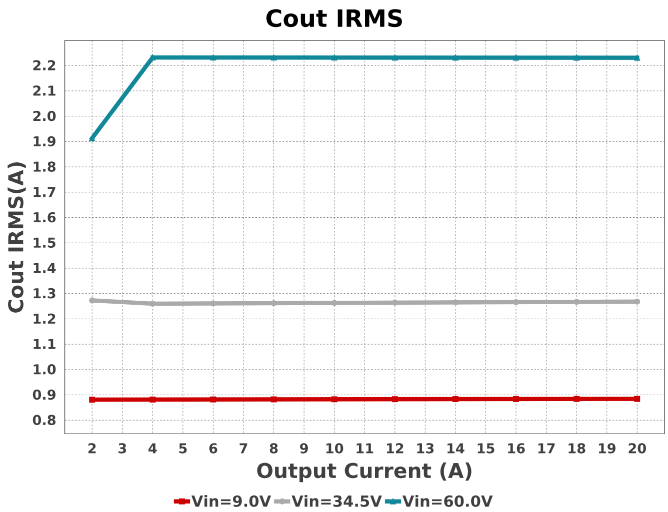

Cin IRMS
Cin IRMS(A)
10.0
9.5
9.0
8.5
8.0
7.5
7.0
6.5
6.0
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Output Current (A)
Vin=9.0V Vin=34.5V Vin=60.0V

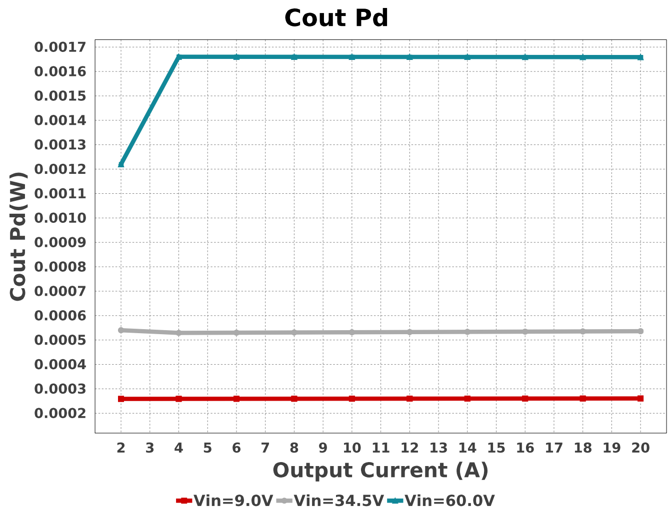

Iin Avg
Iin Avg(A)
7.5
7.0
6.5
6.0
5.5
5.0
4.5
4.0
3.5
3.0
2.5
2.0
1.5
1.0
0.5
0.0
2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Output Current (A)
Vin=9.0V Vin=34.5V Vin=60.0V

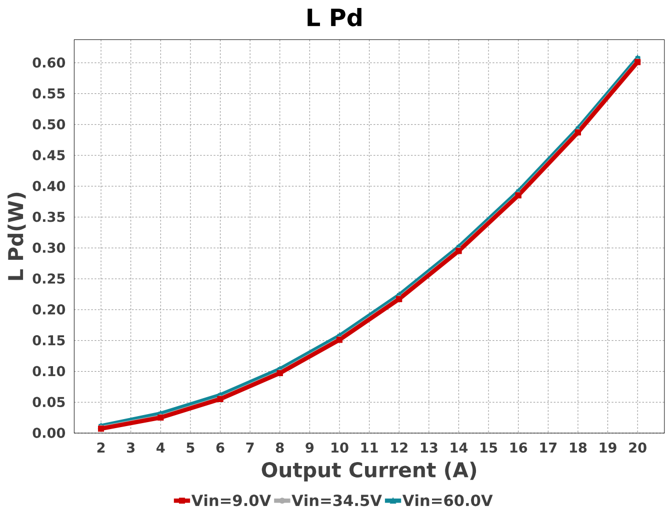

Pout
Pout(W)
65
60
55
50
45
40
35
30
25
20
15
10
5
2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Output Current (A)
Vin=9.0V Vin=34.5V Vin=60.0V

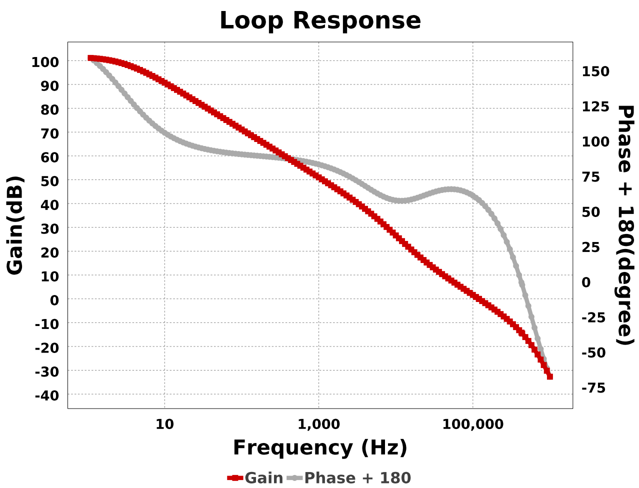

IC Ipk
IC Ipk(A)
22.5
20.0
17.5
15.0
12.5
10.0
7.5
5.0
2.5
2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20
Output Current (A)
Vin=9.0V Vin=34.5V Vin=60.0V











Operating Values

#	Name	Value	Category	Description
1.	Cin IRMS	4.609 A	Capacitor	Input capacitor RMS ripple current
2.	Cin Pd	41.71 mW	Capacitor	Input capacitor power dissipation
3.	Cout IRMS	2.231 A	Capacitor	Output capacitor RMS ripple current
4.	Cout Pd	1.659 mW	Capacitor	Output capacitor power dissipation
5.	IC Ipk	23.864 A	IC	Peak switch current in IC
6.	IC Tolerance	33.0 mV	IC	IC Feedback Tolerance
7.	ICThetaJA Effective	34.8 degC/W	IC	Effective IC Junction-to-Ambient Thermal Resistance
8.	Iin Avg	1.112 A	IC	Average input current
9.	Ipp percentage	38.639 %	Inductor	Inductor ripple current percentage (with respect to average inductor current)
10.	L Ipp	7.728 A	Inductor	Peak-to-peak inductor ripple current

#	Name	Value	Category	Description
11.	L Pd	607.46 mW	Inductor	Inductor power dissipation
12.	Cin Pd	41.71 mW	Power	Input capacitor power dissipation
13.	Cout Pd	1.659 mW	Power	Output capacitor power dissipation
14.	L Pd	607.46 mW	Power	Inductor power dissipation
15.	BOM Count	21	System Information	Total Design BOM count
16.	Cross Freq	119.312 kHz	System Information	Bode plot crossover frequency
17.	FootPrint	602.0 mm^2	System Information	Total Foot Print Area of BOM components
18.	Gain Marg	-14.2 dB	System Information	Bode Plot Gain Margin
19.	Iout	20.0 A	System Information	Iout operating point
20.	Iout transient step used for Cout calculations	10.0 A	System Information	Custom Transient current step requirement that was used for Cout selection (A).
21.	Low Freq Gain	101.138 dB	System Information	Gain at 1Hz
22.	Mode	CCM	System Information	Conduction Mode
23.	Overshoot Value	26.294 mV	System Information	Theoretical Vout Overshoot Value
24.	Phase Marg	58.607 deg	System Information	Bode Plot Phase Margin
25.	Pout	66.0 W	System Information	Total output power
26.	Total BOM	NA	System Information	Total BOM Cost
27.	Undershoot Value	41.824 mV	System Information	Theoretical Vout Undershoot Value
28.	Vin	60.0 V	System Information	Vin operating point
29.	Vin p-p	280.279 mV	System Information	Peak-to-peak input voltage
30.	Vout	3.3 V	System Information	Operational Output Voltage
31.	Vout Ripple requirement used for Cout calculations	1.0 %	System Information	Custom maximum output ripple requirement that was used for Cout selection(% of Vout).
32.	Vout Tolerance	1.0 %	System Information	Vout Tolerance based on IC Tolerance (no load) and voltage divider resistors if applicable
33.	Vout p-p	5.285 mV	System Information	Peak-to-peak output ripple voltage
34.	Vout transient requirement used for Cout calculations	3.0 %	System Information	Custom Transient voltage change requirement that was used for Cout selection (% of Vout).

Design Inputs

Name	Value	Description
Iout	20.0	Maximum Output Current
VinMax	60.0	Maximum input voltage
VinMin	9.0	Minimum input voltage
Vout	3.3	Output Voltage
base_pn	LM5149-Q1	Base Product Number
source	DC	Input Source Type
Ta	85.0	Ambient temperature

WEBENCH® Assembly

Component Testing

Some published data on components in datasheets such as Capacitor ESR and Inductor DC resistance is based on conservative values that will guarantee that the components always exceed the specification. For design purposes it is usually better to work with typical values. Since this data is not always available it is a good practice to measure the Capacitance and ESR values of Cin and Cout, and the inductance and DC resistance of L1 before assembly of the board. Any large discrepancies in values should be electrically simulated in WEBENCH to check for instabilities and thermally simulated in WebTHERM to make sure critical temperatures are not exceeded.

Soldering Component to Board

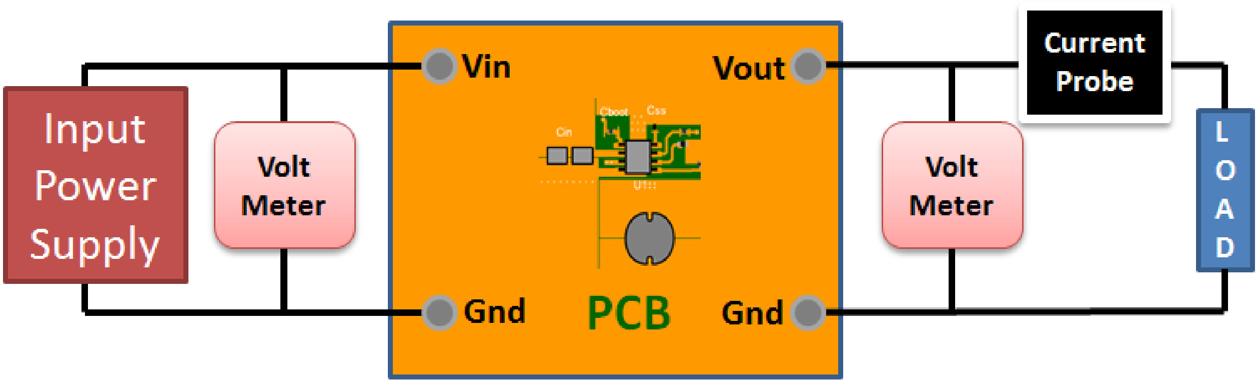
If board assembly is done in house it is best to tack down one terminal of a component on the board then solder the other terminal. For surface mount parts with large tabs, such as the DPAK, the tab on the back of the package should be pre-tinned with solder, then tacked into place by one of the pins. To solder the tab town to the board place the iron down on the board while resting against the tab, heating both surfaces simultaneously. Apply light pressure to the top of the plastic case until the solder flows around the part and the part is flush with the PCB. If the solder is not flowing around the board you may need a higher wattage iron (generally 25W to 30W is enough).

Initial Startup of Circuit

It is best to initially power up the board by setting the input supply voltage to the lowest operating input voltage 9.0V and set the input supply's current limit to zero. With the input supply off connect up the input supply to Vin and GND. Connect a digital volt meter and a load if needed to set the minimum Iout of the design from Vout and GND. Turn on the input supply and slowly turn up the current limit on the input supply.
If the voltage starts to rise on the input supply continue increasing the input supply current limit while watching the output voltage. If the current increases on the input supply, but the voltage remains near zero, then there may be a short or a component misplaced on the board. Power down the board and visually inspect for solder bridges and recheck the diode and capacitor polarities. Once the power supply circuit is operational then more extensive testing may include full load testing, transient load and line tests to compare with simulation results.

Load Testing

The setup is the same as the initial startup, except that an additional digital voltmeter is connected between Vin and GND, a load is connected between Vout and GND and a current meter is connected in series between Vout and the load. The load must be able to handle at least rated output power + 50% (7.5 watts for this design). Ideally the load is supplied in the form of a variable load test unit. It can also be done in the form of suitably large power resistors. When using an oscilloscope to measure waveforms on the prototype board, the ground leads of the oscilloscope probes should be as short as possible and the area of the loop formed by the ground lead should be kept to a minimum. This will help reduce ground lead inductance and eliminate EMI noise that is not actually present in the circuit.



Design Assistance

1. Master key : D97E71332CDFEA55[v1]

2. **LM5149-Q1** Product Folder : http://www.ti.com/product/LM5149%2DQ1 : contains the data sheet and other resources.