



About

= Input Box

TERMS OF USE

Step 1: Operating Specifications

Input Voltage - Min, $V_{IN(min)}$	9 V
Input Voltage - Nom, $V_{IN(nom)}$	14 V
Input Voltage - Max, $V_{IN(max)}$	42 V
Output Voltage, V_{OUT}	28 V
Full Load Output Current, $I_{OUT(max)}$	13 A
Switching Frequency	105 kHz
Frequency Set Resistor, R_T	249 k Ω

Step 2: Filter Inductor

Recommended Filter Inductance	6.6 μ H
Inductance, L_F	4 μ H
Inductor DCR	6 m Ω
Pk-to-Pk Ripple Current at $V_{IN(min)}$, ΔI_L	14.9 A _{pk-ck}
Pk-to-Pk Ripple Current at $V_{IN(nom)}$, ΔI_L	17.0 A _{pk-ck}
Pk-to-Pk Ripple Current at $V_{IN(max)}$, ΔI_L	22.3 A _{pk-ck}
ΔI_L as a % at $V_{IN(min)}$	35 %
ΔI_L as a % at $V_{IN(nom)}$	63 %
ΔI_L as a % at $V_{IN(max)}$	172 %

Step 3: OCP, Sense Resistors, Slope Comp

Required $I_{OCP(MIN)}$ Setpoint at $V_{IN(nom)}$	12 A
Recommended Sense Resistance	3.4 m Ω
Sense Resistance, R_S	6 m Ω
Peak Inductor Current, $I_{L(pk)}$	35.6 A
Power Loss in R_S at Full Load (Min VIN)	7.47 W
Recommended SLOPE Capacitance	180 pF
SLOPE Capacitance, C_{SLOPE}	120 pF
$V_{IN(min)}$	5.9 A
$I_{OUT(typ)}$ at OCP Inception: $V_{IN(nom)}$	8.9 A
$V_{IN(max)}$	24.5 A
Required Const Current Loop Setpoint	N/A A
Output Leg Shunt Resistance, $R_{CS(out)}$	0 m Ω

Step 4: Output Capacitor

Output Voltage Ripple Spec	50 mV _{pk-pk}
Minimum Output Capacitance	1718.1 μ F
Output Capacitance, C_{OUT}	360 μ F
Maximum Permitted ESR	N/A m Ω
Output Capacitor ESR	2 m Ω
Resulting Output Voltage Ripple (max)	265 mV _{pk-pk}
Output Capacitor RMS Current (max)	18.9 A (rms)

Step 5: Input Capacitor

Input Voltage Ripple Spec	180 mV _{pk-pk}
Minimum Input Capacitance	152.3 μ F
Input Capacitance, C_{IN}	180 μ F
Maximum Permitted ESR	1.1 m Ω
Input Capacitor ESR	2 m Ω
Resulting Input Voltage Ripple (max)	201 mV _{pk-pk}
Input Capacitor RMS Current (max)	6.1 A (rms)

Step 6: Soft-start, Dither, UVLO

Soft-Start Time, t_{SS}	16 ms
Soft-Start Capacitance, C_{SS}	100 nF
Modulating Frequency	1 kHz
DITHER Enabled	
DITH Capacitance, C_d	39 nF
Required Input Voltage UVLO On	5.5 V
Input Voltage UVLO Off	4.84 V
Upper UVLO Resistor, R_{UV1}	200 k Ω
Lower UVLO Resistor, R_{UV2}	52.3 k Ω

Step 7: Compensation Design

Load Pole Frequency	1098 Hz
C_{OUT} ESR Zero Frequency	221 kHz
Boost RHP Zero Frequency	21 kHz
Desired Crossover Frequency	8 kHz
Error Amp Pole Frequency	5 Hz
Upper Feedback Resistor, R_{FB1}	100 k Ω
Lower Feedback Resistor, R_{FB2}	2.94 k Ω

Compensation Components

	Calculated / Std Values	Selected	Actual P/Z Frequencies
R_C	28.4	28.7 k Ω	5 Hz (F_{FEA})
C_{C1}	1.4	1.5 nF	3.7 kHz (F_{ZCOMP})
C_{C2}	0	0 pF	219 kHz (F_{PCOMP})

Min COMP Voltage
Max COMP Voltage0.43V
5.4V

Efficiency / Power Loss Analyzer

Step 8: Efficiency

Buck-Leg Power MOSFETs (Q_1 , Q_2) CSD18563Q5A

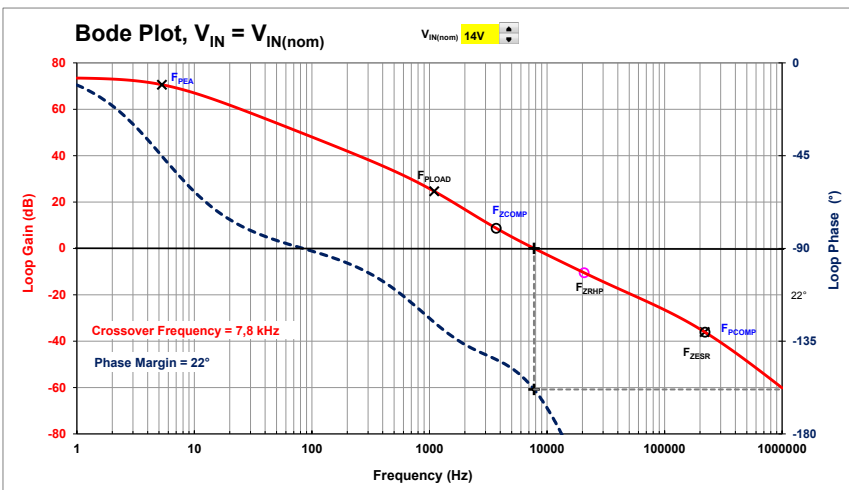
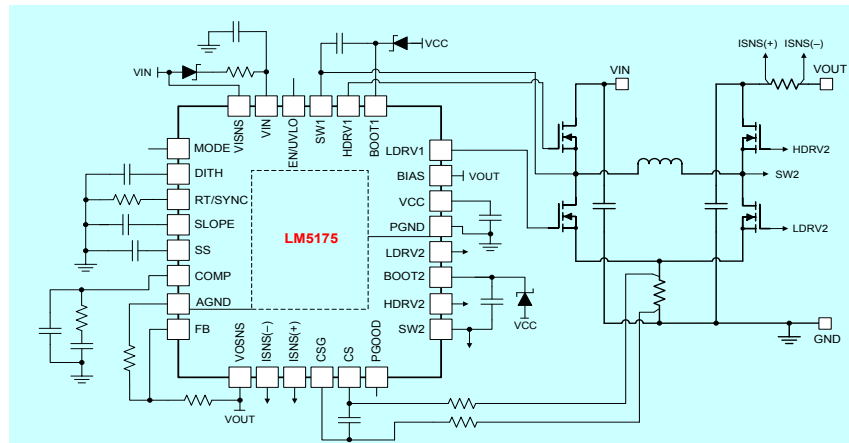
	Hi-side	Low-side
On-State Resistance, $R_{DS(on)}$	5.7	5.7 m Ω
Total Gate Charge, Q_G	11	11 nC
Gate-Drain Charge, Q_{GD}	2.9	2.9 nC
Gate-Source Charge, Q_{GS}	3.3	3.3 nC
Gate Resistance, R_G	1.5	1.5 Ω
Transconductance, g_{FS}	60	60 S
Gate-Source Threshold Voltage, V_{TH}	4	4 V
Body Diode Forward Voltage, V_{SD}	0.8	0.8 V
Body Diode Rev Recovery Charge, Q_{RR}		63 nC
Thermal Resistance, θ_{JA}	50	50 $^{\circ}$ C/W

Boost-Leg Power MOSFETs (Q_3 , Q_4) CSD16321Q5

	Hi-side	Low-side
On-State Resistance, $R_{DS(on)}$	1.9	1.9 m Ω
Total Gate Charge, Q_G	22	22 nC
Gate-Drain Charge, Q_{GD}	2.5	2.5 nC
Gate-Source Charge, Q_{GS}	4	4 nC
Gate Resistance, R_G	1.5	1.5 Ω
Transconductance, g_{FS}	150	150 S
Gate-Source Threshold Voltage, V_{TH}	2	2 V
Body Diode Forward Voltage, V_{SD}	0.8	0.8 V
Body Diode Rev Recovery Charge, Q_{RR}	33	33 nC
Thermal Resistance, θ_{JA}	50	50 $^{\circ}$ C/W

External Schottky Diode (if applicable) Buck Leg Boost Leg

Schottky Fwd Voltage, V_{FSDsch}	0	0 V
Schottky Rev Recovery Charge, Q_{RRsch}	0	0 nC



Efficiency vs IOUT Plot

