



About

 = Input Box

TERMS OF USE

Step 1: Operating Specifications

Input Voltage - Min, $V_{IN(min)}$	10 V
Input Voltage - Nom, $V_{IN(nom)}$	13 V
Input Voltage - Max, $V_{IN(max)}$	15 V
Output Voltage, V_{OUT}	12 V
Full Load Output Current, $I_{OUT(max)}$	4 A
Switching Frequency	400 kHz
Frequency Set Resistor, R_T	61.9 k Ω

Step 2: Filter Inductor

Recommended Filter Inductance	2.3 μ H
Inductance, L_F	2.2 μ H
Inductor DCR	17 m Ω
PK-to-PK Ripple Current at $V_{IN(min)}$, ΔI_{L1}	2.0 A _{pk-pk}
PK-to-PK Ripple Current at $V_{IN(nom)}$, ΔI_{L2}	1.1 A _{pk-pk}
PK-to-PK Ripple Current at $V_{IN(max)}$, ΔI_{L3}	2.7 A _{pk-pk}
ΔI_L as a % at $V_{IN(min)}$	40 %
ΔI_L as a % at $V_{IN(nom)}$	26 %
ΔI_L as a % at $V_{IN(max)}$	69 %

Step 3: OCP, Sense Resistors, Slope Comp

Required $I_{OCP(MIN)}$ Setpoint at $V_{IN(nom)}$	5 A
Recommended Sense Resistance	17.9 m Ω
Sense Resistance, R_S	18 m Ω
Peak Inductor Current, $I_{L(pk)}$	8.9 A
Power Loss in R_S at Full Load (Min VIN)	0.08 W
Recommended SLOPE Capacitance	33 pF
SLOPE Capacitance, C_{SLOPE}	33 pF
$V_{IN(min)}$	6.5 A
$I_{OUT(tp)}$ at OCP Inception: $V_{IN(nom)}$	5.0 A
$V_{IN(nom)}$	5.8 A
$V_{IN(max)}$	5.8 A
Required Const Current Loop Setpoint	N/A A
Output Leg Shunt Resistance, $R_{CS(OUT)}$	0 m Ω

Step 4: Output Capacitor

Output Voltage Ripple Spec	120 mV _{pk-pk}
Minimum Output Capacitance	22.0 μ F
Output Capacitance, C_{OUT}	89 μ F
Maximum Permitted ESR	25.0 m Ω
Output Capacitor ESR	4 m Ω
Resulting Output Voltage Ripple (max)	36 mV _{pk-pk}
Output Capacitor RMS Current (max)	1.8 A (rms)

Step 5: Input Capacitor

Input Voltage Ripple Spec	180 mV _{pk-pk}
Minimum Input Capacitance	10.0 μ F
Input Capacitance, C_{IN}	22 μ F
Maximum Permitted ESR	20.2 m Ω
Input Capacitor ESR	4 m Ω
Resulting Input Voltage Ripple (max)	93 mV _{pk-pk}
Input Capacitor RMS Current (max)	1.6 A (rms)

Step 6: Soft-start, Dither, UVLO

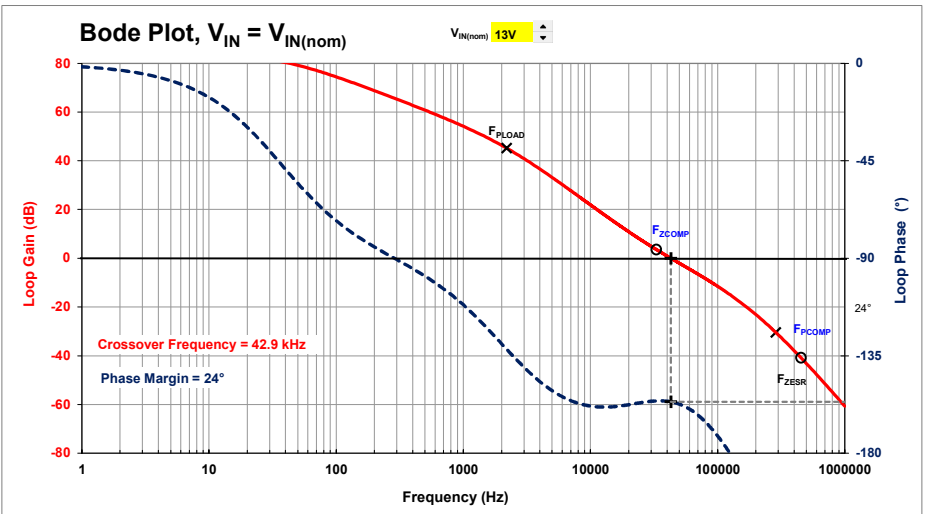
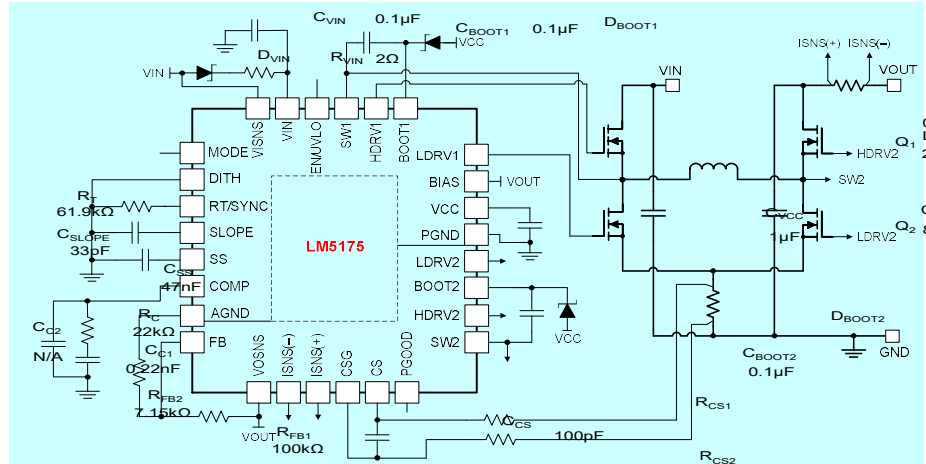
Soft-Start Time, t_{SS}	8 ms
Soft-Start Capacitance, C_{SS}	47 nF
DITHER Disabled	
*Short DITH pin to GND	
Required Input Voltage UVLO On	5.5 V
Input Voltage UVLO Off	4.84 V
Upper UVLO Resistor, R_{UV1}	200 k Ω
Lower UVLO Resistor, R_{UV2}	52.3 k Ω

Step 7: Compensation Design

Load Pole Frequency	2191 Hz
C_{OUT} ESR Zero Frequency	452 kHz
Boost RHP Zero Frequency	1 kHz
Desired Crossover Frequency	50 kHz
Error Amp Pole Frequency	36 Hz
Upper Feedback Resistor, R_{FB1}	100 k Ω
Lower Feedback Resistor, R_{FB2}	7.15 k Ω

Compensation Components

Calculated / Std Values	Selected	Actual P/Z Frequencies
R_C 29.4 / 29.4	22 k Ω	36 Hz (F_{FEA})
C_{C1} 0.2 / 0.22	0.22 nF	32.9 kHz (F_{ZCOMP})
C_{C2} 0 / 0	0 pF	286 kHz (F_{PCOMP})



Efficiency / Power Loss Analyzer

Step 8: Efficiency

Buck-Leg Power MOSFETs (Q_1, Q_2) BSC0702LS

	Hi-side	Low-side
On-State Resistance, $R_{DS(on)}$	2.7 m Ω	2.7 m Ω
Total Gate Charge, Q_G	24 nC	24 nC
Gate-Drain Charge, Q_{GD}	8 nC	8 nC
Gate-Source Charge, Q_{GS}	10 nC	10 nC
Gate Resistance, R_G	1.3 Ω	1.3 Ω
Transconductance, g_{FS}	120 S	120 S
Gate-Source Threshold Voltage, V_{TH}	1.7 V	1.7 V
Body Diode Forward Voltage, V_{BD}	0.8 V	0.8 V
Body Diode Rev Recovery Charge, Q_{RR}	36 nC	36 nC
Thermal Resistance, θ_{JA}	50 $^{\circ}$ C/W	50 $^{\circ}$ C/W

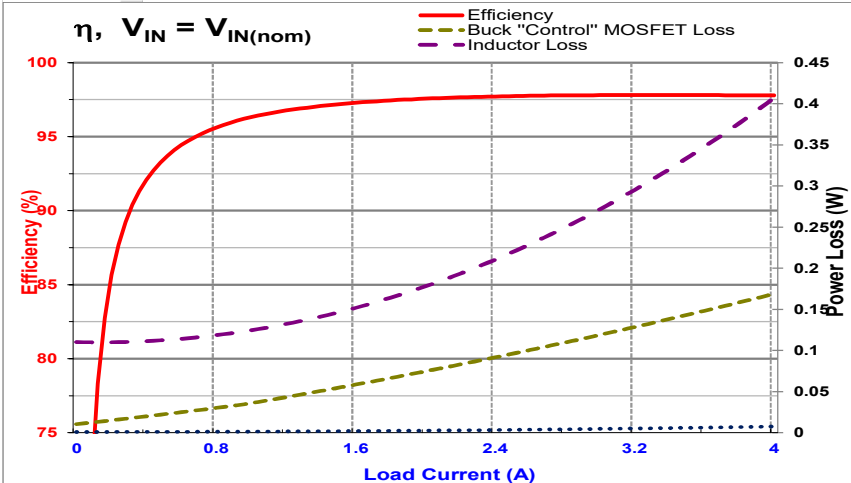
Boost-Leg Power MOSFETs (Q_3, Q_4) RU3040M2

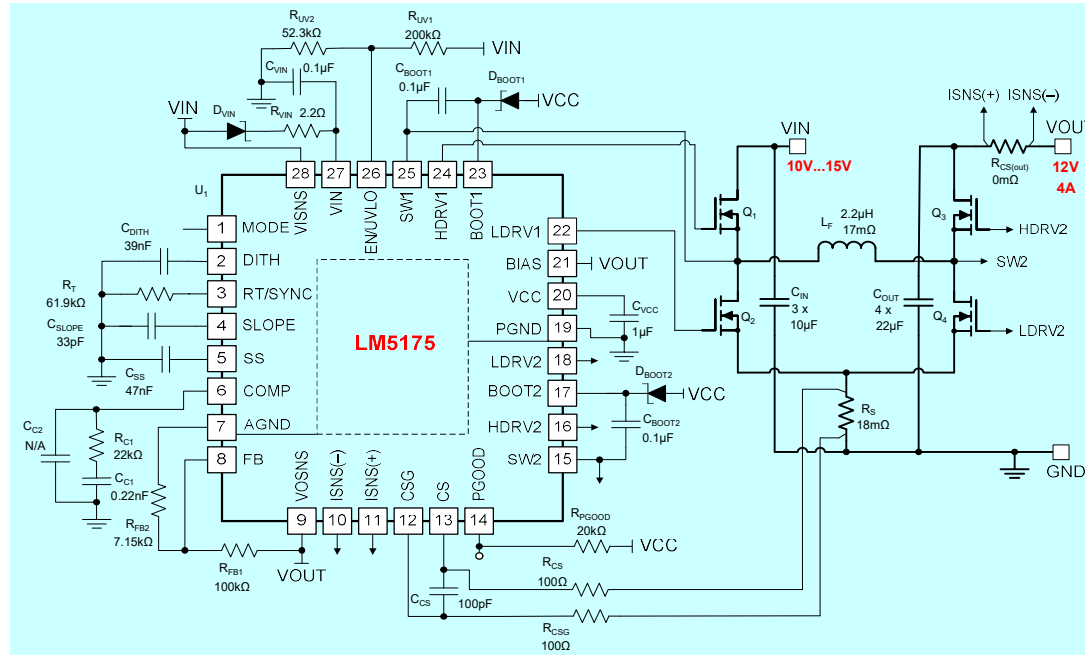
	Hi-side	Low-side
On-State Resistance, $R_{DS(on)}$	5.8 m Ω	8.2 m Ω
Total Gate Charge, Q_G	13 nC	13 nC
Gate-Drain Charge, Q_{GD}	5.5 nC	5.5 nC
Gate-Source Charge, Q_{GS}	3.8 nC	3.8 nC
Gate Resistance, R_G	1 Ω	1 Ω
Transconductance, g_{FS}	125 S	125 S
Gate-Source Threshold Voltage, V_{TH}	1.8 V	1.8 V
Body Diode Forward Voltage, V_{BD}	1.2 V	1.2 V
Body Diode Rev Recovery Charge, Q_{RR}	9 nC	9 nC
Thermal Resistance, θ_{JA}	35 $^{\circ}$ C/W	35 $^{\circ}$ C/W

External Schottky Diode (if applicable) Buck Leg Boost Leg

Schottky Fwd Voltage, V_{FWDsch}	0.35 V	0.35 V
Schottky Rev Recovery Charge, Q_{RRsch}	0.6 nC	0.6 nC

Efficiency vs IOUT Plot





** Tie MODE to VCC (or voltage > 2.4V) for CCM, GND for DCM **

VIN = 10 V to 15 V, VOUT = 12 V, IOUT = 4 A, Fsw = 400 kHz, Current Limit = 5 A

High Efficiency Synchronous Buck-Boost Regulator BOM

Count	Ref Des	Value	Description	Size	Part Number	MFR
2	C _{BOOT1} , C _{BOOT2}	0.1µF	Capacitor, Ceramic, 0.1-µF, 50V, X7R, 20%	0603	Std	Std
1	C _{C1}	0.22nF	Capacitor, Ceramic, 0.22-nF, 16V, X7R, 10%	0603	Std	Std
1	C _{C2}	0pF	Capacitor, Ceramic, 0-pF, 50V, NP0, 5%	0603	Std	Std
1	C _{SLOPE}	33pF	Capacitor, Ceramic, 33-pF, 50V, NP0, 5%	0603	Std	Std
1	C _{CS}	100pF	Capacitor, Ceramic, 100-pF, 16V, X7R, 10%	0603	Std	Std
1	C _{DITH}	39nF	Capacitor, Ceramic, 39-nF, 16V, X7R, 10%	0603	Std	Std
3	C _{IN}	10µF	Capacitor, Ceramic, 10-µF, 50V, X7R, 20%	1210	Std	Std
4	C _{OUT}	22µF	Capacitor, Ceramic, 22-µF, 25V, X5R, 20%	1210	Std	Std
1	C _{SS}	47nF	Capacitor, Ceramic, 47-nF, 16V, X7R, 10%	0603	Std	Std
1	C _{VCC}	1µF	Capacitor, Ceramic, 1-µF, 25V, X7R, 20%	0603	Std	Std
1	C _{VIN}	0.1µF	Capacitor, Ceramic, 0.1-µF, 100V, X7R, 20%	0603	Std	Std
3	D _{BOOT1} , D _{BOOT2} , D _{VIN}	See description	Schottky Diode, 200mA	-	-	Various
1	L _F	2.2µH	Inductor, 2.2µH, 17mΩ, >10A	-	-	Various
2	Q ₁ , Q ₂	See description	MOSFET, N-CH, 60V, 2.7mΩ	Std	BSC0702LS	-
2	Q ₃ , Q ₄	See description	MOSFET, N-CH, 60V, 5.8mΩ	Std	RU3040M2	-
1	R _{C1}	22k	Resistor, Chip, 22-kΩ, 1/16W, 1%	0603	Std	Std
1	R _S	18m	Resistor, Chip, 18-mΩ, 2W, 1%	2512	Std	Std
1	R _{CS(out)}	0m	Resistor, Chip, 0-mΩ, 2W, 1%	2512	Std	Std
1	R _T	61.9k	Resistor, Chip, 61.9-kΩ, 1/16W, 1%	0603	Std	Std
1	R _{FB1}	100k	Resistor, Chip, 100-kΩ, 1/16W, 1%	0603	Std	Std
1	R _{FB2}	7.15k	Resistor, Chip, 7.15-kΩ, 1/16W, 1%	0603	Std	Std
1	R _{PGOOD}	20k	Resistor, Chip, 20-kΩ, 1/16W, 1%	0603	Std	Std
2	R _{CS} , R _{CSG}	100	Resistor, Chip, 100-Ω, 1/16W, 1%	0603	Std	Std
1	R _{UV1}	200k	Resistor, Chip, 200-kΩ, 1/16W, 1%	0603	Std	Std
1	R _{UV2}	52.3k	Resistor, Chip, 52.3-kΩ, 1/16W, 1%	0603	Std	Std
1	R _{VIN}	2.2	Resistor, Chip, 2.2-Ω, 1/16W, 1%	0603	Std	Std
1	U ₁	LM5175	IC, LM5175, Buck-Boost PWM Controller, 3.5V-42V Input	QFN-28 TSSOP-28	LM5175RHF LM5175PWP	TI

NOTES:

** For information on TI NexFET™ MOSFETs, see ** <http://www.ti.com/nexfet> **

** Inductor saturation current should be higher than the peak inductor current at the OCP setpoint for all input voltages and operating temperatures **

** Effective input and output capacitances should be appropriately derated for applied voltage and temperature, particularly with ceramics **