



About

 = Input Box

V 1.0.1 October 2022

Step 1: Operating Specifications

Input Voltage - Min, $V_{IN(min)}$	12 V
Input Voltage - Nom, $V_{IN(nom)}$	20 V
Input Voltage - Max, $V_{IN(max)}$	24 V
Output Voltage, V_{OUT}	21 V
Full Load Output Current, $I_{OUT(max)}$	1.8 A
Switching Frequency	520 kHz
Frequency Set Resistor, R_T	15 kΩ

Step 2: Filter Inductor

Recommended Filter Inductance	6.5 μH
Inductance, L_F	6.8 μH
Inductor DCR	18.5 mΩ
PK-to-PK Ripple Current at $V_{IN(min)}$, ΔI_{L1}	1.5 A _{pk-pk}
PK-to-PK Ripple Current at $V_{IN(nom)}$, ΔI_{L2}	0.3 A _{pk-pk}
PK-to-PK Ripple Current at $V_{IN(max)}$, ΔI_{L3}	0.7 A _{pk-pk}
ΔI_L as a % at $V_{IN(min)}$	42 %
ΔI_L as a % at $V_{IN(nom)}$	13 %
ΔI_L as a % at $V_{IN(max)}$	41 %

Step 3: OCP, Sense Resistors, Slope Comp

Required $I_{OCP(MIN)}$ Setpoint at $V_{IN(nom)}$	2.2 A
Recommended Sense Resistance	23.9 mΩ
Sense Resistance, R_S	24 mΩ
Peak Inductor Current, $I_{L(PK)}$	5.0 A
Power Loss in R_S at Full Load (Min V_{IN})	0.13 W
Recommended SLOPE Capacitance	120 pF
SLOPE Capacitance, C_{SLOPE}	120 pF
$V_{IN(min)}$	2.4 A
$I_{OUT(typ)}$ at OCP Inception: $V_{IN(nom)}$	3.0 A
$V_{IN(max)}$	3.7 A
Set Const Current Loop Setpoint (?)	1.8 A
Output Leg Shunt Resistance, $R_{CS(out)}$	28 mΩ

Step 4: Output Capacitor

Output Voltage Ripple Spec	100 mV _{pk-pk}
Minimum Output Capacitance	22.0 μF
Output Capacitance, C_{OUT}	170 μF
Maximum Permitted ESR	50.7 mΩ
Output Capacitor ESR	28 mΩ
Resulting Output Voltage Ripple (max)	59 mV _{pk-pk}
Output Capacitor RMS Current (max)	1.6 A (rms)

Step 5: Input Capacitor

Input Voltage Ripple Spec	200 mV _{pk-pk}
Minimum Input Capacitance	10.0 μF
Input Capacitance, C_{IN}	40 μF
Maximum Permitted ESR	87.8 mΩ
Input Capacitor ESR	0.1 mΩ
Resulting Input Voltage Ripple (max)	10 mV _{pk-pk}
Input Capacitor RMS Current (max)	0.6 A (rms)

Step 6: Soft-start, Dither, UVLO

Soft-Start Time, t_{SS}	50 ms
Soft-Start Capacitance, C_{SS}	330 nF
DITHER Disabled	☐
*Short DITH pin to GND	
Required Input Voltage UVLO On	10 V
Input Voltage UVLO Off	9.14 V
Upper UVLO Resistor, R_{UV1}	250 kΩ
Lower UVLO Resistor, R_{UV2}	33.2 kΩ

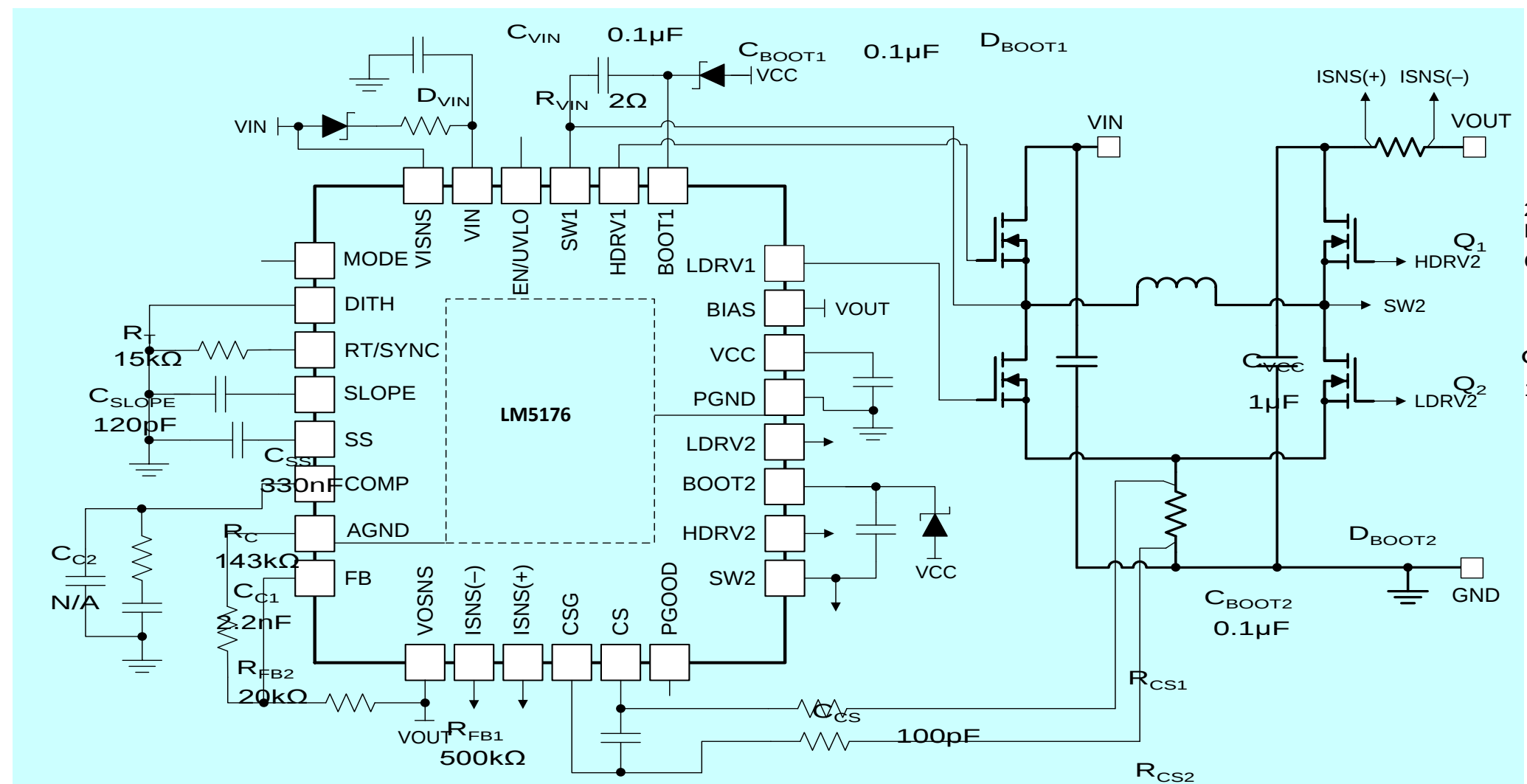
Step 7: Compensation Design

Load Pole Frequency	307 Hz
C_{OUT} ESR Zero Frequency	33 kHz
Boost RHP Zero Frequency	247 kHz
Desired Crossover Frequency	52 kHz
Error Amp Pole Frequency	4 Hz
Upper Feedback Resistor, R_{FB1}	500 kΩ
Lower Feedback Resistor, R_{FB2}	20 kΩ

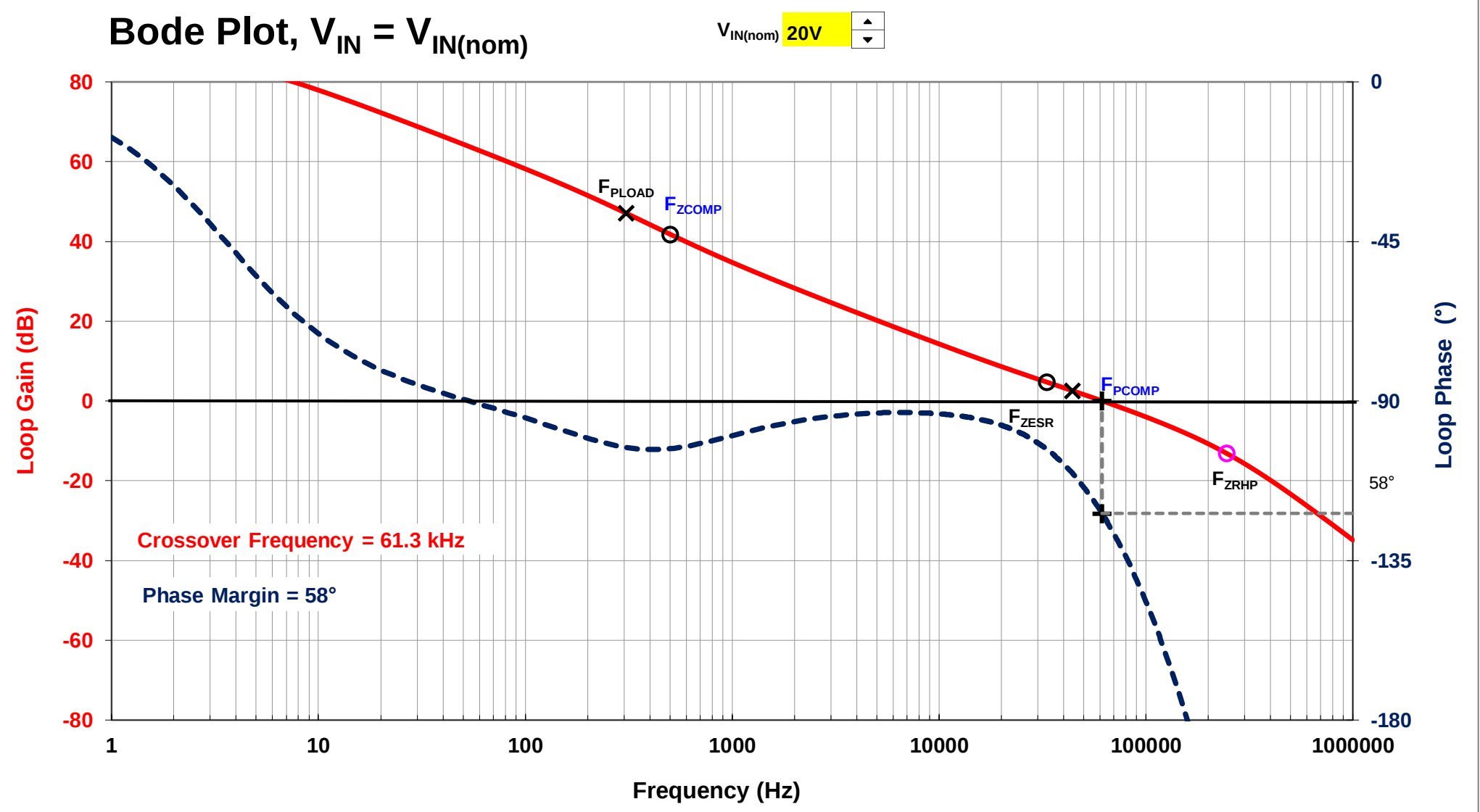
Compensation Components

	Calculated / Std Values	Selected	Actual P/Z Frequencies
R_C	141.8 143	143 kΩ	4 Hz (F_{PEA})
C_{C1}	2.4 2.2	2.2 nF	0.5 kHz (F_{ZCOMP})
C_{C2}	0 0	0 pF	44 kHz (F_{PCOMP})

Min COMP Voltage 1.54V
Max COMP Voltage 2.26V



Bode Plot, $V_{IN} = V_{IN(nom)}$



Efficiency / Power Loss Analyzer

Step 8: Efficiency

Buck-Leg Power MOSFETs (Q_1, Q_2) CSD18563Q5A

	Hi-side	Low-side
On-State Resistance, $R_{DS(on)}$	16.0	16.0 mΩ
Total Gate Charge, Q_G	13.2	13.2 nC
Gate-Drain Charge, Q_{GD}	1.8	1.8 nC
Gate-Source Charge, Q_{GS}	2.2	2.2 nC
Gate Resistance, R_G	1.47	1.47 Ω
Transconductance, g_{FS}	8.3	8.3 S
Gate-Source Threshold Voltage, V_{TH}	1.7	1.7 V
Body Diode Forward Voltage, V_{BD}	1.2	1.2 V
Body Diode Rev Recovery Charge, Q_{RR}		7.9 nC
Thermal Resistance, θ_{JA}	50	50 °C/W

Boost-Leg Power MOSFETs (Q_3, Q_4) CSD16321Q5

	Hi-side	Low-side
On-State Resistance, $R_{DS(on)}$	16	16 mΩ
Total Gate Charge, Q_G	13.2	13.2 nC
Gate-Drain Charge, Q_{GD}	1.8	1.8 nC
Gate-Source Charge, Q_{GS}	2.2	2.2 nC
Gate Resistance, R_G	1.47	1.47 Ω
Transconductance, g_{FS}	8.3	8.3 S
Gate-Source Threshold Voltage, V_{TH}	1.7	1.7 V
Body Diode Forward Voltage, V_{BD}	1.2	1.2 V
Body Diode Rev Recovery Charge, Q_{RR}		7.9 nC
Thermal Resistance, θ_{JA}	50	50 °C/W

External Schottky Diode (if applicable)

	Buck Leg	Boost Leg
Schottky Fwd Voltage, V_{FWDsch}	0	0 V
Schottky Rev Recovery Charge, Q_{RRsch}	0	0 nC

