WIDE V_{IN} DC/DC Power Solutions
Reliable Power for Demanding Systems

LM5177 DC/DC Controller Design Tool

About
Version 1.0.9

= Input Box

http://www.ti.com/product/lm5177

TERMS OF USE

Step 1: Operating Specifications

Input Voltage - Min, $V_{IN(min)}$	**9**	**V**
Input Voltage - Nom, $V_{IN(nom)}$	**12**	**V**
Input Voltage - Max, $V_{IN(max)}$	**50**	**V**
Output Voltage, V_{OUT}	**20.5**	**V**
Full Load Output Current, $I_{OUT(max)}$	**6**	**A**
Switching Frequency	**120**	**kHz**
Frequency Set Resistor, R_T	249	kΩ

Step 2: Filter Inductor

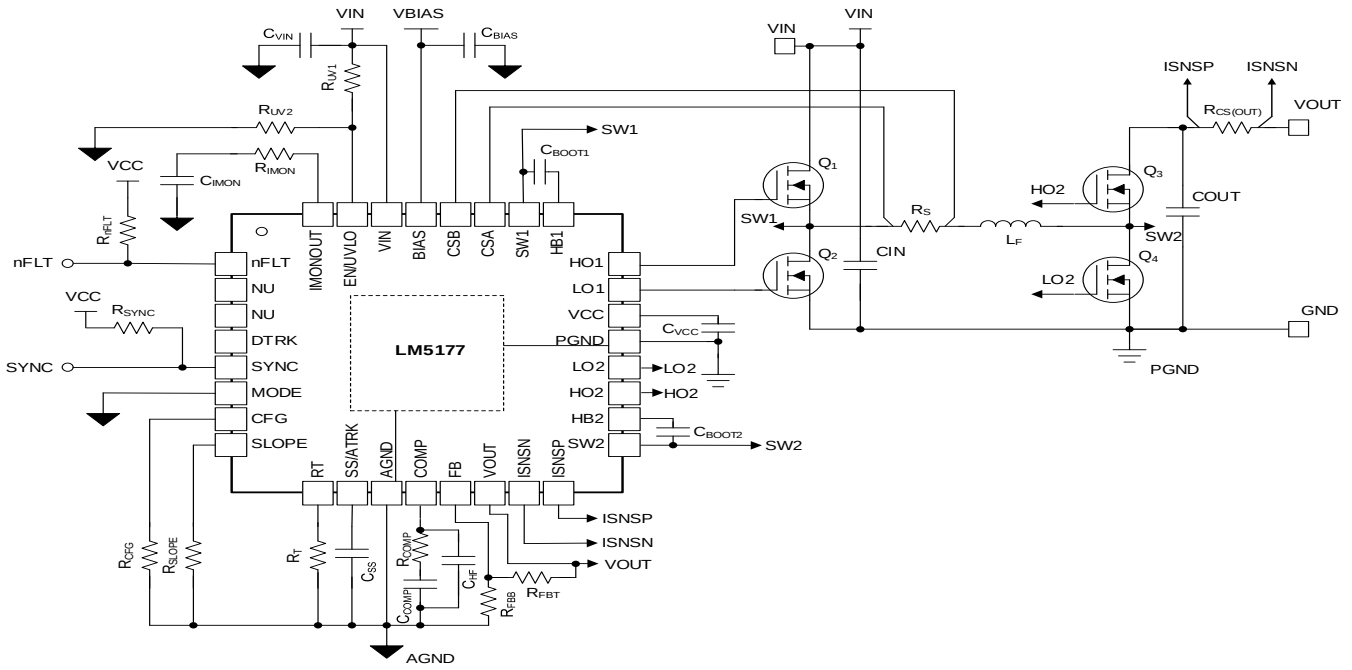
Recommended Filter Inductance	10.8	µH
Inductance, L_F	**10**	**µH**
Inductor DCR	**1.9**	**mΩ**
Pk-to-Pk Ripple Current at $V_{IN(min)}$, ΔI_{L1}	4.2	A_{pk-pk}
Pk-to-Pk Ripple Current at $V_{IN(nom)}$, ΔI_{L2}	4.2	A_{pk-pk}
Pk-to-Pk Ripple Current at $V_{IN(max)}$, ΔI_{L3}	10.1	A_{pk-pk}
ΔI_L as a % at $V_{IN(min)}$	29	%
ΔI_L as a % at $V_{IN(nom)}$	39	%
ΔI_L as a % at $V_{IN(max)}$	168	%

Step 3: OCP, Sense Resistors, Slope Comp

Peak Current Limit Margin	20	%
Recommended Sense Resistance	1.9	mΩ
Sense Resistance, R_S	**1.8**	**mΩ**
Peak Inductor Over Current Limit, $I_{LPK,Limit}$	32.5	A
Max Peak Inductor Current, $I_{LPk,Max}$	16.5	A
Power Loss in Rs at over current limit	0.78	W
Recommended SLOPE Resistor	**280**	**kΩ**
SLOPE Resistor, R_{SLOPE}	**280**	**kΩ**
$I_{OUT(typ)}$ at OCP Inception: $V_{IN(min)}$	11.2	A
$V_{IN(nom)}$	15.0	A
$V_{IN(max)}$	22.7	A

Step 4: Output Capacitor

Output Voltage Ripple Spec	**150**	**mV_{pk-pk}**
Minimum Output Capacitance	187.7	µF
Output Capacitance, C_{OUT}	**250**	**µF**
Maximum Permitted ESR	6.2	mΩ
Output Capacitor ESR	**6**	**mΩ**
Resulting Output Voltage Ripple (max)	149	mV_{pk-pk}
Output Capacitor RMS Current (max)	6.8	A (rms)



Step 5: Input Capacitor

Input Voltage Ripple Spec	**180**	**mV_{pk-pk}**
Minimum Input Capacitance	69.4	µF
Input Capacitance, C_{IN}	**300**	**µF**
Maximum Permitted ESR	12.5	mΩ
Input Capacitor ESR	**10**	**mΩ**
Resulting Input Voltage Ripple (max)	152	mV_{pk-pk}
Input Capacitor RMS Current (max)	3.0	A (rms)

Step 6: Soft-start, UVLO, CFG

recommended Soft-Start Time, t_{SS} for $I_{SCP(MIN)}$	0.4	ms
Soft-Start Time, t_{SS}	**3**	**ms**
Soft-Start Capacitance, C_{SS}	33	nF

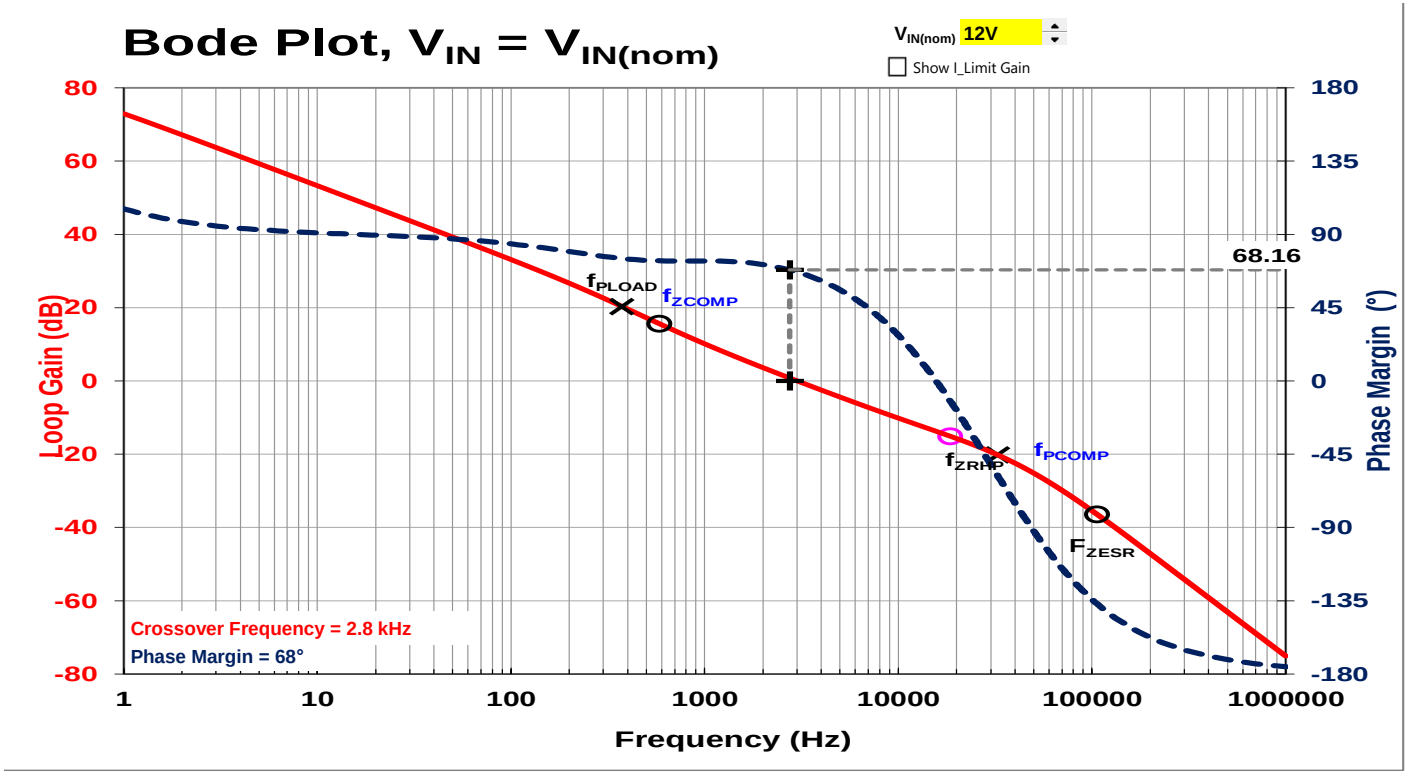
DRSS: off | HICCUP: off | uSleep: on | ILIMIT: positive

Configuration Setting	**13**	
Configuration Resistor on CFG: R_{CFG}	20.5	kΩ
Required Input Voltage UVLO On	**9**	**V**
Input Voltage UVLO Off	**8.5**	**V**
Upper UVLO Resistor, R_{UV1}	100	kΩ
Lower UVLO Resistor, R_{UV2}	15.8	kΩ

Current Monitor/Limiter		
Average Current Limit	**6**	**A**
Current Sense Shunt Resistance, $R_{CS(out/in)}$	8	mΩ
SYNC pin during startup	High	
IMONOUT Filter , C_{IMON}	**3**	nF
IMONOUT Filter , R_{IMON}	**1**	kΩ

Step 7: Compensation Design

Load Pole Frequency	373	Hz
C_{OUT} ESR Zero Frequency	106	kHz
Boost RHP Zero Frequency @ $V_{IN(MIN)}$	10	kHz
Boost RHP Zero Frequency @ $V_{IN(NOM)}$	19	kHz
Desired Crossover Frequency	**3**	**kHz**
Error Amp Pole Frequency	0	Hz
Upper Feedback Resistor, R_{FBT}	**71.5**	**kΩ**
Lower Feedback Resistor, R_{FBB}	3.65	kΩ



Compensation Components

	Calculated / Std Values		Selected	Actual P/Z Frequencies
R_C	4.9	4.87	**4.87 kΩ**	0 Hz (F_{PEA})
C_{C1}	58.1	56	**56 nF**	0.6 kHz (F_{ZCOMP})
C_{C2}	1076	1000	**1000 pF**	32 kHz (F_{PCOMP})

Efficiency / Power Loss Analyzer

Step 8: Efficiency

Buck-Leg Power MOSFETs (Q_1, Q_2)	SQJ422EP		
	Hi-side	Low-side	
On-State Resistance, $R_{DS(on)}$	1.5	1.5	mΩ
Total Gate Charge, Q_G	100	100	nC
Gate-Drain Charge, Q_{GD}	10	10	nC
Gate-Source Charge, Q_{GS}	15	15	nC
Gate Resistance, R_G	1	1	Ω
Transconductance, g_{FS}	140	140	S
Gate-Source Threshold Voltage, V_{TH}	2.5	2.5	V
Body Diode Forward Voltage, V_{BD}	1	1	V
Body Diode Rev Recovery Charge, Q_{RR}		120	nC
Thermal Resistance, θ_{JA}	20	20	°C/W

Boost-Leg Power MOSFETs (Q_3, Q_4)	SQJ422EP		
	Hi-side	Low-side	
On-State Resistance, $R_{DS(on)}$	1.5	1.5	mΩ
Total Gate Charge, Q_G	100	100	nC
Gate-Drain Charge, Q_{GD}	10	10	nC
Gate-Source Charge, Q_{GS}	15	15	nC
Gate Resistance, R_G	1	1	Ω
Transconductance, g_{FS}	140	140	S
Gate-Source Threshold Voltage, V_{TH}	2.5	2.5	V
Body Diode Forward Voltage, V_{BD}	1	1	V
Body Diode Rev Recovery Charge, Q_{RR}	120		nC
Thermal Resistance, θ_{JA}	20	20	°C/W

External Schottky Diode (if applicable)	*Buck* Leg	*Boost* Leg	
Schottky Fwd Voltage, V_{FWDsch}	0	0	V
Schottky Rev Recovery Charge, Q_{RRsch}	0	0	nC