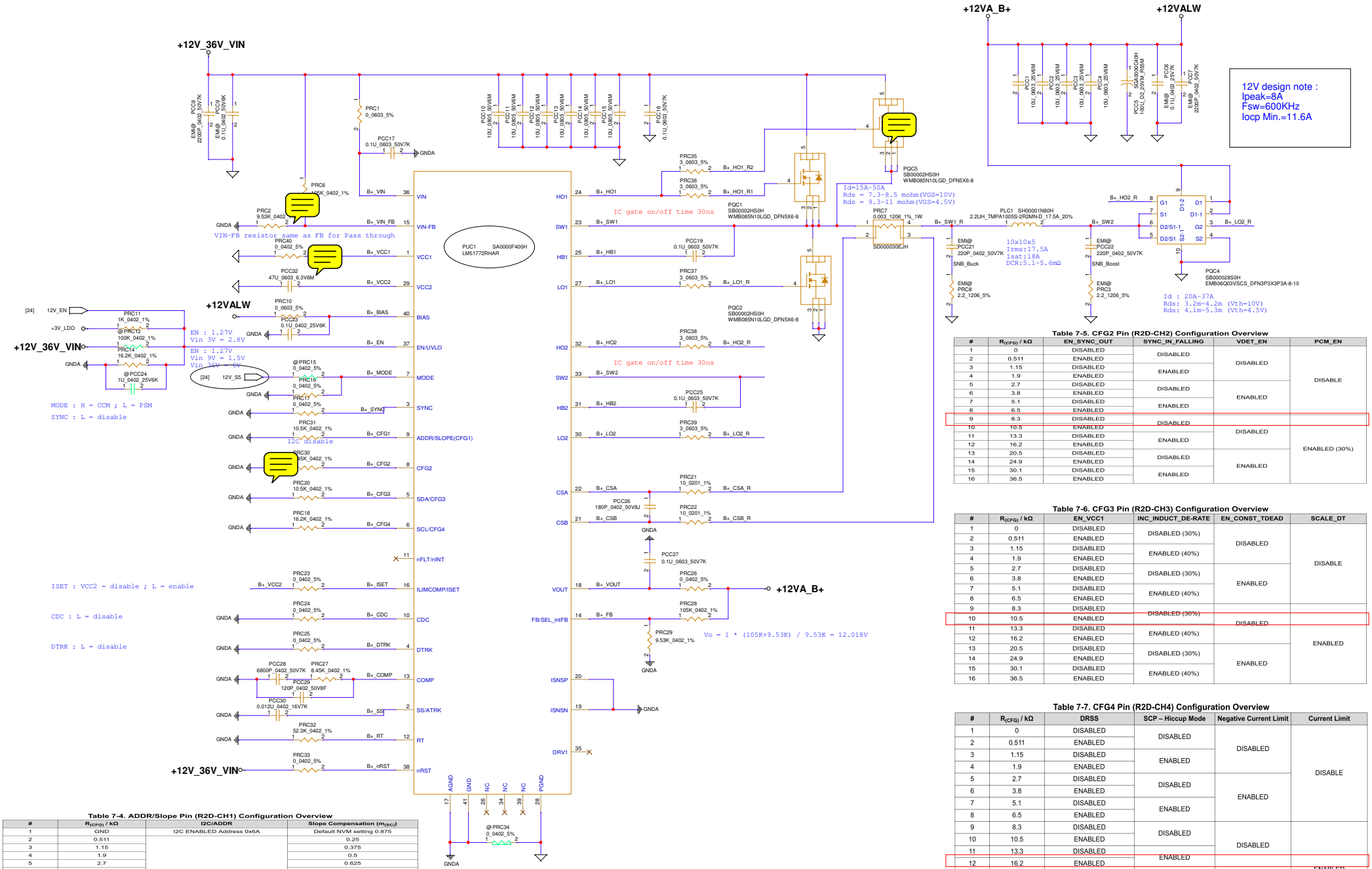

Table 7-4. ADDR/Slope Pin (R2D-CH1) Configuration Overview

#	$R_{(CFG)}$ / kΩ	I2C/ADDR	Slope Compensation (m_{SC})
1	GND	I2C ENABLED Address 0x6A	Default NVM setting 0.875
2	0.511		0.25
3	1.15		0.375
4	1.9		0.5
5	2.7		0.625
6	3.8		0.75
7	5.1		0.875
8	6.5	I2C DISABLED	1
9	8.3		1.5
10	10.5		2
11	13.3		2.5
12	16.2		3
13	20.5		3.5
14	24.9		4
15	30.1		4.5
16	VCC2	I2C ENABLED Address 0x6B	Default NVM setting 0.875

Table 7-5. CFG2 Pin (R2D-CH2) Configuration Overview

#	$R_{(CFG)}$ / kΩ	EN_SYNC_OUT	SYNC_IN_FALLING	VDET_EN	PCM_EN
1	0	DISABLED	DISABLED	DISABLED	DISABLE
2	0.511	ENABLED			
3	1.15	DISABLED	ENABLED		
4	1.9	ENABLED			
5	2.7	DISABLED	DISABLED	ENABLED	
6	3.8	ENABLED			
7	5.1	DISABLED	ENABLED		
8	6.5	ENABLED			
9	8.3	DISABLED	DISABLED		
10	10.5	ENABLED		DISABLED	ENABLED (30%)
11	13.3	DISABLED	ENABLED		
12	16.2	ENABLED			
13	20.5	DISABLED	DISABLED	ENABLED	
14	24.9	ENABLED			
15	30.1	DISABLED	ENABLED		
16	36.5	ENABLED			

Table 7-6. CFG3 Pin (R2D-CH3) Configuration Overview

#	$R_{(CFG)}$ / kΩ	EN_VCC1	INC_INDUCT_DE-RATE	EN_CONST_TDEAD	SCALE_DT
1	0	DISABLED	DISABLED (30%)	DISABLED	DISABLE
2	0.511	ENABLED			
3	1.15	DISABLED	ENABLED (40%)		
4	1.9	ENABLED			
5	2.7	DISABLED	DISABLED (30%)	ENABLED	
6	3.8	ENABLED			
7	5.1	DISABLED	ENABLED (40%)		
8	6.5	ENABLED			
9	8.3	DISABLED	DISABLED (30%)		
10	10.5	ENABLED		DISABLED	ENABLED
11	13.3	DISABLED	ENABLED (40%)		
12	16.2	ENABLED			
13	20.5	DISABLED	DISABLED (30%)	ENABLED	
14	24.9	ENABLED			
15	30.1	DISABLED	ENABLED (40%)		
16	36.5	ENABLED			

Table 7-7. CFG4 Pin (R2D-CH4) Configuration Overview

#	$R_{(CFG)}$ / kΩ	DRSS	SCP – Hiccup Mode	Negative Current Limit	Current Limit
1	0	DISABLED	DISABLED	DISABLED	DISABLE
2	0.511	ENABLED			
3	1.15	DISABLED	ENABLED		
4	1.9	ENABLED			
5	2.7	DISABLED	DISABLED	ENABLED	
6	3.8	ENABLED			
7	5.1	DISABLED	ENABLED		
8	6.5	ENABLED			
9	8.3	DISABLED	DISABLED		
10	10.5	ENABLED		DISABLED	ENABLED
11	13.3	DISABLED	ENABLED		
12	16.2	ENABLED			
13	20.5	DISABLED	DISABLED	ENABLED	
14	24.9	ENABLED			
15	30.1	DISABLED	ENABLED		
16	36.5	ENABLED			

Compal Electronics, Inc.
Title: LPDDR5
Size: Custom | Document Number: LA-P741P | Rev: 0.2
Date: Thursday, August 21, 2025 | Sheet 1 of 1