
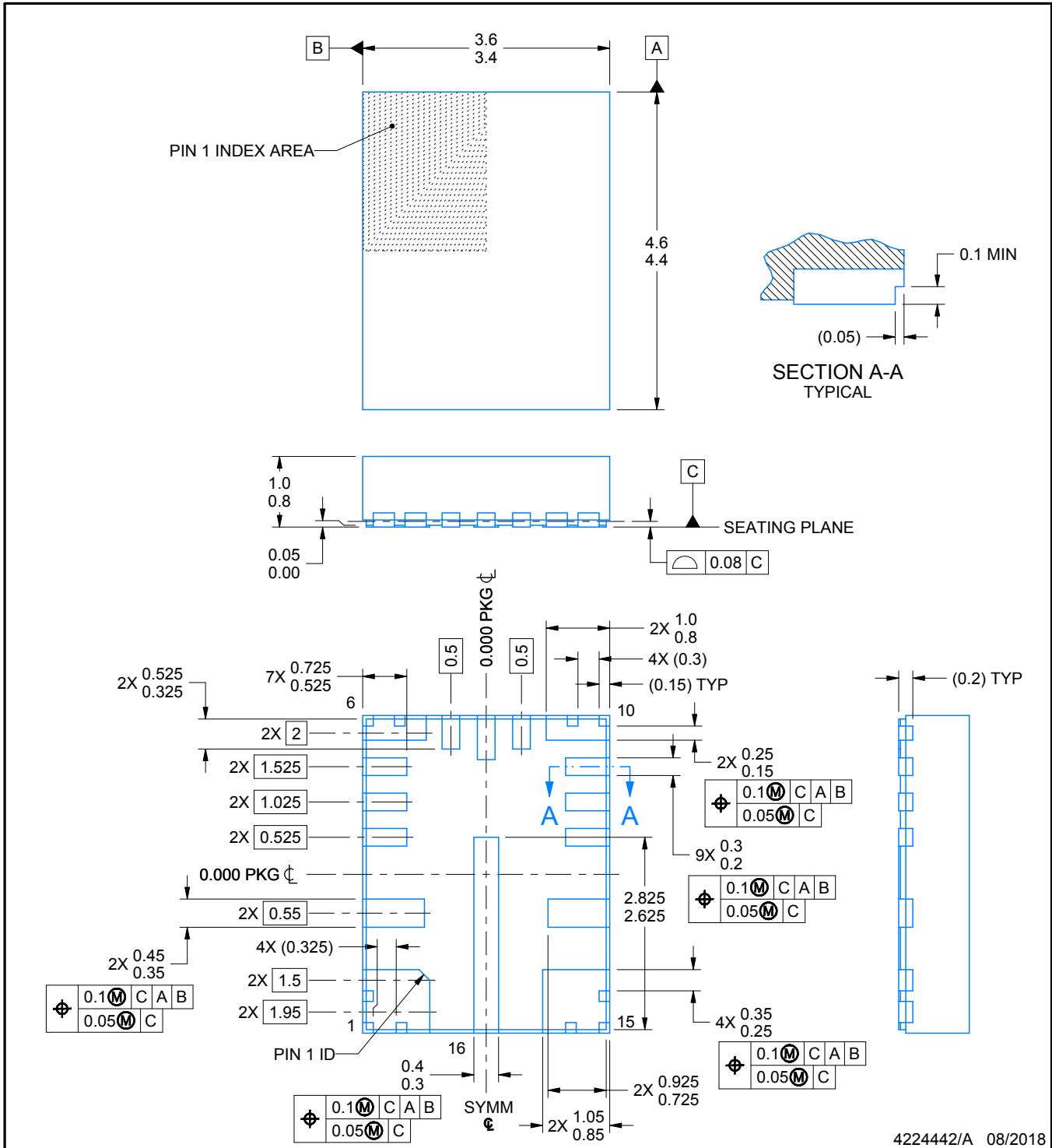
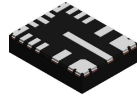


DATA BOOK PACKAGE OUTLINE

DRAFTER: K. SINCERBOX	DATE: 08/17/2018		DIMENSIONS IN MILLIMETERS
DESIGNER:	DATE:	 TEXAS INSTRUMENTS <small>SEMICONDUCTOR OPERATIONS</small>	CODE IDENTITY NUMBER 01295
CHECKER: K. SINCERBOX	DATE: 08/17/2018		
ENGINEER: S. JAFFE	DATE: 08/17/2018		
APPROVED: D. CHIN & D. BABARAN	DATE: 08/17/2018		
RELEASED: WDM	DATE: 08/17/2018		
TEMPLATE INFO: EDGE# 4218519		DATE: 04/07/2016	
SCALE NTS	SIZE A	4224442	REV A PAGE 1 OF 5



4224442/A 08/2018

NOTES:

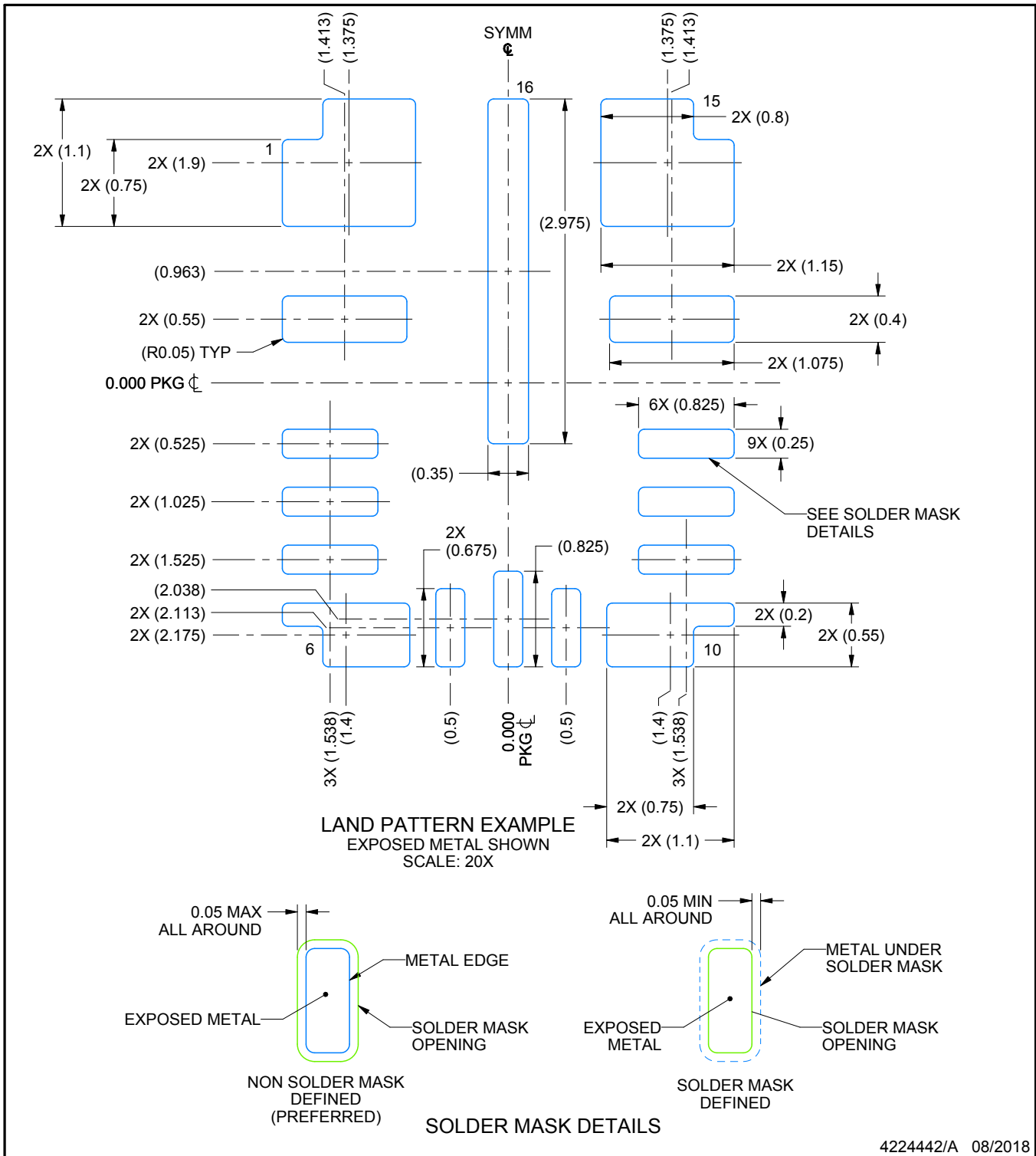
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

RPH0016A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4224442/A 08/2018

NOTES: (continued)

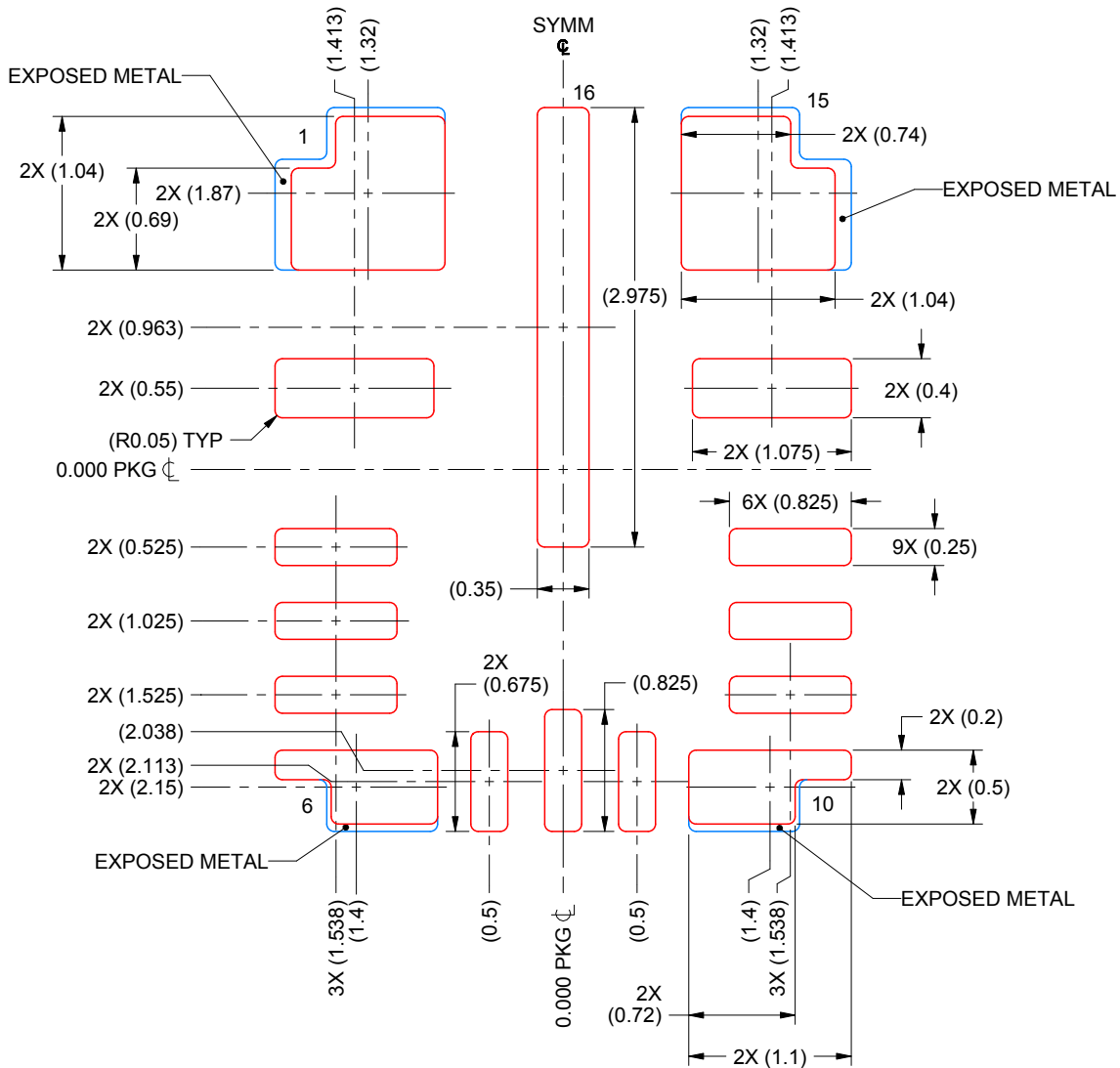
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RPH0016A

VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
 BASED ON 0.125 MM THICK STENCIL
 SCALE: 20X

PADS 1 & 15:
 85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
 PADS 6 & 10:
 90% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224442/A 08/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

REVISIONS

REV	DESCRIPTION	ECR	DATE	ENGINEER / DRAFTER
A	RELEASE NEW DRAWING	2175530	08/17/2018	S. JAFFE / K. SINCERBOX