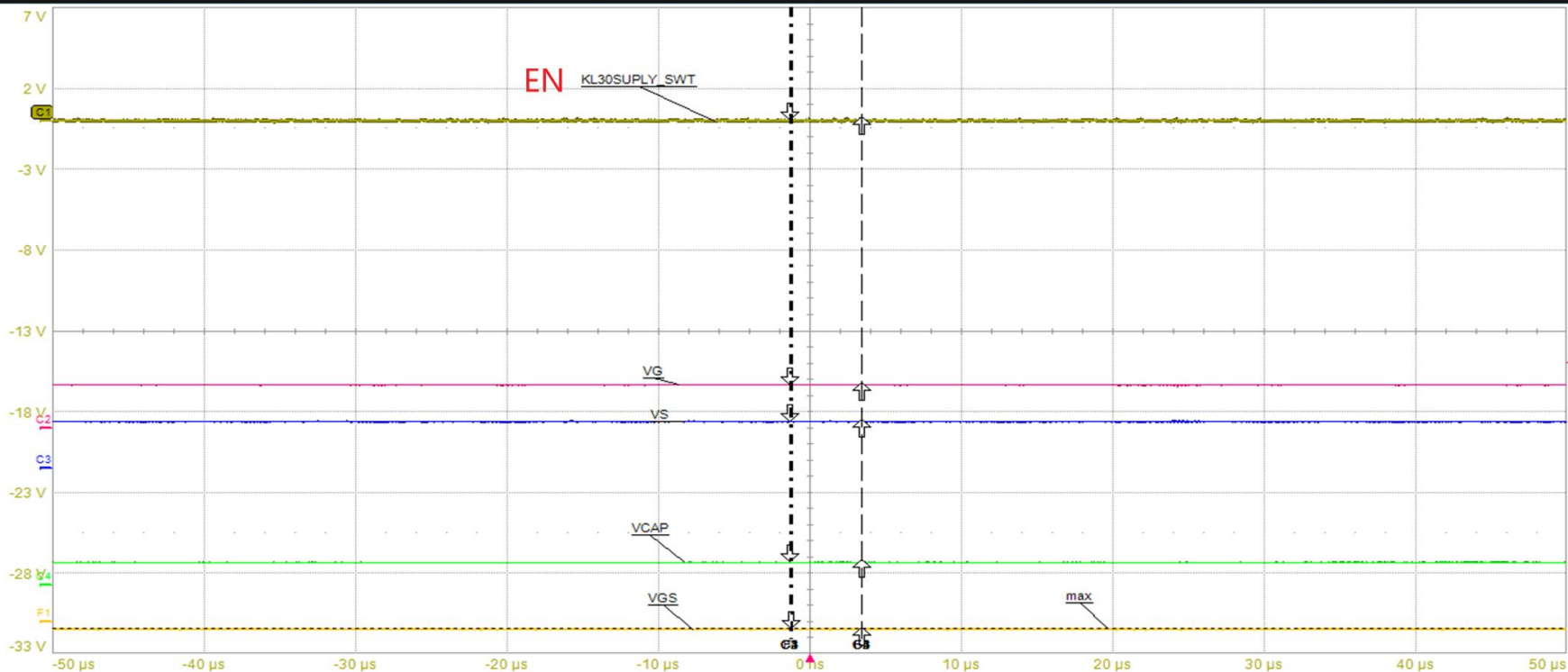


# LM74700 Module test



Measure	P1: max(C1)	P2: min(C1)	P3: max(C2)	P4: min(C2)	P5: max(C3)	P6: min(C3)	P7: max(F1)	P8: min(F1)
value	140 mV	-190 mV	5.34 V	5.11 V	5.85 V	5.64 V	-440 mV	-570 mV
status								
C1	ESR(DC1M)	C2	E(F)D1	C3	E(F)D1	C4	E(F)D1	F1 zoom((C2...
5.00 V/div	10.0 V/div	10.0 V/div	20.0 V/div	5.00 V/div	10.0 V/div	20.0 V/div	5.00 V/div	5.00 V/div
13.000 V	-12.0000 V	-17.0000 V	-63.0000 V	10.0 μs/div	10.0 μs/div	20.0 V/div	10.0 μs/div	10.0 μs/div
-22 mV	5.2413 V	5.7363 V	5.5725 V	-495.3 mV	-12 mV	5.2350 V	5.7237 V	5.5075 V
-12 mV	5.2350 V	5.7237 V	5.5075 V	-487.8 mV				

HD	时基	0.0 μs	触发	C2 DC
12 Bits	1 MS	10.0 μs/div	自动	8.1 V
		10 GS/s	边沿	或
X1=	-1.2500 μs	ΔX=	4.7458 μs	
X2=	3.4958 μs	1/ΔX=	210.713 kHz	

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	DATA1	DATA2	MAX	MIN	
MCUIO	0	0	0.14	-0.19	V
VS (Vanode)	5.74	5.72			V
VG (GATE)	5.24	5.24			V
VCAP	5.61	5.562			V
VGS	-0.5	-0.48	-0.44	-0.57	V
VCAP-VS	-0.13	-0.158			V

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

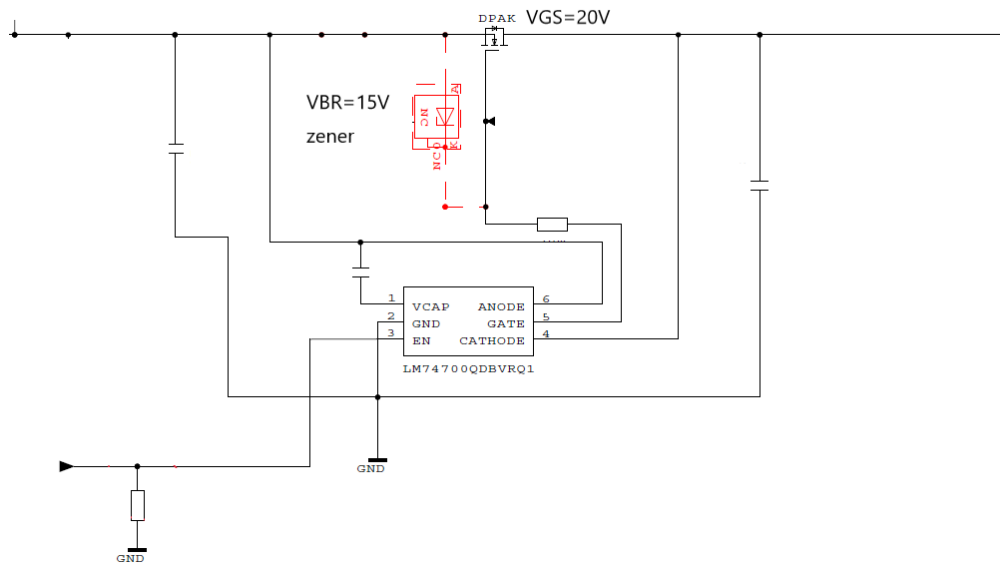
		MIN	MAX	UNIT
Input Pins	ANODE to GND	-65	65	V
	EN to GND, $V_{(ANODE)} > 0$ V	-0.3	65	V
	EN to GND, $V_{(ANODE)} \leq 0$ V	$V_{(ANODE)}$	$(65 + V_{(ANODE)})$	V
Output Pins	GATE to ANODE	-0.3	15	V
	VCAP to ANODE	-0.3	15	V
Output to Input Pins	CATHODE to ANODE	-5	75	V
Operating junction temperature <sup>(2)</sup>		-40	150	°C
Storage temperature, $T_{stg}$		-40	150	°C

According to the datasheet

Maxrating Gate to anode is about : -0.3V~15V

Q1: -0.3V? How does this value come from? If the Gate-anode  $< -0.3V$ , what problem will it causes?

Q2: As the waveform shows when Vanode is 5.7V, EN=0, why the VGS is  $< -0.3V$ , about this what circuit or element should we do to solve this problem?



Q3:

Add one Zener which  $V_{BR} = 15V$ , please evaluate the feasibility of this circuit.

THX