7.4 Thermal Information

The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and cannot be used for design purposes. These values were calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. They do not represent the performance obtained in an actual application. For example, with a 2-layer PCB, a $R_{\theta JA}$ = 80°C/W can be achieved. For design information, see Maximum Output Current Versus Ambient Temperature.

THERMAL METRIC(1)		DDC (SOT-23-6) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	107.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

Limits apply over operating junction temperature (T_J) range of –40°C to +150°C, unless otherwise stated. Minimum and maximum limits(1) are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4.5 V to 36 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
$I_{Q(VIN)}$	VIN quiescent current (non-switching)(2)	V_{EN} = 3 V, PFM variant only		40	65	µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{EN} = 0 V		3	15	µA
UVLO						
$VIN_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising		3.89	4.5	V
$VIN_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling	3.35	3.58		V
$VIN_{UVLO(H)}$	VIN UVLO hysteresis			0.3		V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.1	1.227	1.36	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	0.95	1.08	1.22	V
$I_{EN(P2)}$	EN pin sourcing current post EN rising threshold	V_{EN} = 3 V		10	200	nA
REFERENCE VOLTAGE						
Vfb	Reference voltage		0.591	0.6	0.609	V
$I_{FB(LKG)}$	FB input leakage current	V_{FB} = 1.2 V		0.8	50	nA
SWITCHING FREQUENCY						
$f_{SW1(CCM)}$	Switching frequency, CCM operation	500-kHz trim option	450	500	560	kHz
$f_{SW2(CCM)}$	Switching frequency, CCM operation	1.1-MHz trim option	0.95	1.1	1.25	MHz
STARTUP						
t_{SS}	Internal fixed soft-start time		3.2	4.0	5.4	ms
POWER STAGE						
$R_{DSON(HS)}$	High-side MOSFET on-resistance	T_J = 25°C		0.12		Ω
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	T_J = 25°C		0.07		Ω
$t_{ON(min)}$	Minimum ON pulse width	V_{IN} = 12 V, I_{OUT} = 2 A		70		ns
$t_{ON(max)}$	Maximum ON pulse width	V_{IN} = 12 V, I_{OUT} = 2 A		6.76		µs
$t_{OFF(min)}$	Minimum OFF pulse width	V_{IN} = 4.5 V		150		ns
OVERCURRENT PROTECTION						
$I_{HS\_PK(OC)}$	High-side peak current limit(3)	LM51420	2.7	3.5	5.1	A