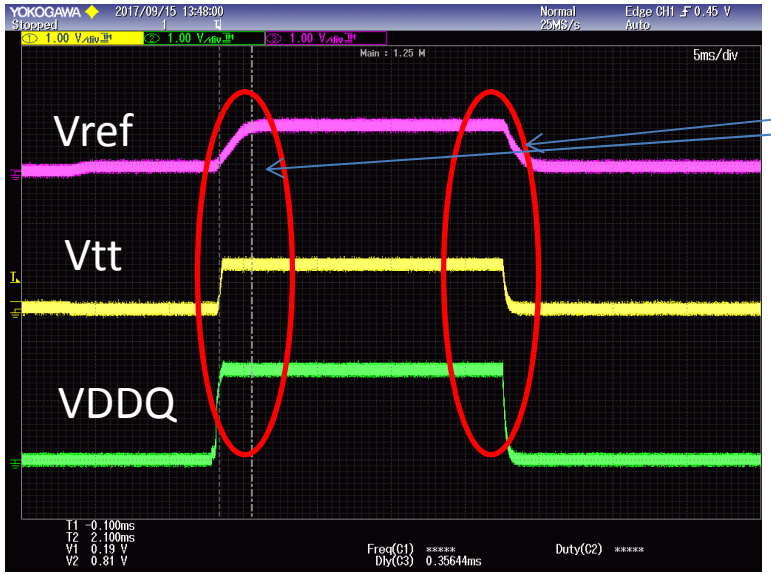
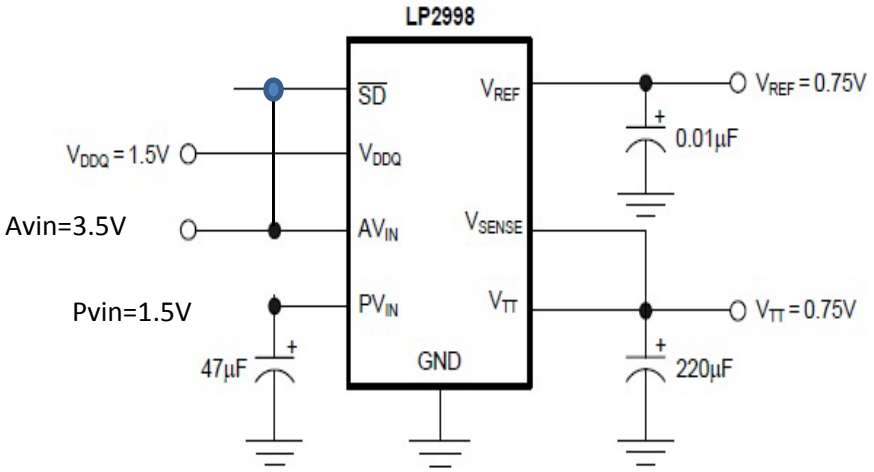
■LP2998：Vrefoutput



Vref:A few mS（milliseconds）delay



Sequence：AVIN＝SD=3.5V → VDDQ=PVIN=1.5V
MEM:DDR3 1 piece

Question
・Why is the rising and falling edge of Vref terminal delayed by several mS?