Pin	Name	I/O	Purpose	Connection for functional use	Connection if not used	Check if complete	Comments
1	FB_B2	A	Output voltage feedback (positive) for the BUCK2 converter.	In 2+1+1-ph, 1+1+1+1-ph and 2+2-ph config connect to point-of-load capacitor positive terminal	Connect to ground	Not used & completed	
2	EN3	D/I/O	Programmable enable signal for the buck regulators (can be also configured to select between two buck output-voltage levels). This pin functions alternatively as GPIO3.	If used as EN3 or GPIO3 input/output connect appropriate control signal. Check pull-up resistor if configured as open-drain output.	Not connected	Not used & completed	
3	CLKIN	D/I	External clock input	Connect external clock signal to this pin if synchronization is needed. Check frequency	Connect to ground	Not used & completed	
4, 17, ThermalPad	AGND	G	Ground	Connect to ground potential	Connect to ground	Used & completed	
5	SCL	D/I	Serial interface clock input for I2C access	Connect I2C compatible serial clock. Check pull-up resistor	Connect to ground	Used & completed	
6	SDA	D/I/O	Serial interface data input/output for I2C access	Connect I2C compatible serial data. Check pull-up resistor	Connect to ground	Used & completed	
7	EN1	D/I/O	Programmable enable signal for the buck regulators (can be also configured to select between two buck output-voltage levels). This pin functions alternatively as GPIO1.	If used as EN1 or GPIO1 input/output connect appropriate control signal. Check pull-up resistor if configured as open-drain output.	Not connected	Used & completed	
8	FB_B0	A	Output voltage feedback (positive) for the BUCK0 converter.	In 1+1+1+1-ph, 4-ph, 3+1-ph, 2+1+1-ph and 2+2-ph configs connect to point-of-load capacitor positive terminal	N/A	Used & completed	
9	VIN_B0	P	Input for the BUCK0 converter	The separate power pins, VIN_Bx, have to be connected together. Bypass locally with 10µF capacitor.	N/A	Used & completed	
10	SW_B0	A	BUCK0 switch node	Connect to 470nH inductor + 22uF output capacitor with additional 22uF point of load capacitor. If VIN >4V snubber circuit (390pF + 3.9ohm) needs to be used.	Not connected	Open	Check total output capacitance. At least 22+22uF would be needed per phase (176uF total)
11	PGND_B01	G	Power ground for the BUCK0 and BUCK1	Connect to ground potential	Connect to ground	Used & completed	
12	SW_B1	A	BUCK1 switch node	Connect to 470nH inductor + 22uF output capacitor with additional 22uF point of load capacitor. If VIN >4V snubber circuit (390pF + 3.9ohm) needs to be used.	Not connected	Open	Check total output capacitance. At least 22+22uF would be needed per phase (176uF total)
13	VIN_B1	P	Input for the BUCK1 converter	The separate power pins, VIN_Bx, have to be connected together. Bypass locally with 10µF capacitor.	N/A	Used & completed	
14	FB_B1	A	Output voltage feedback (positive) for the BUCK1 converter. Alternatively as the output ground feedback (negative) for the BUCK0 converter	In 1+1+1+1-ph connect to point-of-load capacitor positive terminal. In 4-ph, 3+1-ph, 2+1+1-ph and 2+2-ph configs connect to point-of-load capacitor negative terminal	N/A	Used & completed	
15	EN2	D/I/O	Programmable enable signal for the buck regulators (can be also configured to select between two buck output-voltage levels). This pin functions alternatively as GPIO2.	If used as EN2 or GPIO2 input/output connect appropriate control signal. Check pull-up resistor if configured as open-drain output.	Not connected	Not used & completed	
16	PGOOD	D/O	Power-good indication signal	Check pull-up resistor if configured as open-drain output	Not connected	Not used & completed	
18	VANA	P	Supply voltage for the analog and digital blocks	Pin must be connected to the same node as VIN_Bx. Bypass with 100nF capacitor	N/A	Used & completed	
19	nINT	D/O	Interrupt output. Active low	Check pull-up resistor if used	Not connected	Used & completed	
20	NRST	D/I	Reset signal for the device	Must be controlled or connected to same node as VIN_Bx	N/A	Used & completed	
21	FB_B3	A	Output voltage feedback (positive) for the BUCK3 converter. Alternatively as the output ground feedback (negative) for the BUCK2 converter	In 3+1-ph, 2+1+1-ph and 1+1+1+1 connect to point-of-load capacitor positive terminal. In 2+2-ph config connect to point-of-load capacitor negative terminal	Connect to ground	Not used & completed	
22	VIN_B3	P	Input for the BUCK3 converter	The separate power pins, VIN_Bx, have to be connected together. Bypass locally with 10µF capacitor.	N/A	Used & completed	
23	SW_B3	A	BUCK3 switch node	Connect to 470nH inductor + 22uF output capacitor with additional 22uF point of load capacitor. If VIN >4V snubber circuit (390pF + 3.9ohm) needs to be used.	Not connected	Open	Check total output capacitance. At least 22+22uF would be needed per phase (176uF total)
24	PGND_B23	G	Power ground for the BUCK2 and BUCK3	Connect to ground potential	Connect to ground	Used & completed	
25	SW_B2	A	BUCK2 switch node	Connect to 470nH inductor + 22uF output capacitor with additional 22uF point of load capacitor. If VIN >4V snubber circuit (390pF + 3.9ohm) needs to be used.	Not connected	Open	Check total output capacitance. At least 22+22uF would be needed per phase (176uF total)
26	VIN_B2	P	Input for the BUCK2 converter	The separate power pins, VIN_Bx, have to be connected together. Bypass locally with 10µF capacitor.	N/A	Used & completed	

Note: A: Analog Pin, D: Digital Pin, G: Ground Pin, P: Power Pin, I: Input Pin, O: Output Pin

CHECK TOTAL OUTPUT CAPACITANCE PER PHASE AGAINST TABLE BELOW
Recommended minimum 22µF local output capacitor and 22µF at the point of load capacitor per phase. Maximum per phase depends on slew-rate and switching frequency. Values below are valid for 2MHz switching frequency.

Open — Check that total capacitance does not exceed the limits

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output voltage slew-rate(5)	SLEW_RATEx[2:0] = 2h, $C_{OUT-TOTAL}$ ≤ 80 µF/phase	–15%	10	15%	mV/µs
	SLEW_RATEx[2:0] = 3h, $C_{OUT-TOTAL}$ ≤ 130 µF/phase	–15%	7.5	15%	
	SLEW_RATEx[2:0] = 4h, $C_{OUT-TOTAL}$ ≤ 250 µF/phase	–15%	3.8	15%	
	SLEW_RATEx[2:0] = 5h, $C_{OUT-TOTAL}$ ≤ 500 µF/phase	–15%	1.9	15%	
	SLEW_RATEx[2:0] = 6h, $C_{OUT-TOTAL}$ ≤ 500 µF/phase	–15%	0.94	15%	
	SLEW_RATEx[2:0] = 7h, $C_{OUT-TOTAL}$ ≤ 500 µF/phase	–15%	0.47	15%	

Pin	Name	I/O	Purpose	High frequency	Max current	Layout advice	Check if complete	Comments
1	FB_B2	A	Output voltage feedback (positive) for the BUCK2 converter.	-	High impedance	Avoid crosstalk from high frequency switching signals. In 2+1+1-ph and 1+1+1+1-ph connect to point-of-load capacitor positive terminal. In 2+2-ph config route differentially with FB_B3 to point-of-load capacitor positive terminal	Not used & completed	
2	EN3	D/I/O	Programmable enable signal for the buck regulators (can be also configured to select between two buck output-voltage levels). This pin functions alternatively as GPIO3.	-	-	-	Not used & completed	
3	CLKIN	D/I	External clock input	Yes	-	This trace can cause crosstalk, avoid routing near sensitive signals	Not used & completed	
4, 17, ThermalPad	AGND	G	Ground	-	-	Connect pins together and with multiple vias to ground plane	Used & completed	
5	SCL	D/I	Serial interface clock input for I2C access	Yes	-	This trace can cause crosstalk, avoid routing near sensitive signals	Used & completed	
6	SDA	D/I/O	Serial interface data input/output for I2C access	Yes	-	This trace can cause crosstalk, avoid routing near sensitive signals	Used & completed	
7	EN1	D/I/O	Programmable enable signal for the buck regulators (can be also configured to select between two buck output-voltage levels). This pin functions alternatively as GPIO1.	-	-	-	Used & completed	
8	FB_B0	A	Output voltage feedback (positive) for the BUCK0 converter.	-	High impedance	Avoid crosstalk from high frequency switching signals. In 1+1+1+1-ph connect to point-of-load capacitor positive terminal. In 4-ph, 3+1-ph, 2+1+1-ph and 2+2-ph configs route differentially with FB_B1 to point-of-load capacitor positive terminal	Used & completed	
9	VIN_B0	P	Input for the BUCK0 converter	-	6A DC	Place input capacitor as close to device as possible. Use wide trace/copper layer for routing. Ensure strong connection to ground plane also	Open	Input capacitor GND quite far away from the output capacitor GND causing large current loops. Check is it possible to place input capacitors to bottom side as in LP87561Q1EVM
10	SW_B0	A	BUCK0 switch node	Yes	4A DC + 0.5 x Iripple	Keep trace to inductor short and wide. Place snubber components on same layer as device, as small current loop as possible	Used & completed	
11	PGND_B01	G	Power ground for the BUCK0 and BUCK1	-	-	Ensure strong connection to ground plane with multiple vias. Separate from AGND/thermal pad on top layer	Open	Remove connection from center pad. See datasheet layout example.
12	SW_B1	A	BUCK1 switch node	Yes	4A DC + 0.5 x Iripple	Keep trace to inductor short and wide. Place snubber components on same layer as device, as small current loop as possible	Used & completed	
13	VIN_B1	P	Input for the BUCK1 converter	-	6A DC	Place input capacitor as close to device as possible. Use wide trace/copper layer for routing. Ensure strong connection to ground plane also	Open	Input capacitor GND quite far away from the output capacitor GND causing large current loops. Check is it possible to place input capacitors to bottom side as in LP87561Q1EVM
14	FB_B1	A	Output voltage feedback (positive) for the BUCK1 converter. Alternatively as the output ground feedback (negative) for the BUCK0 converter	-	High impedance	Avoid crosstalk from high frequency switching signals. In 1+1+1+1-ph connect to point-of-load capacitor positive terminal. In 4-ph, 3+1-ph, 2+1+1-ph and 2+2-ph configs route differentially with FB_B0 to point-of-load capacitor negative terminal	Used & completed	
15	EN2	D/I/O	Programmable enable signal for the buck regulators (can be also configured to select between two buck output-voltage levels). This pin functions alternatively as GPIO2.	-	-	-	Not used & completed	
16	PGOOD	D/O	Power-good indication signal	-	-	-	Not used & completed	
18	VANA	P	Supply voltage for the analog and digital blocks	-	100mA DC	Place input capacitor as close to device as possible. Use wide trace/copper layer for routing. Ensure strong connection to ground plane also	Open	Check is it possible to rotate the bypass cap on top layer so that the GND is close to the GNDA pin 17. Then it would be possible to route the GND on top layer as well (with vias also to GND plane)
19	nINT	D/O	Interrupt output. Active low	-	-	-	Used & completed	
20	NRST	D/I	Reset signal for the device	-	-	-	Used & completed	
21	FB_B3	A	Output voltage feedback (positive) for the BUCK3 converter. Alternatively as the output ground feedback (negative) for the BUCK2 converter	-	High impedance	In 3+1-ph, 2+1+1-ph and 1+1+1+1 connect to point-of-load capacitor positive terminal. In 2+2-ph config route differentially with FB_B2 to point-of-load capacitor negative terminal	Not used & completed	

22	VIN_B3	P	Input for the BUCK3 converter	-	6A DC	Place input capacitor as close to device as possible. Use wide trace/copper layer for routing. Ensure strong connection to ground plane also	Open	Input capacitor GND quite far away from the output capacitor GND causing large current loops. Check is it possible to place input capacitors to bottom side as in LP87561Q1EVM
23	SW_B3	A	BUCK3 switch node	Yes	4A DC + 0.5 x Iripple	Keep trace to inductor short and wide. Place snubber components on same layer as device, as small current loop as possible	Used & completed	
24	PGND_B23	G	Power ground for the BUCK2 and BUCK3	-	-	Ensure strong connection to ground plane with multiple vias. Separate from AGND/thermal pad on top layer	Open	Remove connection from center pad. See datasheet layout example.
25	SW_B2	A	BUCK2 switch node	Yes	4A DC + 0.5 x Iripple	Keep trace to inductor short and wide. Place snubber components on same layer as device, as small current loop as possible	Used & completed	
26	VIN_B2	P	Input for the BUCK2 converter	-	6A DC	Place input capacitor as close to device as possible. Use wide trace/copper layer for routing. Ensure strong connection to ground plane also	Open	Input capacitor GND quite far away from the output capacitor GND causing large current loops. Check is it possible to place input capacitors to bottom side as in LP87561Q1EVM

Note: A: Analog Pin, D: Digital Pin, G: Ground Pin, P: Power Pin, I: Input Pin, O: Output Pin

Date	Version	Notes
2019 January	1.0	Initial version
2020 January	1.1	Refined FB_Bx connections text
2020 February	1.2	Added note to layout section PGND_B01 and PGND_B23 "Separate from AGND

/thermal pad on top layer"