Layout guidelines and example for the BQ24610, BQ24616, BQ24617, BQ24618, and BQ24630.

Layout Guidelines

Proper layout of the components to minimize the high-frequency current-path loop is important to prevent electrical and magnetic field radiation and high-frequency resonant problems. Here is a PCB layout priority list for proper layout.

RULES	COMPONENTS	FUNCTION	IMPACT	GUIDELINES
1		PCB Layer Stack Up	Thermal efficiency, signal integrity	Multi- layer PCB is suggested. Allocate at least two ground layers. The BQ24610EVM uses a 4-layer PCB (top layer, two signal layers, and bottom layer)
2	$C_{IN,}$ Q_H,Q_L	Input Loop	High frequency noise, ripple	Place the input capacitor as close as possible to the drain of Q_H MOSFET and the source of the Q_L MOSFET and use the shortest possible copper trace connection. These parts should be placed on the same layer of the PCB instead of on different layers and should use vias to make this connection.
3	Q_H, Q_L	Gate Drive Path	High frequency noise	The IC should be placed close to the switching MOSFET gate terminals to keep the gate-drive signal traces short for a clean MOSFET drive. The IC can be placed on the other side of the PCB from the switching MOSFETs.
4	L, Q_H,Q_L	Current Path	Efficiency, high frequency noise, ripple	Place the inductor input terminal as close as possible to the switching MOSFET output terminal. Minimize the copper area of this trace to lower electrical and magnetic field radiation, but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.

5	L, R_{SR}	Current sense	Regulation accuracy	The charging-current sensing resistor should be placed right next to the inductor output. Route the sense leads connected across the sensing resistor back to the IC in same layer, close to each other (minimize loop area) and do not route the sense leads through a high-current path (see Figure 27 of the BQ24610 datasheet for Kelvin connection for best current accuracy). Place the decoupling capacitor on these traces next to the IC.
6	C_{BAT}, R_{SR}	Output loop	High frequency noise, ripple	Place the output capacitor next to the sensing resistor output and ground. Output capacitor ground connections must be tied to the same copper that connects to the input capacitor ground before connecting to system ground.
7		Ground partition	Measurement accuracy, regulation accuracy, jitter, ripple	Route the analog ground separately from the power ground and use a single ground connection to tie the charger power ground to the charger analog ground. Just beneath the IC, use the copper-pour for analog ground, but avoid power pins to reduce inductive and capacitive noise coupling. Connect analog ground and power ground together using the thermal pad as the single ground connection point. Or use a 0-Ω resistor to tie analog ground to power ground (thermal pad should tie to analog ground in this case). A star connection under the thermal pad is highly recommended.
8		Thermal pad	Efficiency	It is critical to solder the exposed thermal pad on the back side of the IC package to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
9	Small capacitors	IC Bypass Capacitors	Noise, jitter, ripple	Place decoupling capacitors next to the IC pins and make the trace connection as short as possible.
10		Vias	Efficiency	Size and number of all vias must be enough for a given current path.

Layout Example

Based on the above layout guidelines, the buck charger layout example top view is shown below including all the key power components.