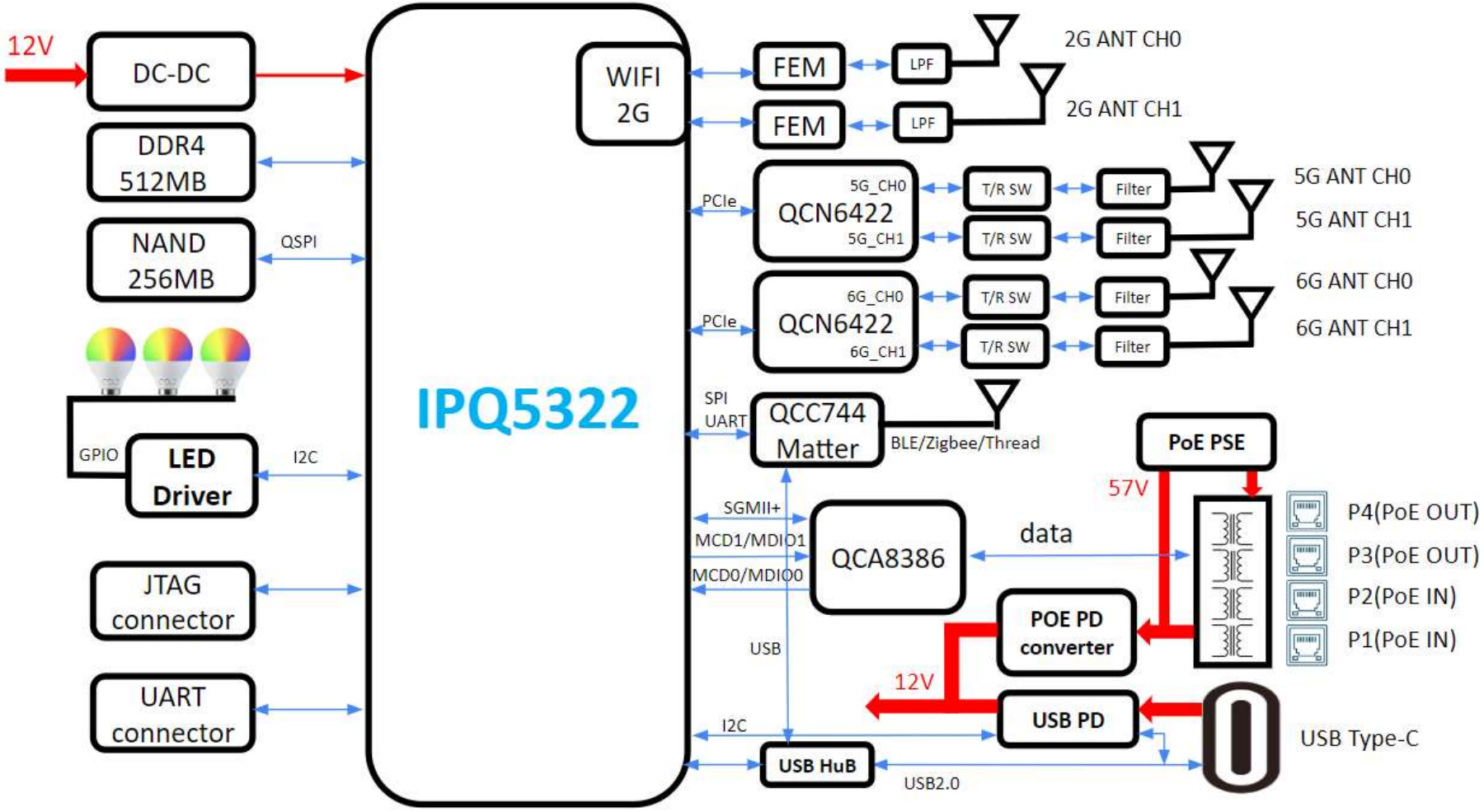
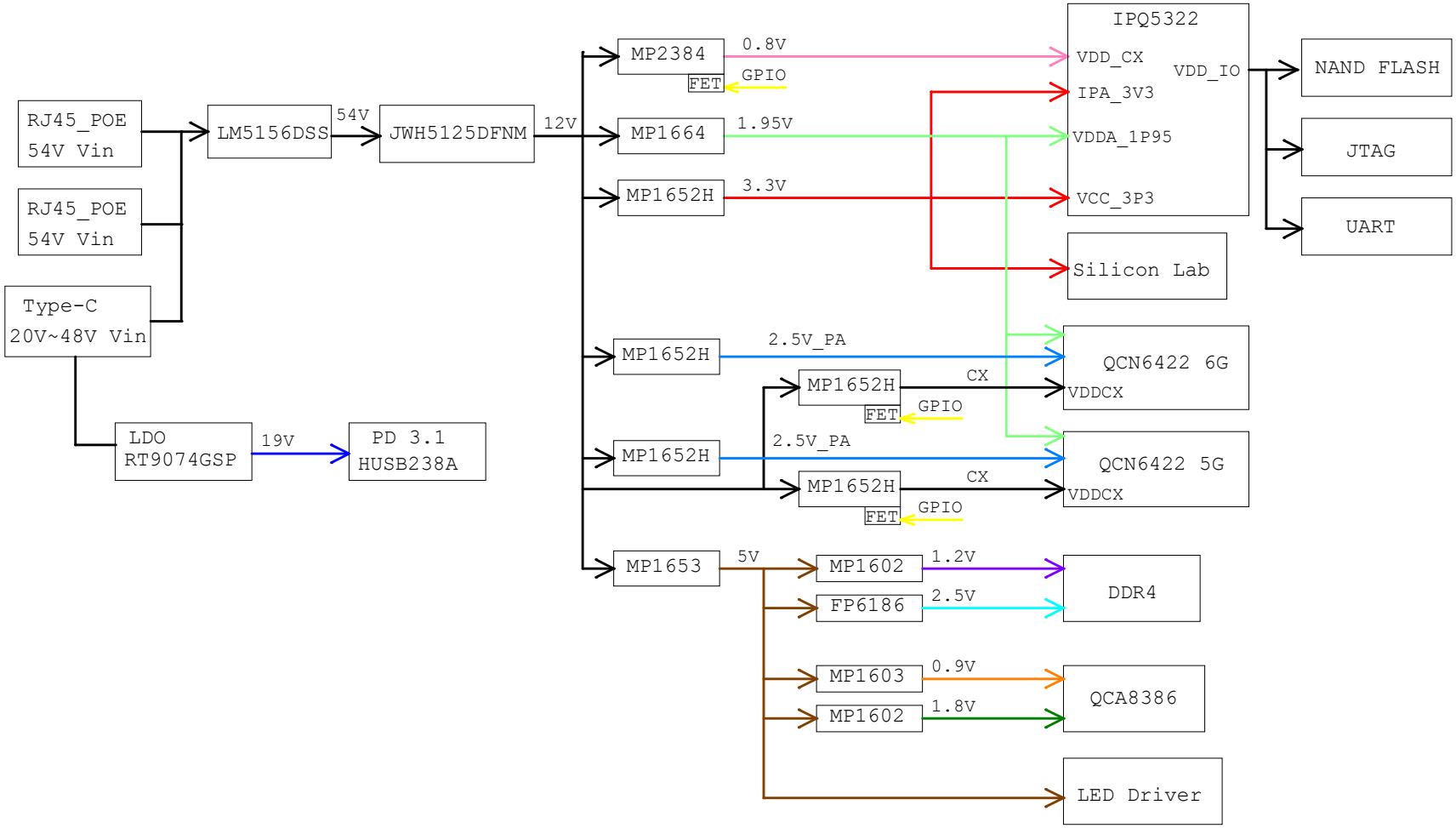
SCHEMATIC, CCA, IPQ5312, AP.MI04.1, 512MB DDR4, 2X2 2G iPA, 2X2 5G iPA,2X2 6G iPA, USB2.0, QCA8386, MDIO SFP



Functional Block Diagram

Inventec Appliances Corporation			
Approval:	Title	02_Functional Block_Diagram	
Check:	Size B	Document Number LUCKY 7	Rev PT1
Design:	Date: Thursday, July 18, 2024	Sheet 2 of 35	

Power Regs Diagram



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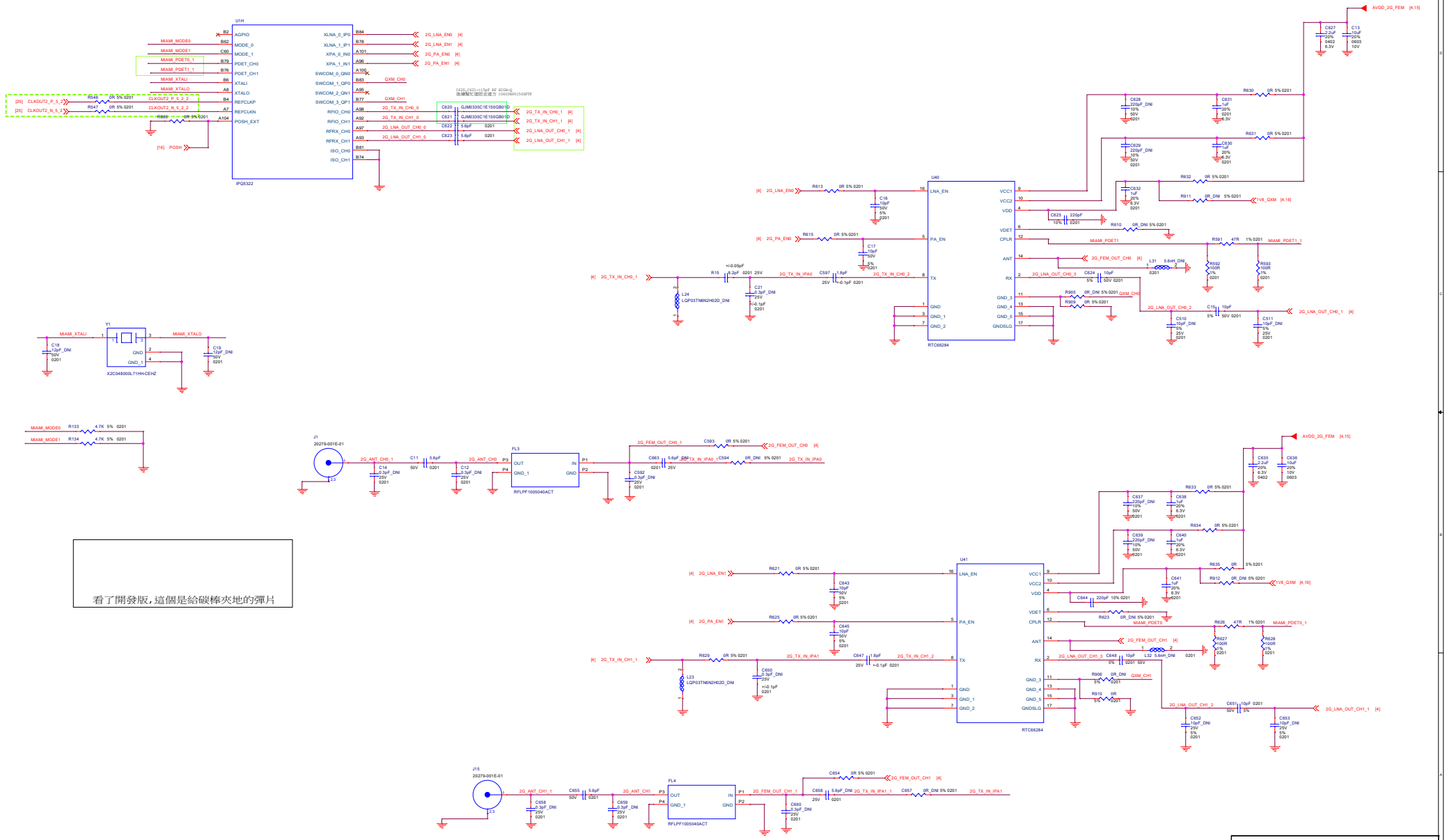
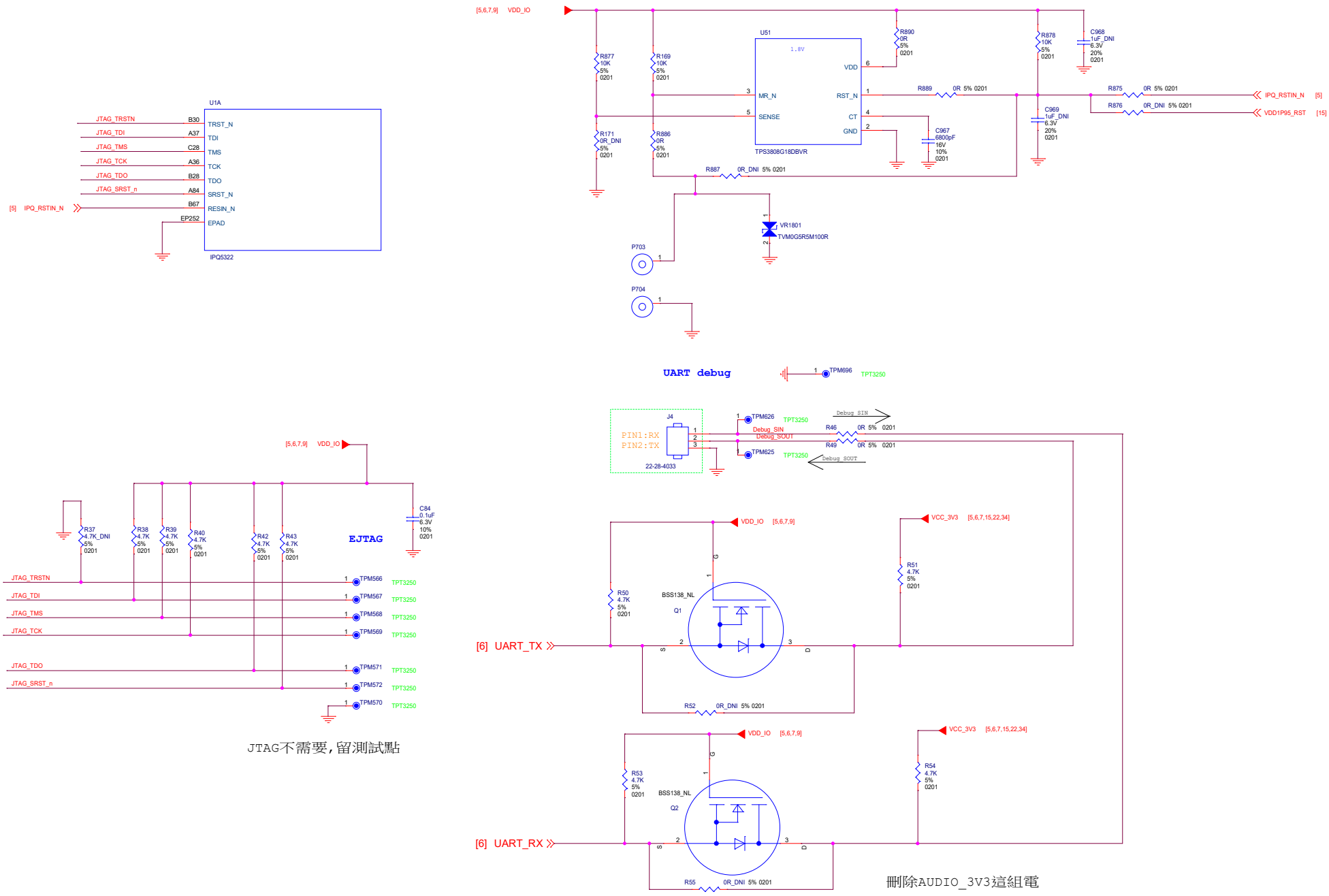
Approval:	Title	03_Power Regs Diagram	
Check:	Size C	Document Number LUCKY 7	Rev PT1
Design:	Date: Thursday, July 18, 2024	Sheet 3 of 35	



Inventec Appliances Corporation

Approval:	Title: 04_RFA_2G_FEM		
Check:	Size:	Document Number: LUCKY 7	Rev: PT1
Design:	D		
	Date: Friday, July 26, 2024	Sheet 4 of 35	

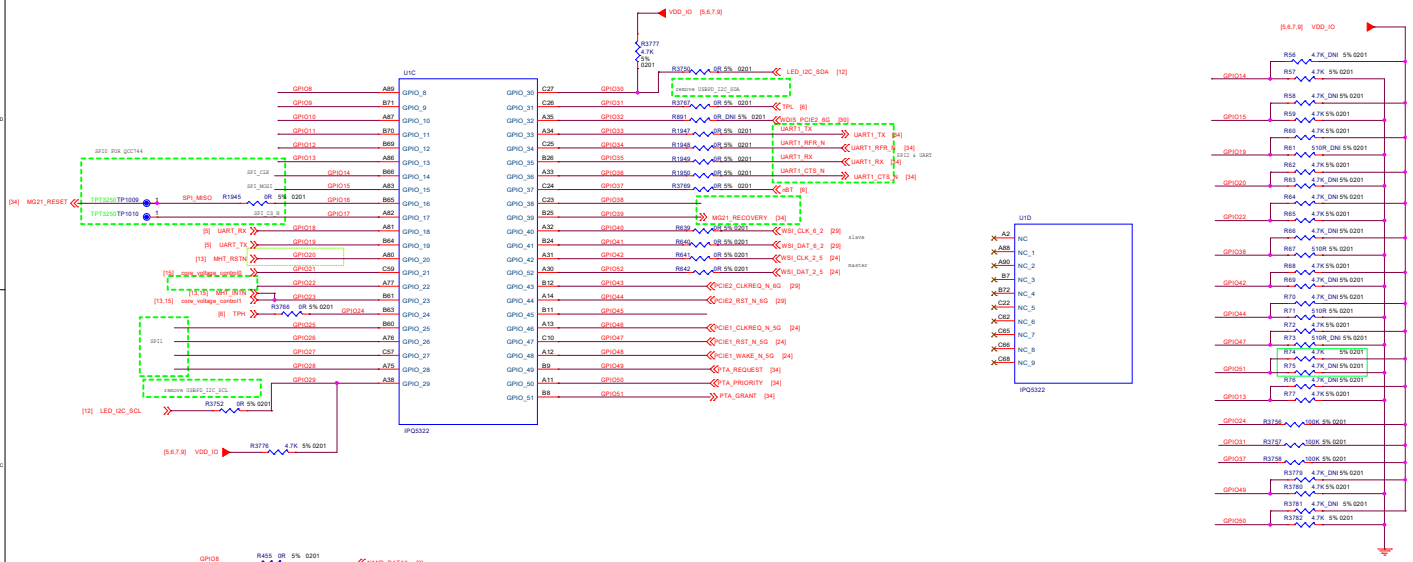
RFA_2G_FEM



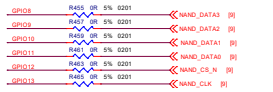
JTAG不需要,留測試點

刪除AUDIO_3V3這組電

Inventec Appliances Corporation			
Approval:	Title	05_EJTAG_UART_Reset	
Check:	Size C	Document Number LUCKY 7	Rev PT1
Design:	Date: Thursday, July 18, 2024	Sheet 5 of 35	



GPIO #	TLMM Boot Configure Name	Description	Default board pull status
14	Boot_Config[0]	Auth enable: 0: no auth 1: auth is required	pull down
15	Boot_Config[1]	Fast boot (boot interface select): 0: SPI-NOR 1: eMMC 2: QSPI(4bit) 3: USB2.0	pull down
19	Boot_Config[2]		pull up
20	Boot_Config[3]	Routing ref clk Control ; 0: 48M 1: 96M	pull up
22	Boot_Config[4]	Hash in fuse (SW use only) 0: PK hash is stored in boot ROM 1: PK hash is stored in OTP	pull down
38	Boot_Config[6]	Boot ROM boot speed: 0: 24MHz 1: 400MHz	pull down
42	boot_config[7]	Clock mode select: 0: Master Mode 1: Slave Mode	pull up
44	boot_config [8]	Use Serial Num: 0: Use Serial Num 1: Use OEM ID	pull down
47	boot_config [9]	tcxo_mode: 0: xo-mode 1: tcxo-mode	pull up
51	boot_config [10]	RFA refclk frequency selection: 0: 48MHz 1: 96MHz	pull up
13	forced_usb_boot	0: Not force boot from USB 1: force boot from USB	pull down

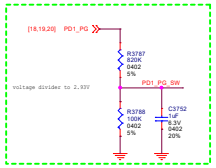


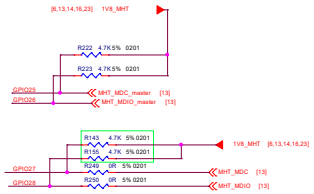
QSPI NAND

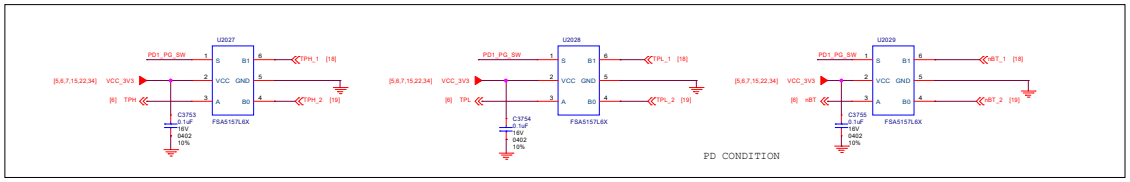
EMMC REMOVE

SFP REMOVE

TO PAGE 18 LED



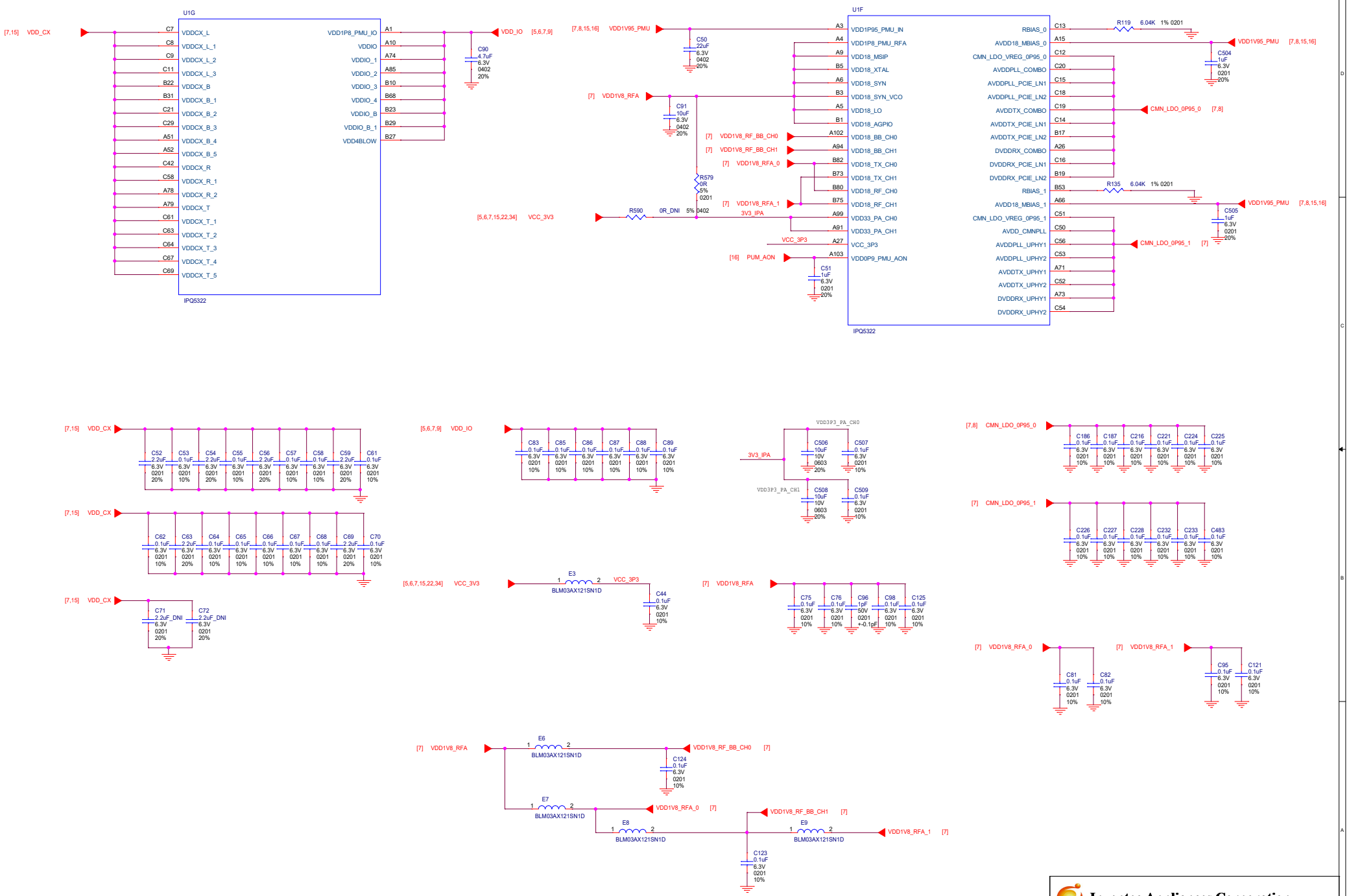




PD CONDITION

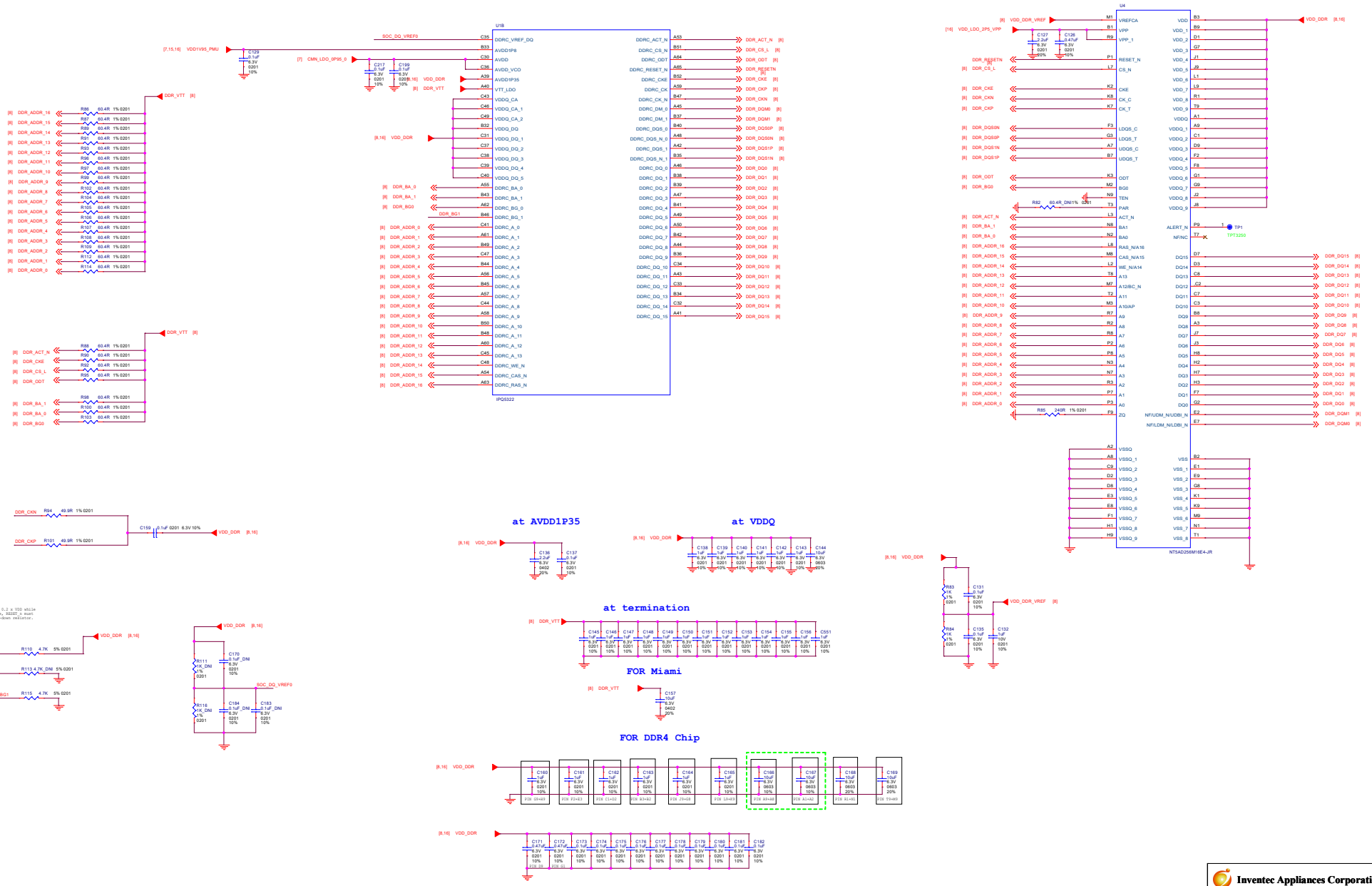
Inventec Appliances Corporation

Approval:		Title: 06_GPIO_BOOTSTRAP	
Check:		Size: D	Document Number: LUCKY 7	Rev: PT1
Design:		Date: Monday, November 29, 2004	Sheet 8 of 36

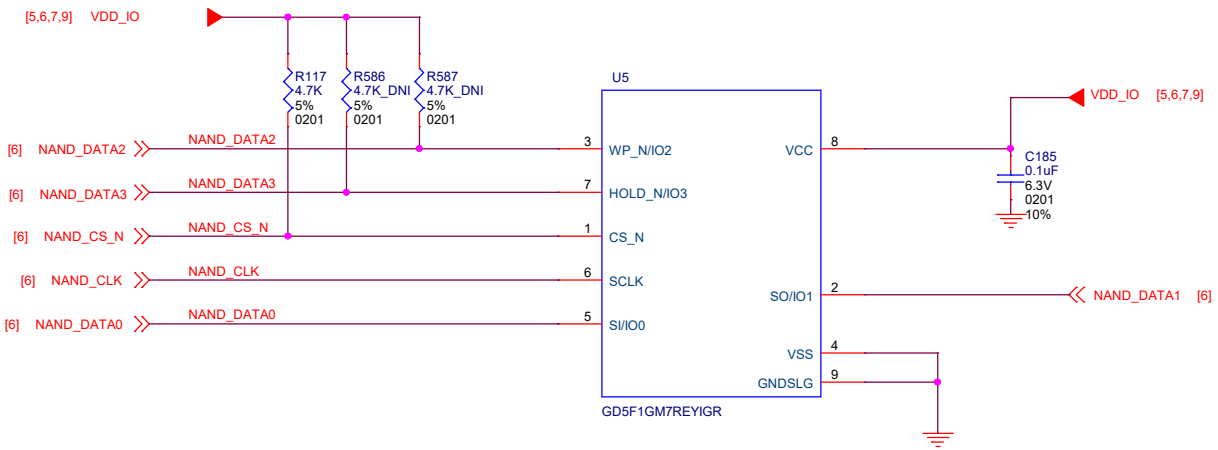


Inventec Appliances Corporation

Approval:	Title: 07_Miami_Power		
Check:	Size: C	Document Number: LUCKY 7	Rev: PT1
Design:	Date: Thursday, July 18, 2024	Sheet 7 of 35	


U18
IP05322
U4
NT5AD256M16E4-JR
at AVDD1P35
at VDDQ
at termination
FOR Miami
FOR DDR4 Chip
Inventec Appliances Corporation
08_Miami_DDR4
LUCKY 7
Thursday, July 16, 2015
8 of 35

QSPI NAND Flash_128MB



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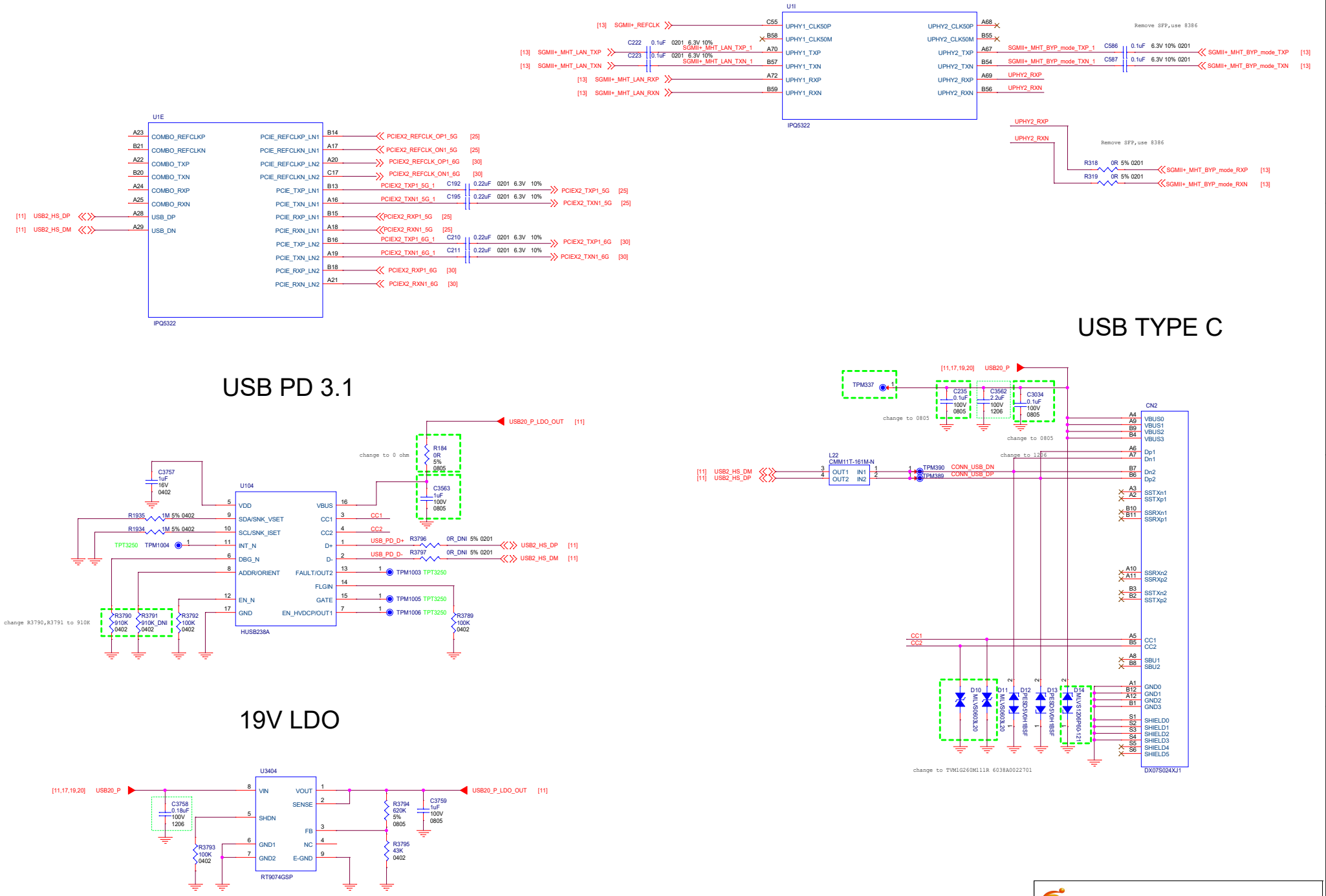
Approval:	Title: 09_Flash		
Check:	Size: B	Document Number: LUCKY 7	Rev: PT1
Design:	Date: Thursday, July 18, 2024	Sheet 9 of 35	

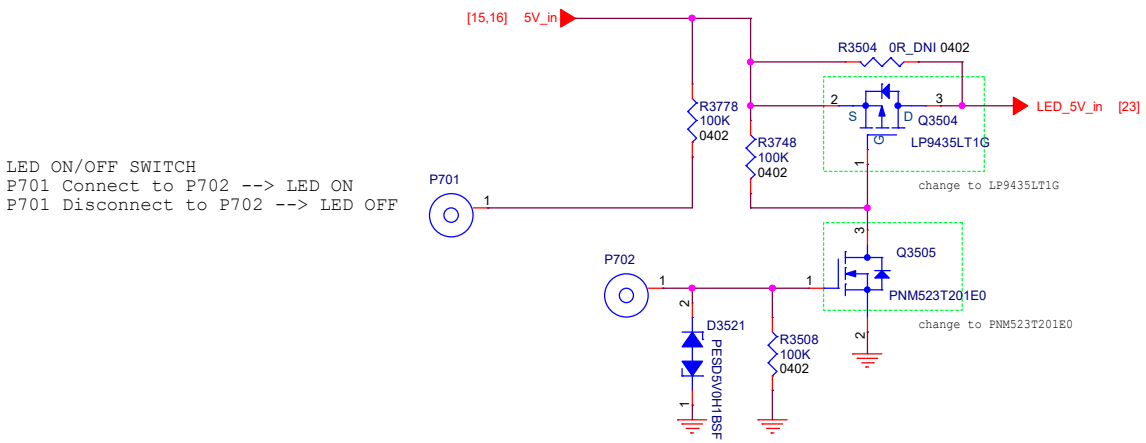
Inventec Appliances Corporation

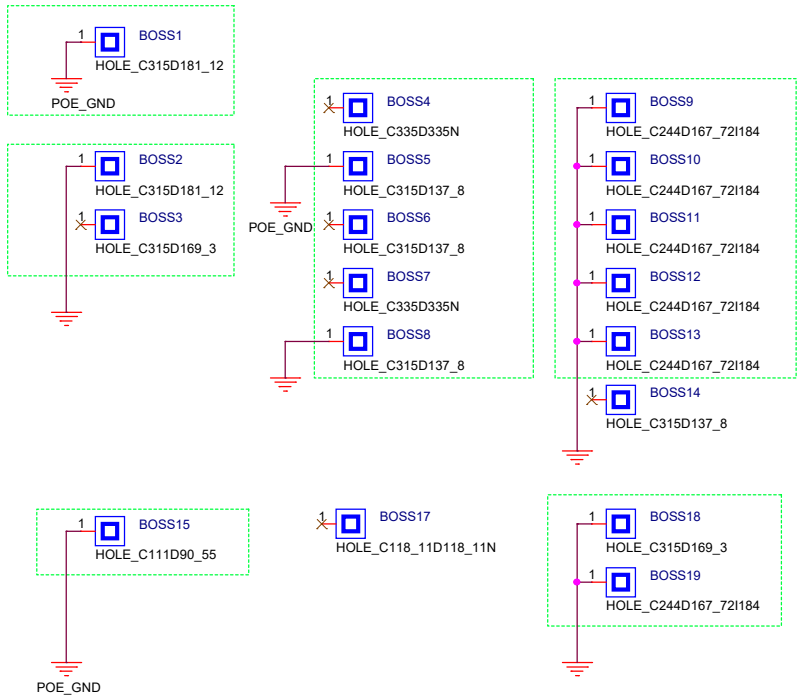
Approval:	Title	10_USB Hub_TUSB4020BI	
Check:	Size	Document Number	Rev
	C	LUCKY 7	PT1
Design:	Date: Thursday, July 18, 2024	Sheet 10 of 35	



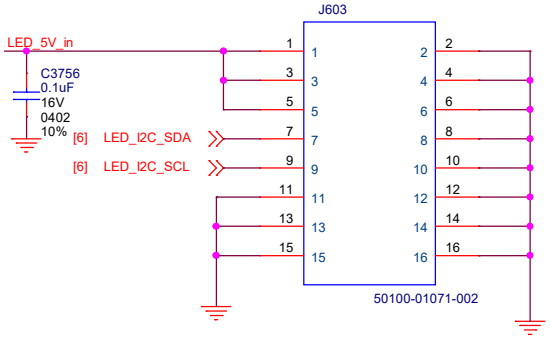
Inventec Appliances Corporation			
Approval:	Title	11_PCIE & UPHY & USB	
Check:	Size C	Document Number LUCKY 7	Rev PT1
Design:	Date: Friday, July 19, 2024	Sheet 11 of 35	

LED ON/OFF Control

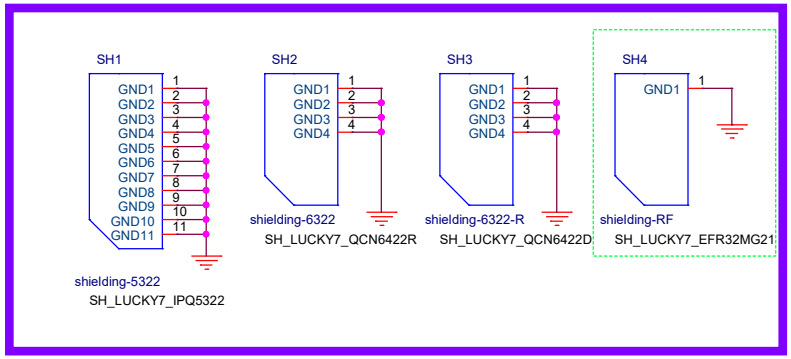


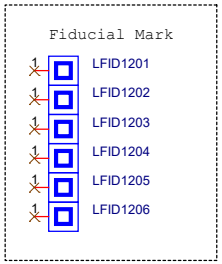


LED Board Connector



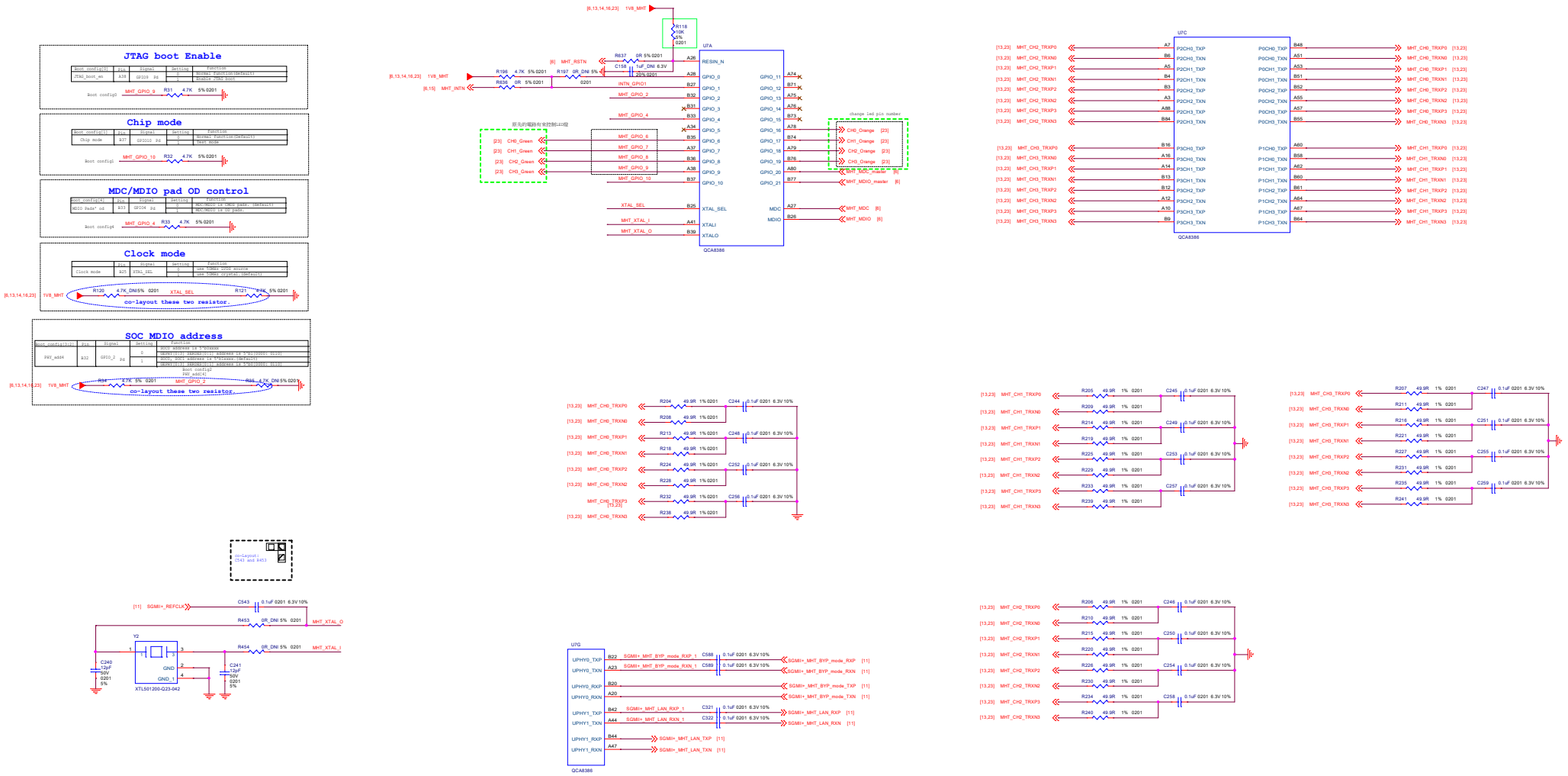
Shield Frame

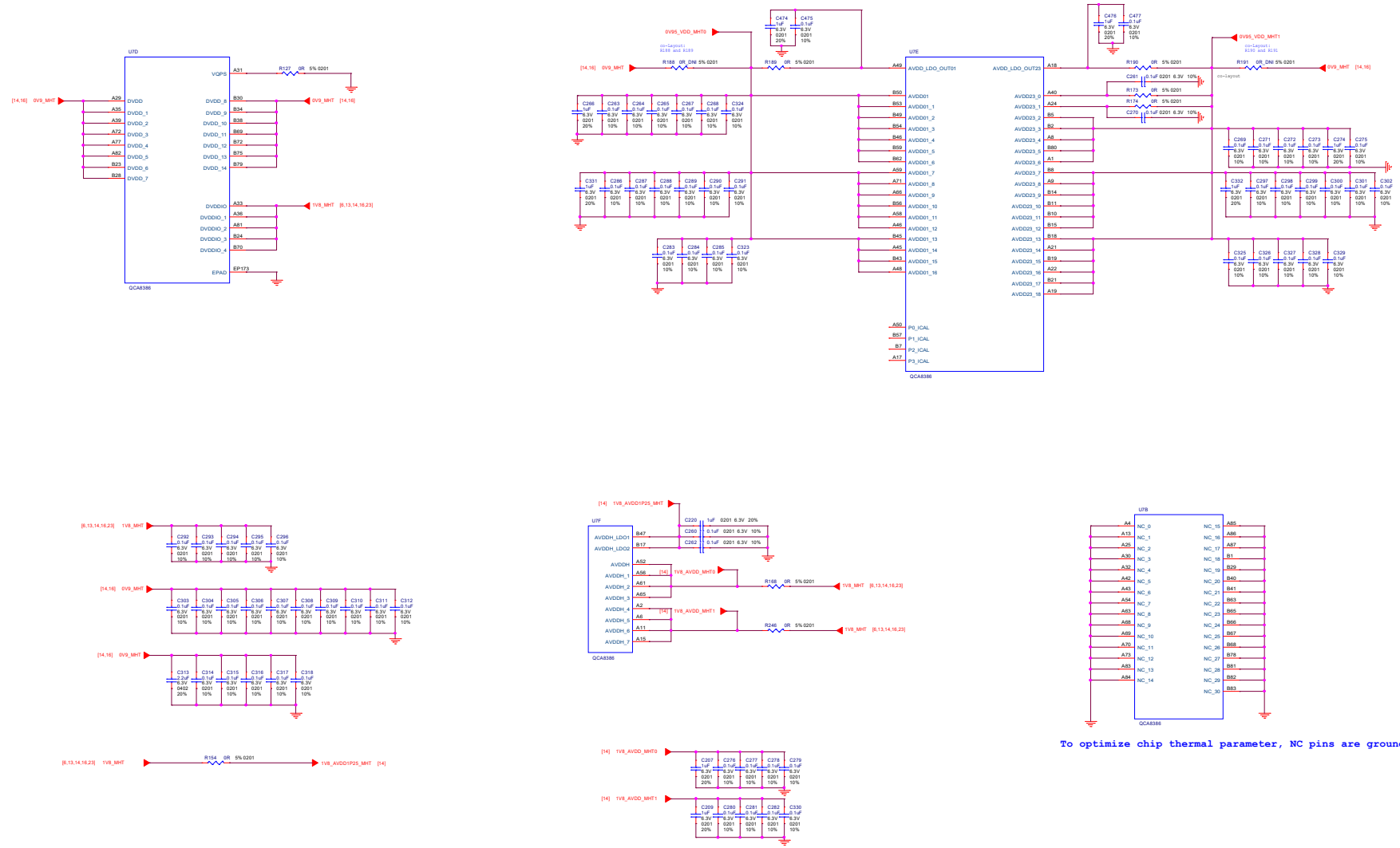




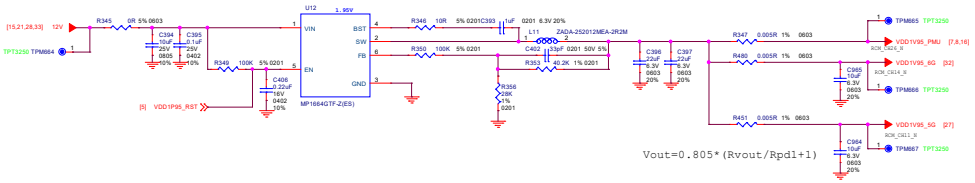
Inventec Appliances Corporation

Approval:	Title	12_LED_Board_Connector	
Check:	Size	Document Number	Rev
	B	LUCKY 7	PT1
Design:	Date: Thursday, July 18, 2024	Sheet 12 of 35	


JTAG boot Enable
Chip mode
MDC/MDIO pad OD control
Clock mode
co-layout these two resistor.
SOC MDIO address
co-layout these two resistor.
U7A
QCA8386
U7C
QCA8386
U7G
QCA8386
XTL501200-Q23-042
Inventec Appliances Corporation
13_MHT
LUCKY 7

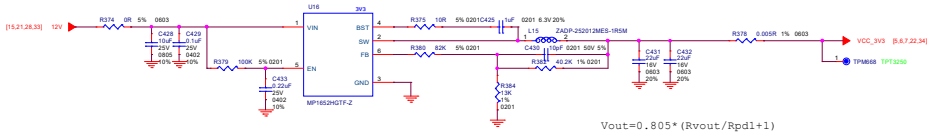


Inventec Appliances Corporation			
Approval:	Title: 14_MHT PWR		
Check:	Size: D	Document Number: LUCKY 7	Rev: P11
Design:	Date: Thursday, July 16, 2009	Sheet 14 of 35	

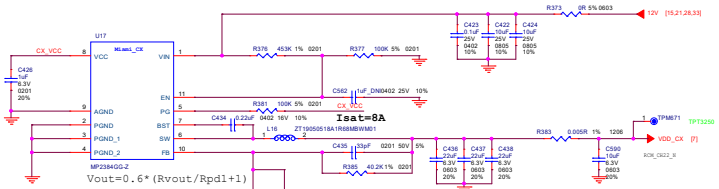


Vout=0.805*(Rvout/Rpdl+1)

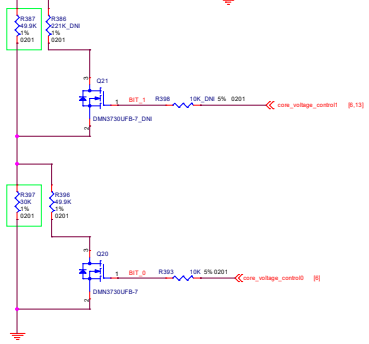
remove 3V3_PCIE



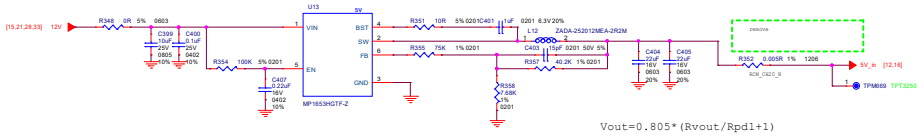
Vout=0.805*(Rvout/Rpdl+1)



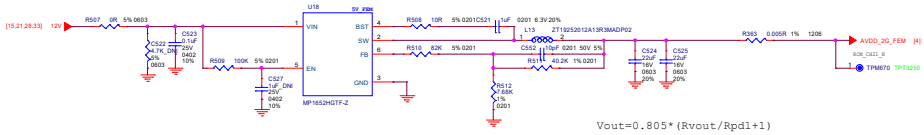
Vout=0.6*(Rvout/Rpdl+1)



config	Bit 0	Voltage
1	0	0.9
2	1	0.95



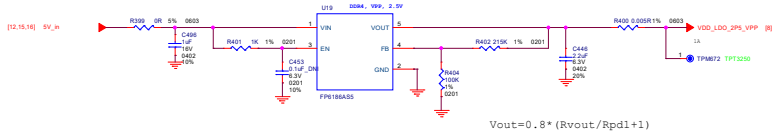
Vout=0.805*(Rvout/Rpdl+1)



Vout=0.805*(Rvout/Rpdl+1)

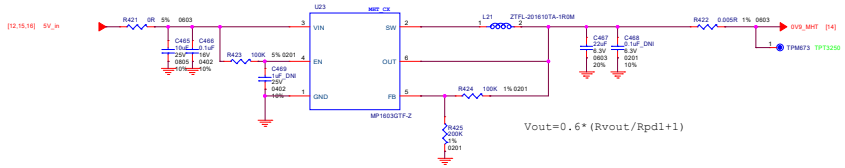
Inventec Appliances Corporation

Approval:		Title: 15_12 Vin Power Regulator	
Check:		Size: D	Document Number: LUCKY 7	Rev: PT1
Design:		Date: Monday, November 25, 2024	Sheet 15 of 35	

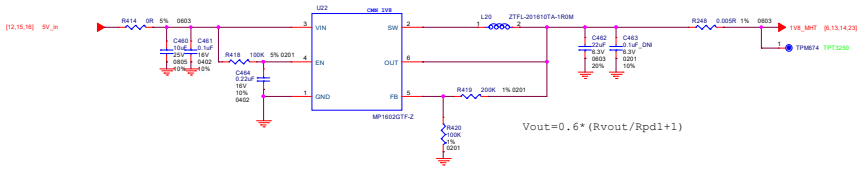


Vout=0.8*(Rvout/Rpdl+1)

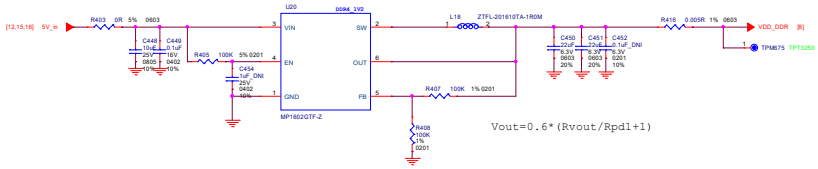
remove 3V3_SFP



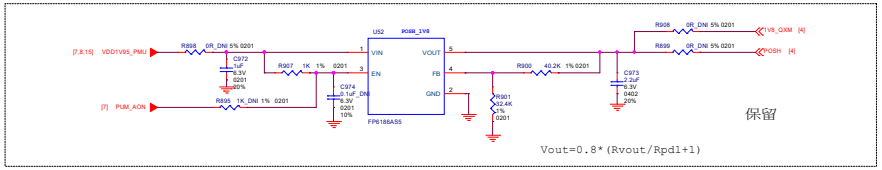
Vout=0.6*(Rvout/Rpdl+1)



Vout=0.6*(Rvout/Rpdl+1)



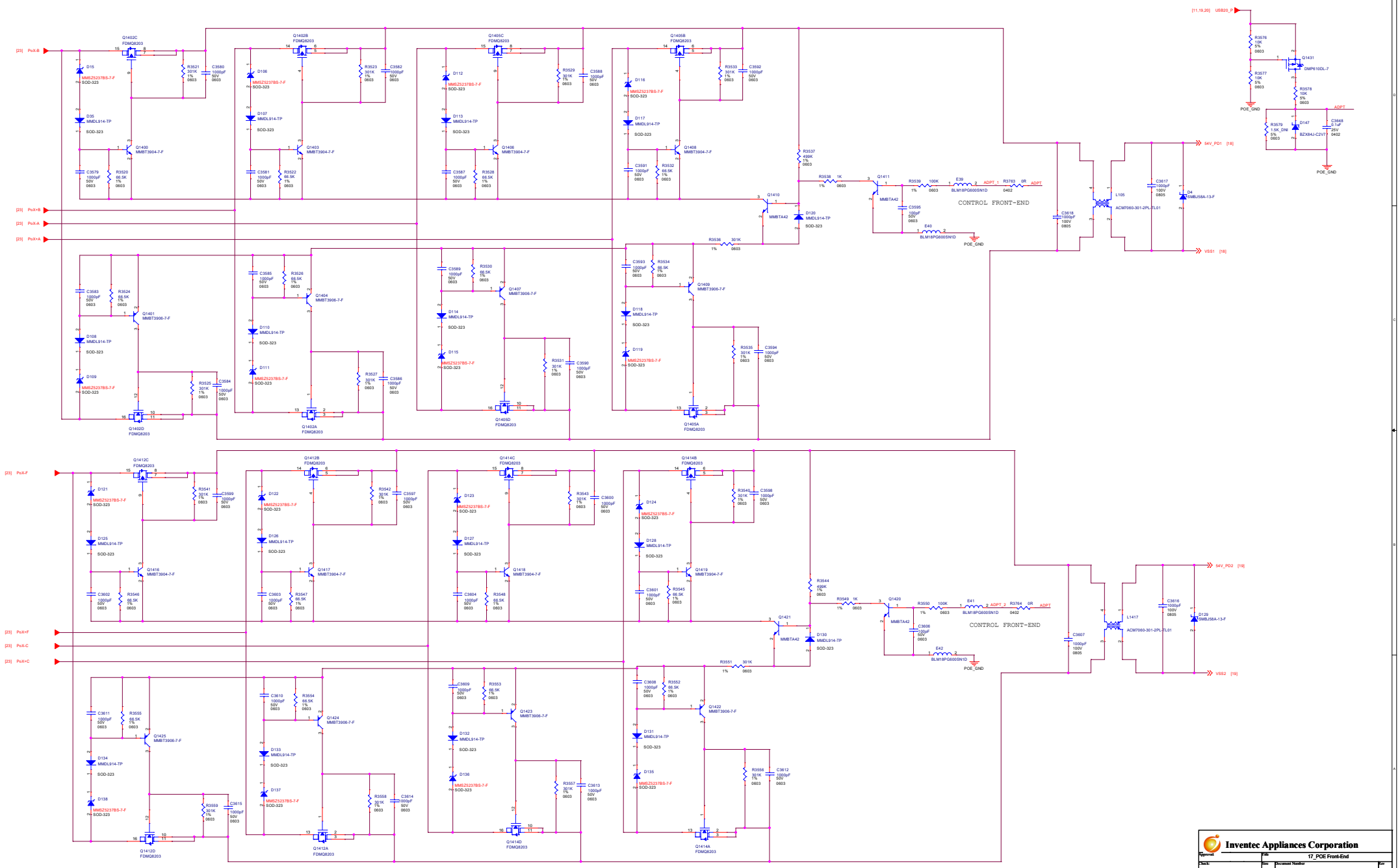
Vout=0.6*(Rvout/Rpdl+1)



保留

Vout=0.8*(Rvout/Rpdl+1)

Inventec Appliances Corporation			
Approval:	Title: 16_5 Vin Power Regulator		
Check:	Size: D	Document Number: LUCKY 7	Rev: PT1
Design:	Date: Thursday, July 16, 2020	Sheet 16 of 36	


[23] PoX-B
[23] PoX+B
[23] PoX-A
[23] PoX+A
[23] PoX-F
[23] PoX+F
[23] PoX-C
[23] PoX+C
[11,19,20] USB20_P
54V_PD1 [18]
VBS1 [18]
54V_PD2 [19]
VBS2 [19]
CONTROL FRONT-END
CONTROL FRONT-END
POE_GND
ADPT
Q1402C FDMQ8203
Q1402B FDMQ8203
Q1405C FDMQ8203
Q1405B FDMQ8203
Q1412C FDMQ8203
Q1412B FDMQ8203
Q1414C FDMQ8203
Q1414B FDMQ8203
Q1402D FDMQ8203
Q1402A FDMQ8203
Q1405D FDMQ8203
Q1405A FDMQ8203
Q1412D FDMQ8203
Q1412A FDMQ8203
Q1414D FDMQ8203
Q1414A FDMQ8203
Q1400 MMBT3904-7-F
Q1403 MMBT3904-7-F
Q1406 MMBT3904-7-F
Q1408 MMBT3904-7-F
Q1411 MMBTA42
Q1410 MMBTA42
Q1416 MMBT3904-7-F
Q1417 MMBT3904-7-F
Q1418 MMBT3904-7-F
Q1419 MMBT3904-7-F
Q1420 MMBTA42
Q1421 MMBTA42
Q1431 DMP610DL-7
L105 ACM7060-301-2PL-TL01
L1417 ACM7060-301-2PL-TL01
D4 SMBJ58A-13-F
D129 SMBJ58A-13-F
D147 BZX84J-C2V7
E39 BLM18PG600SN1D
E40 BLM18PG600SN1D
E41 BLM18PG600SN1D
E42 BLM18PG600SN1D
R3537 499K 1% 0603
R3538 1K 1% 0603
R3539 100K 1% 0603
R3763 0R 0402
R3536 301K 1% 0603
R3551 301K 1% 0603
R3544 499K 1% 0603
R3549 1K 1% 0603
R3550 100K 1% 0603
R3764 0R 0402
C3848 0.1uF 25V 0402
C3617 1000pF 100V 0805
C3618 1000pF 100V 0805
C3616 1000pF 100V 0805
C3607 1000pF 100V 0805
Inventec Appliances Corporation
Approval:
Check:
Design:
Size: D
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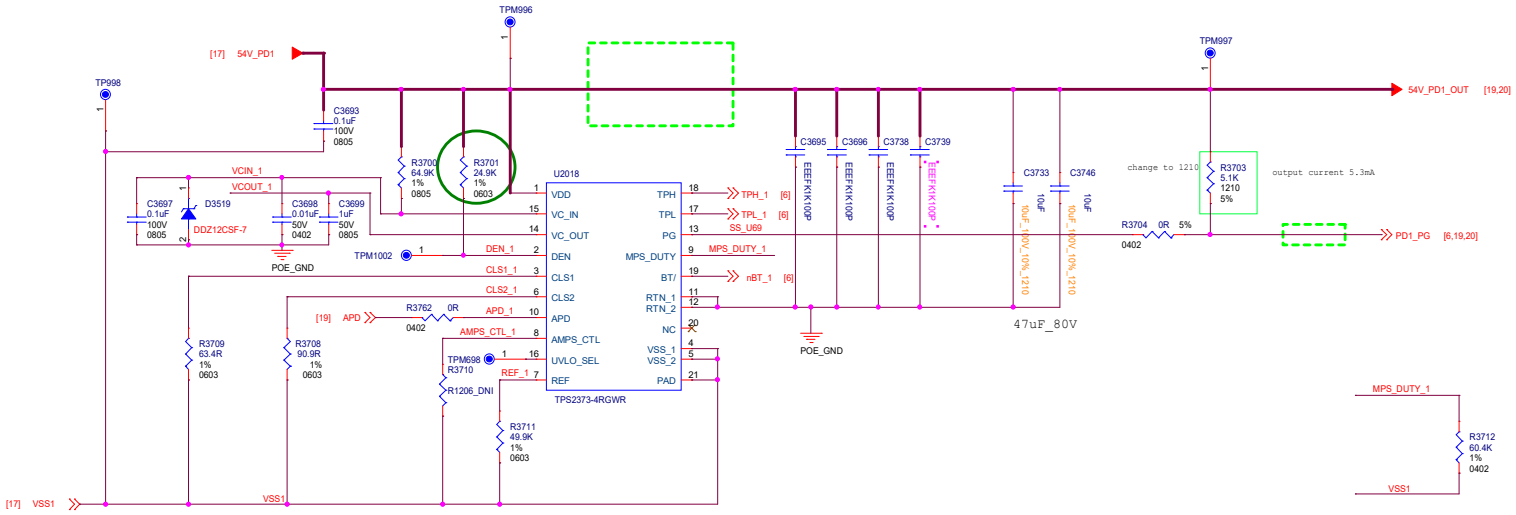
Rev: P71
Date: Thursday, July 16, 2009
Sheet 17 of 35

PoE PD 1 TPS2373

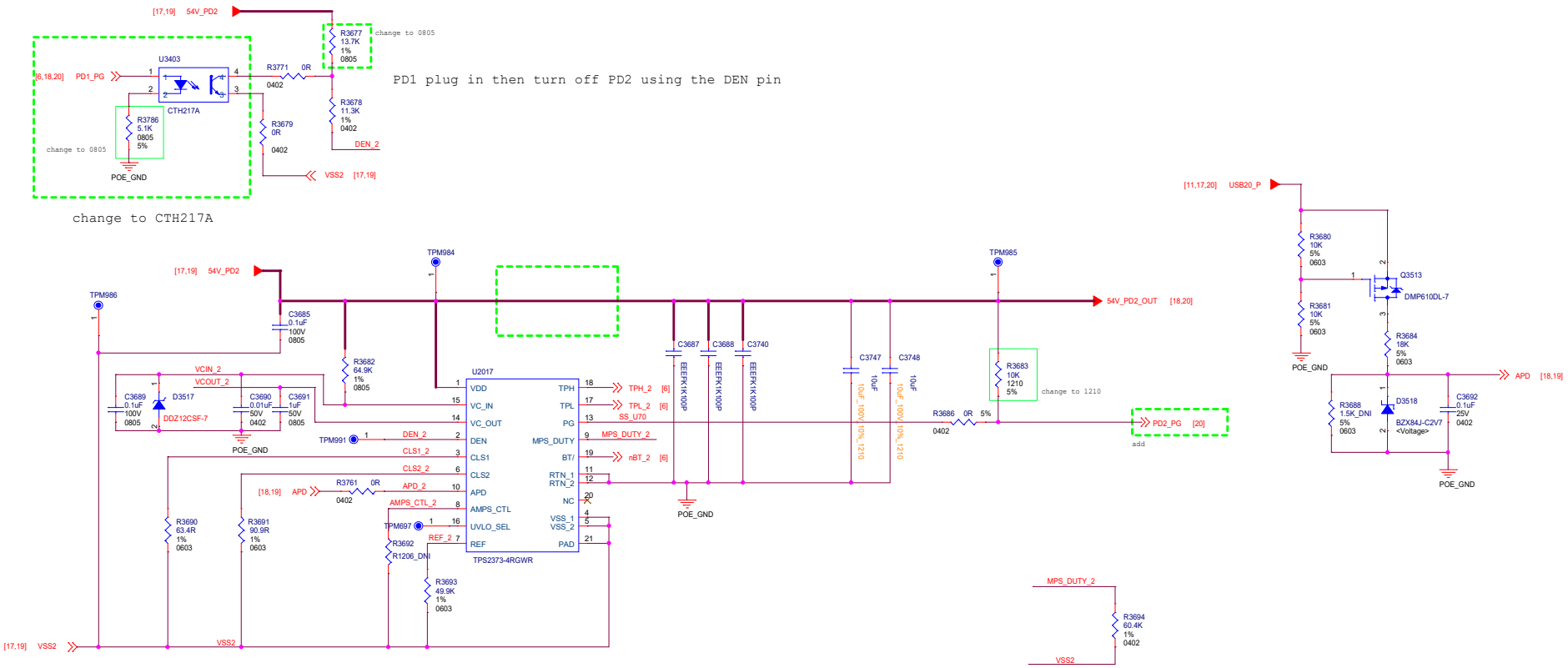


USB Adapter plug in PoE Port 1 plug in PoE Port 2 plug in	PoE PD 1 Disable PoE PD 2 Disable
USB Adapter unplugged PoE Port 1 plug in PoE Port 2 plug in	PoE PD 1 Enable PoE PD 2 Disable
USB Adapter unplugged PoE Port 1 unplugged PoE Port 2 plug in	PoE PD 1 Disable PoE PD 2 Enable

Inventec Appliances Corporation

Approval:	Title: 18_PoE PD1_TPS2373		
Check:	Size: C	Document Number: LUCKY 7	Rev: PT1
Design:	Date: Monday, November 25, 2024	Sheet 18 of 35	

PoE PD 2 TPS2373



USB Adapter plug in PoE Port 1 plug in PoE Port 2 plug in	PoE PD 1 Disable PoE PD 2 Disable
USB Adapter unplugged PoE Port 1 plug in PoE Port 2 plug in	PoE PD 1 Enable PoE PD 2 Disable
USB Adapter unplugged PoE Port 1 unplugged PoE Port 2 plug in	PoE PD 1 Disable PoE PD 2 Enable

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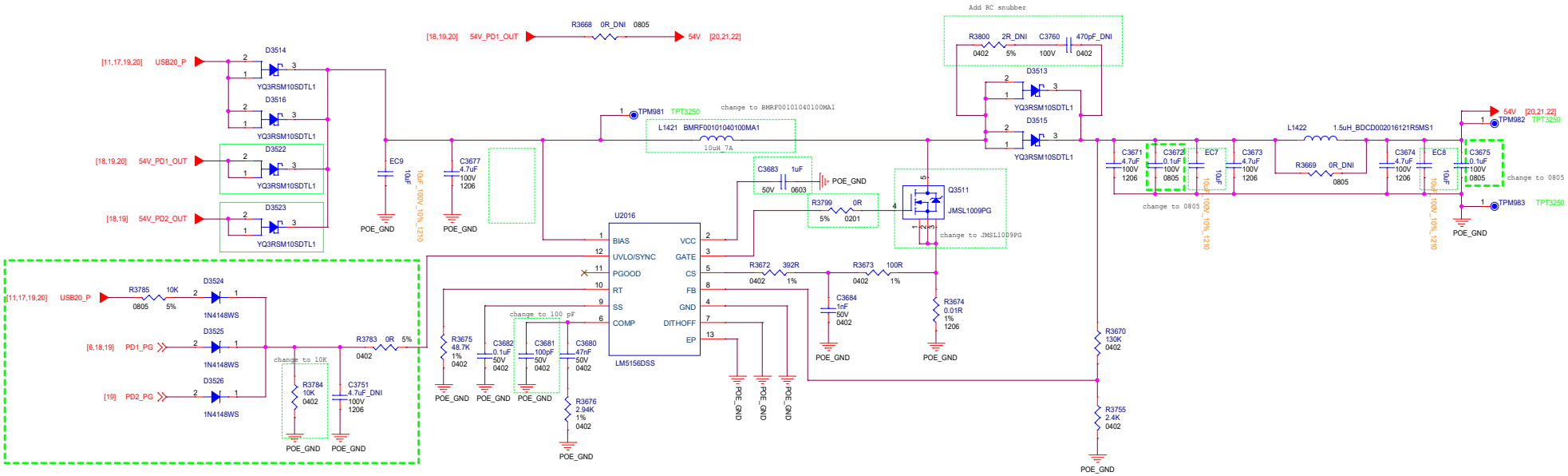
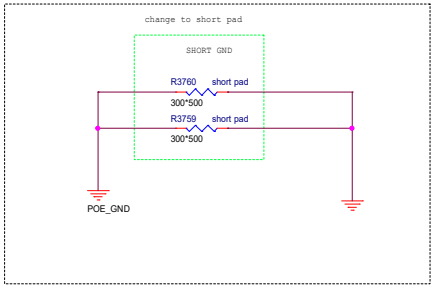
Approval:	Title: 19_PoE PD2_TPS2373		
Check:	Size: C	Document Number: LUCKY 7	Rev: PT1
Design:	Date: Monday, November 25, 2024	Sheet 19 of 35	

Boost Converter_LM5156DSSR

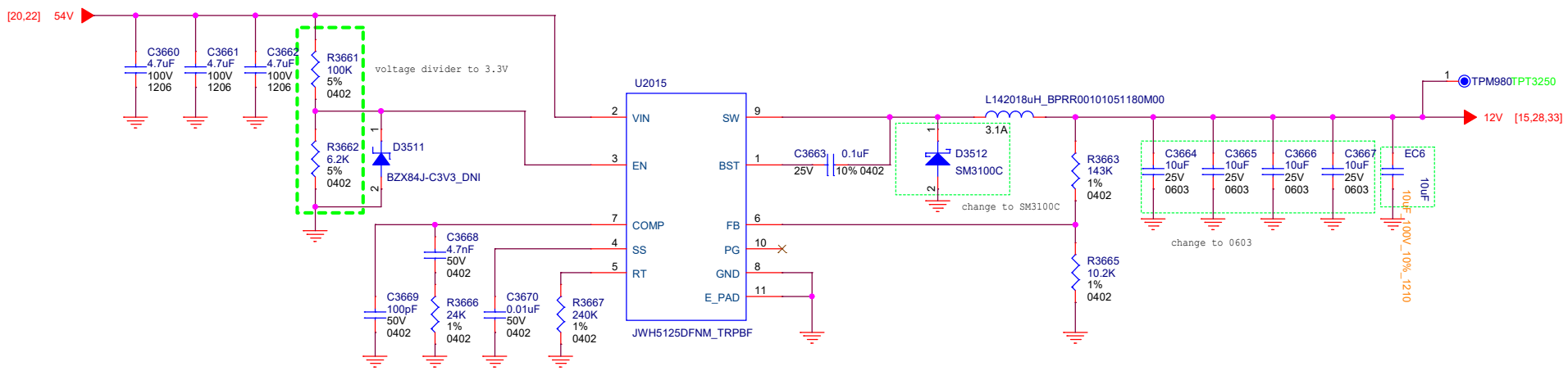




Inventec Appliances Corporation

Approval:	Title: 20_Boost Converter_LM5156DSSR		
Check:	Size: C	Document Number: LUCKY 7	Rev: PT1
Design:	Date: Monday, November 25, 2024	Sheet 20 of 35	

12V Buck Converter JWH5125



Inventec Appliances Corporation			
Approval:	Title: 21_12V Buck Converter_JWH5125		
Check:	Size: B	Document Number: LUCKY 7	Rev: PT1
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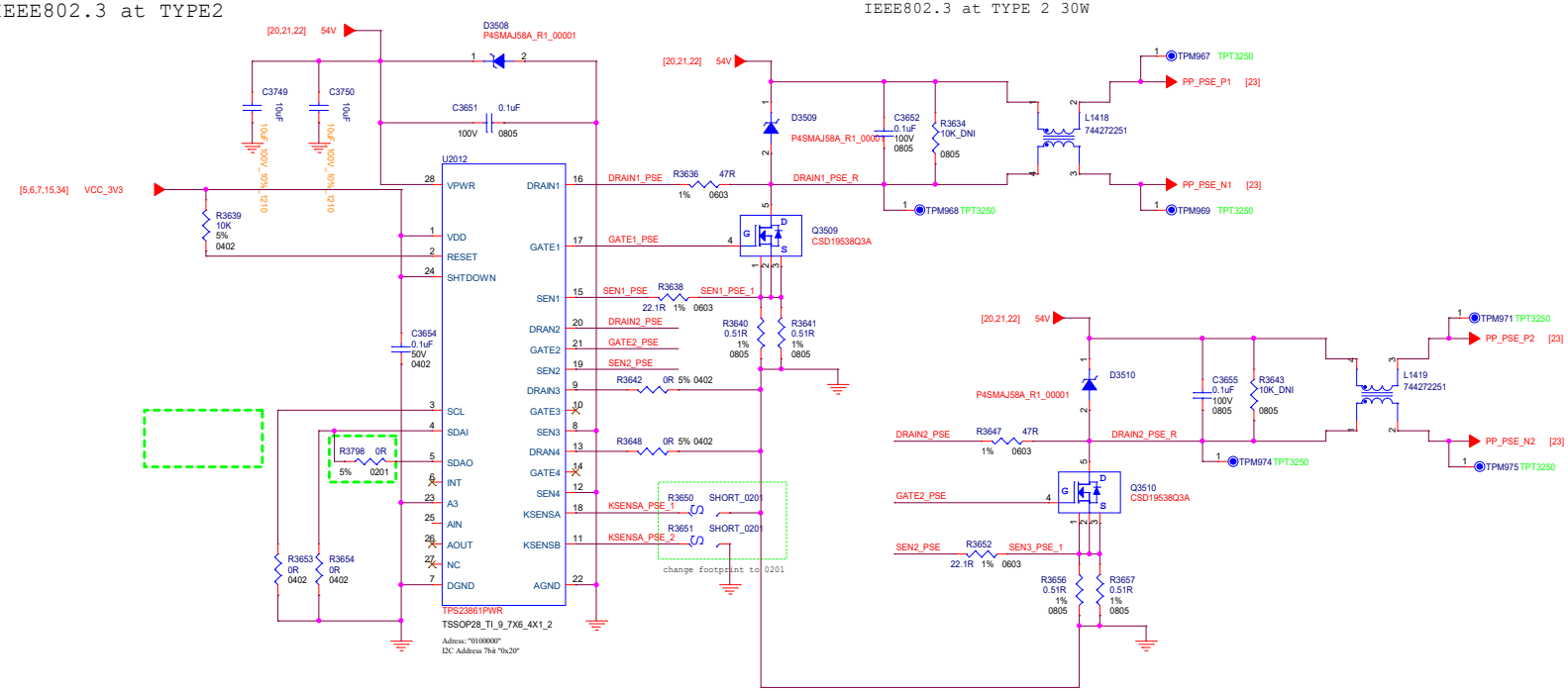
IEEE802.3 at TYPE2

IEEE802.3 at TYPE 2 30W



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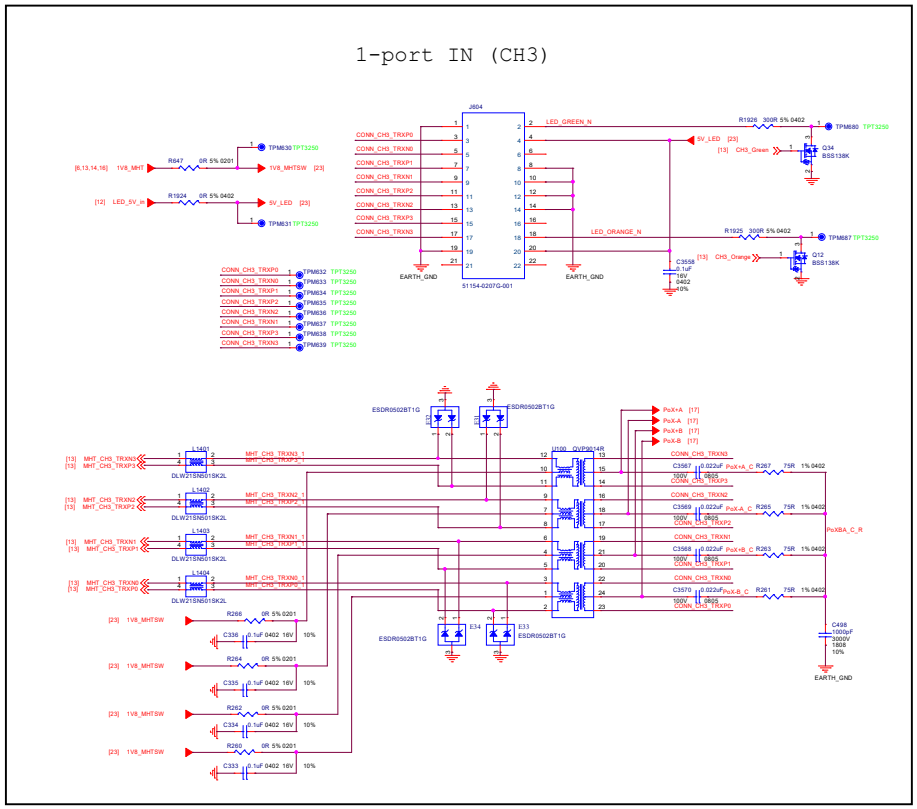
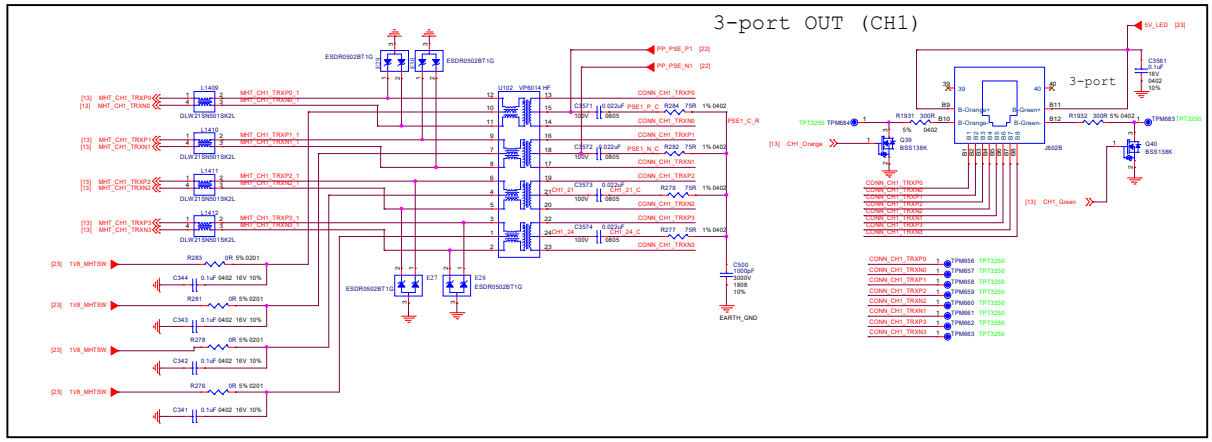
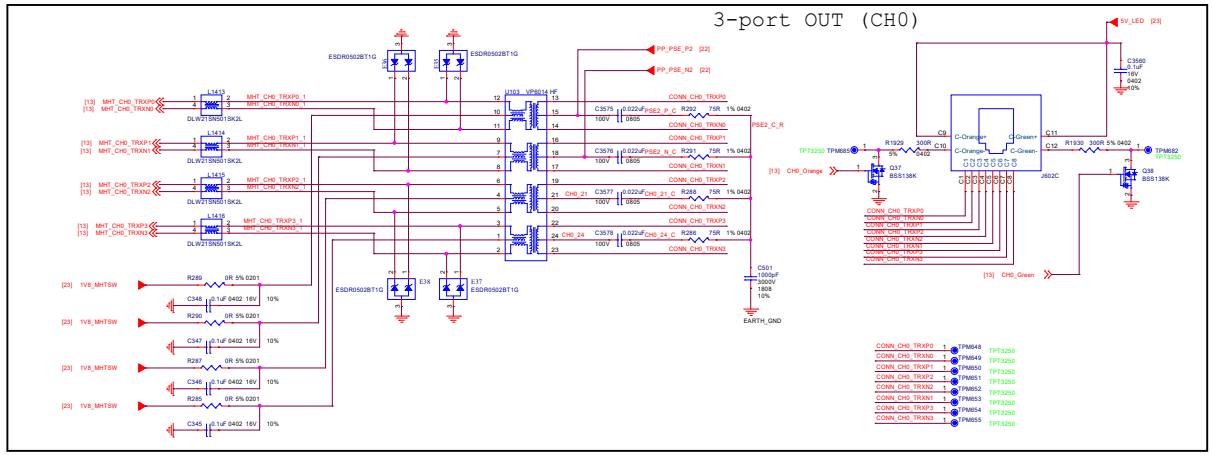
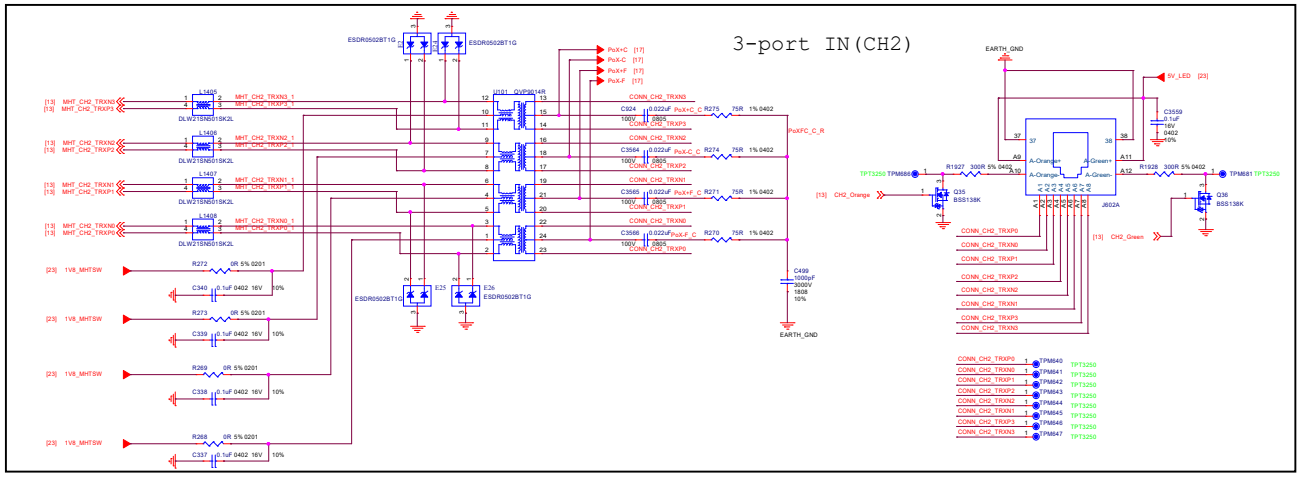
Approval:	Title	22_PoE PSE_TPS23861	
Check:	Size C	Document Number LUCKY 7	Rev PT1
Design:	Date: Thursday, July 18, 2024	Sheet 22 of 35	









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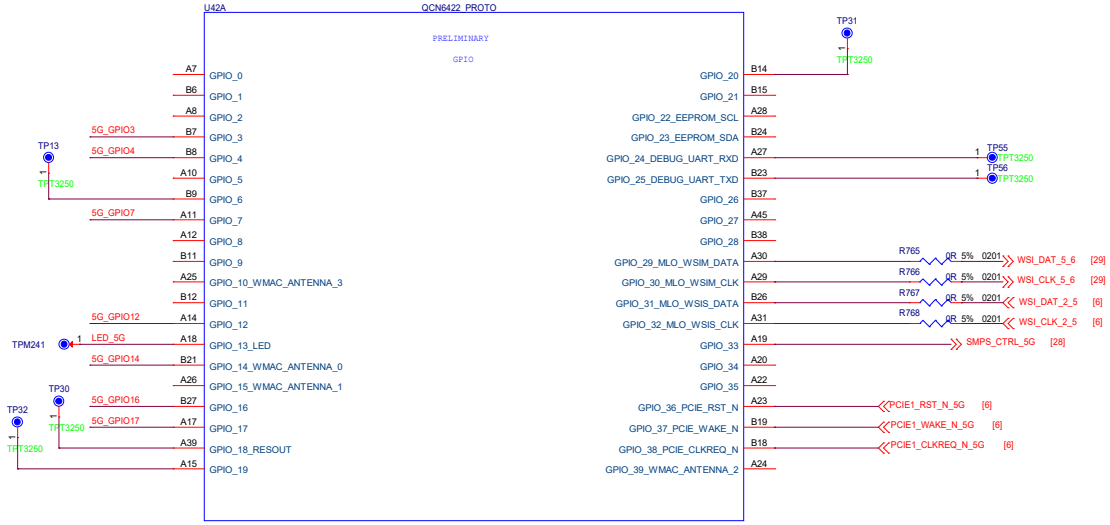
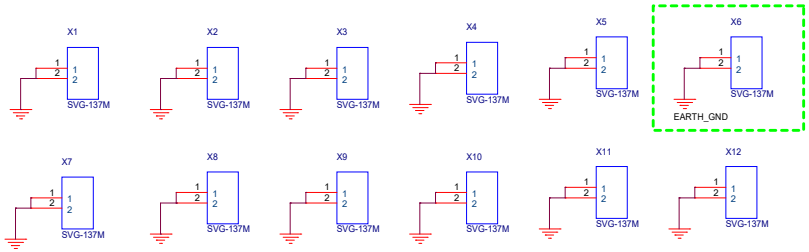
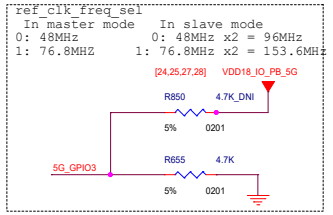
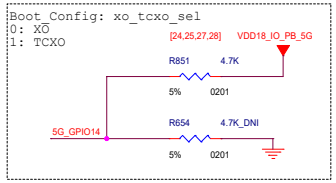
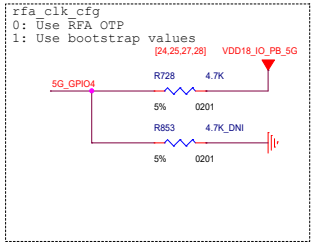
Approval:		Title: 23_RJ45&Transfromer	
Check:		Size: D	Document Number: LUCKY 7	Rev: P71
Design:		Date: Friday, July 26, 2024	Sheet 23 of 35

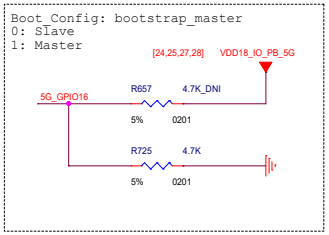


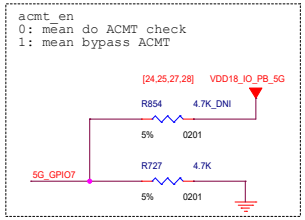


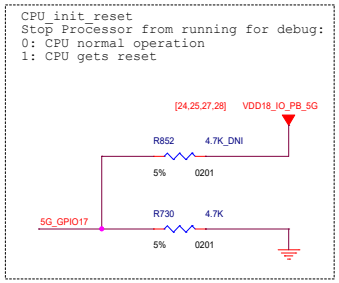


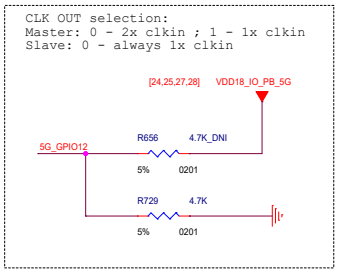


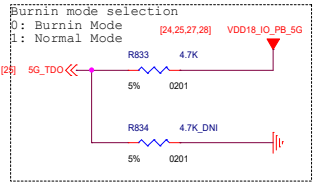












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Approval:	Title: 24_5G_Pebble GPIO		
Check:	Size: C	Document Number: LUCKY 7	Rev: PT1
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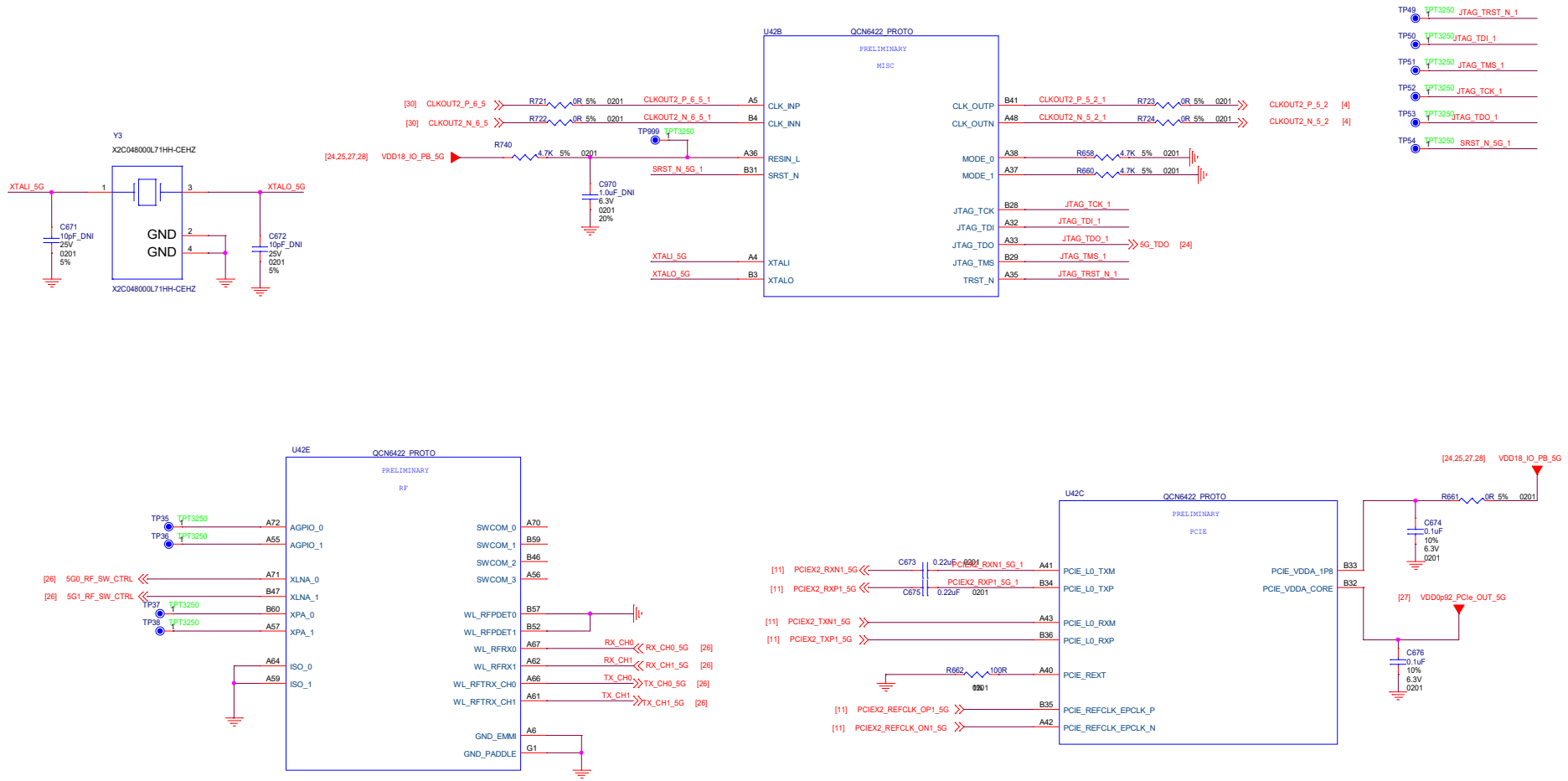
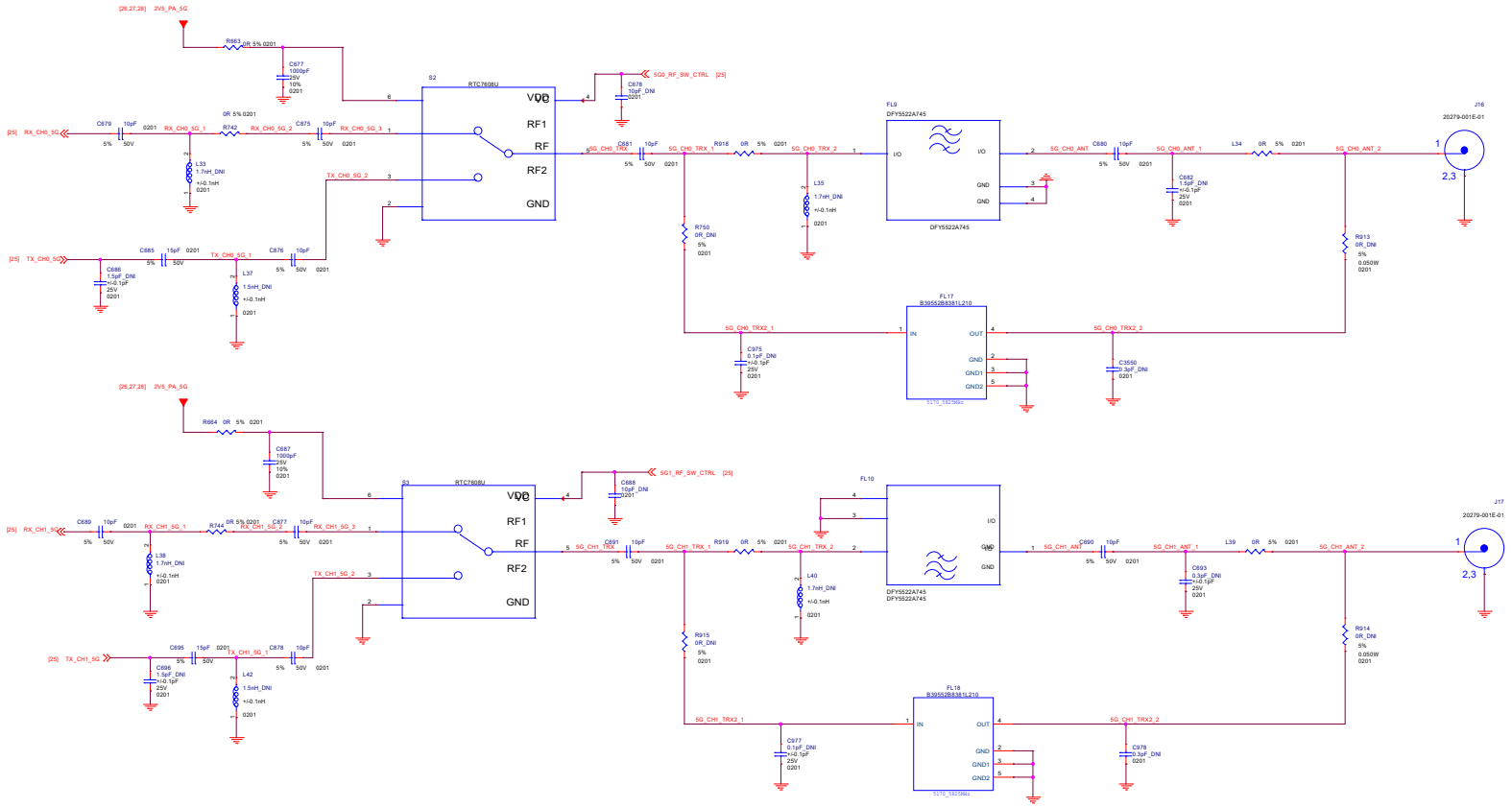


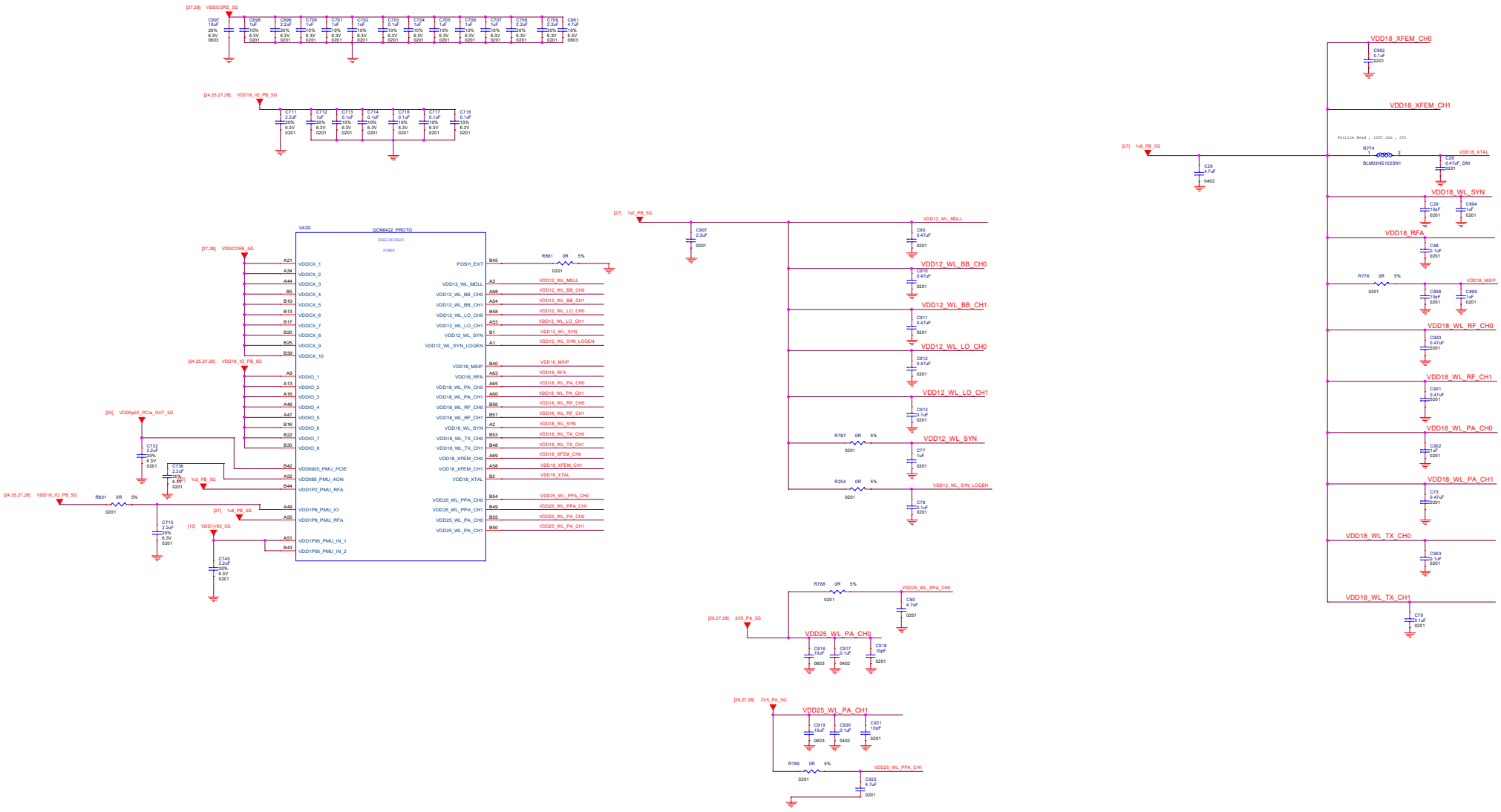
Inventec Appliances Corporation

Approval:	Title: 25_5G RF & Clock & PCIE		
Check:	Size: C	Document Number: LUCKY 7	Rev: PT1
Design:	Date: Thursday, July 18, 2024	Sheet 25 of 35	



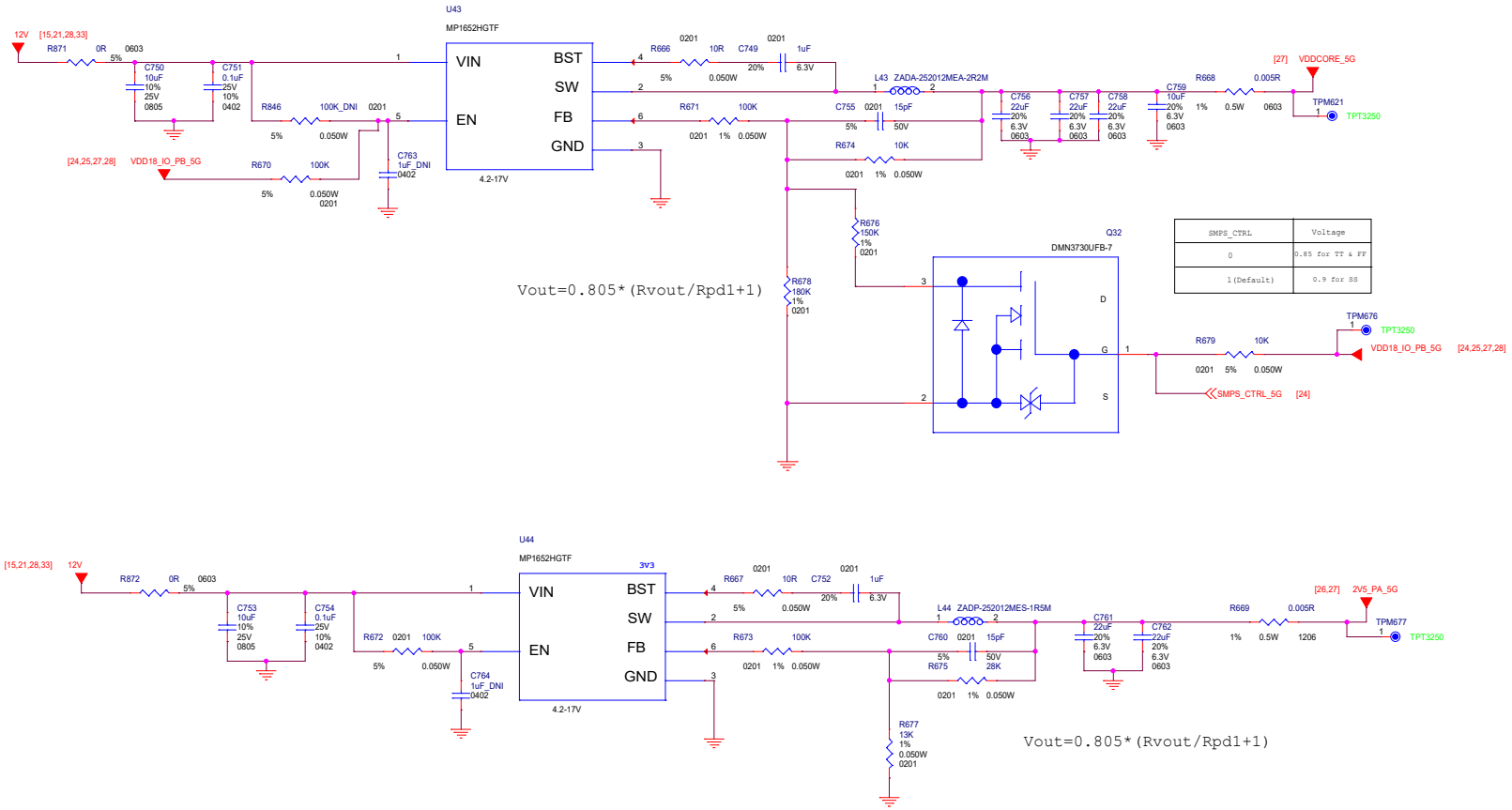
Inventec Appliances Corporation

Approval:	Title: 28_5G-RF Front-end		
Check:	Size: D	Document Number: LUCKY 7	Rev: P11
Design:	Date: Thursday, July 18, 2024	Sheet 28 of 35	



Inventec Appliances Corporation

Approval:	Title: 27_5G_power rail & SOC		
Check:	Size: D	Document Number: LUCKY 7	Rev: P11
Design:	Date: Thursday, July 16, 2015	Sheet 27 of 35	



SMPS_CTRL	Voltage
0	0.85 for TT & FF
1(Default)	0.9 for SS

Inventec Appliances Corporation

Approval:	Title: 28_5G_POWER		
Check:	Size: C	Document Number: LUCKY 7	Rev: PT1
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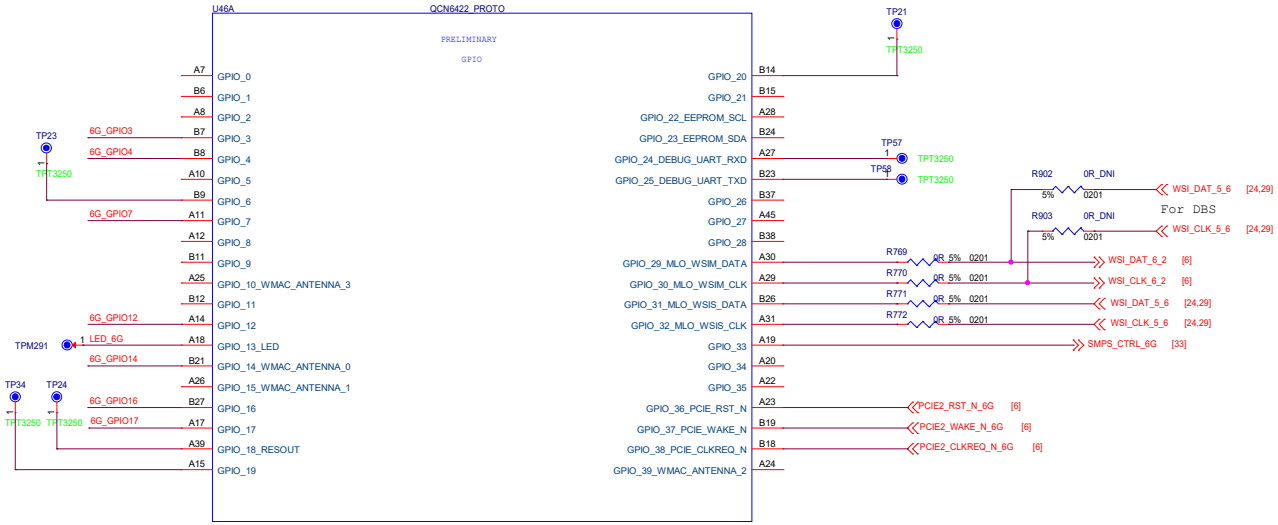
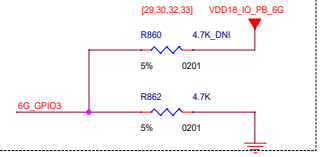
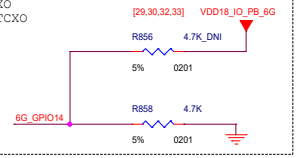


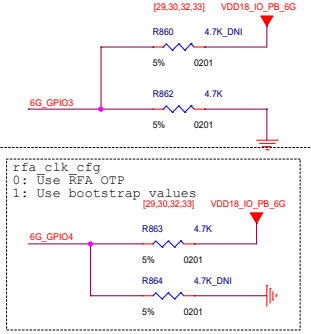
ref_clk_freq_sel
In master mode In slave mode
0: 48MHz 0: 48MHz x2 = 96MHz
1: 76.8MHZ 1: 76.8MHz x2 = 153.6MHz



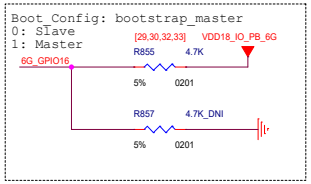
Boot_Config: xo_tcxo_sel
0: XO
1: TCXO



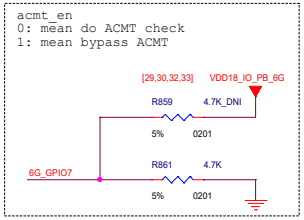
rfa_clk_cfg
0: Use RFA OTP
1: Use bootstrap values



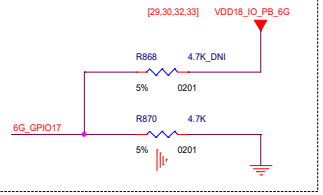
Boot_Config: bootstrap_master
0: Slave
1: Master



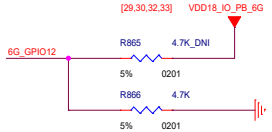
acmt_en
0: mean do ACMT check
1: mean bypass ACMT



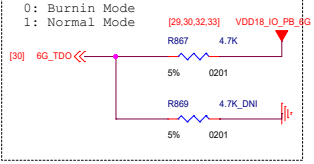
CPU_init_reset
Stop Processor from running for debug:
0: CPU normal operation
1: CPU gets reset



CLK OUT selection:
Master: 0 - 2x clkin ; 1 - 1x clkin
Slave: 0 - always 1x clkin



Burnin mode selection
0: Burnin Mode
1: Normal Mode



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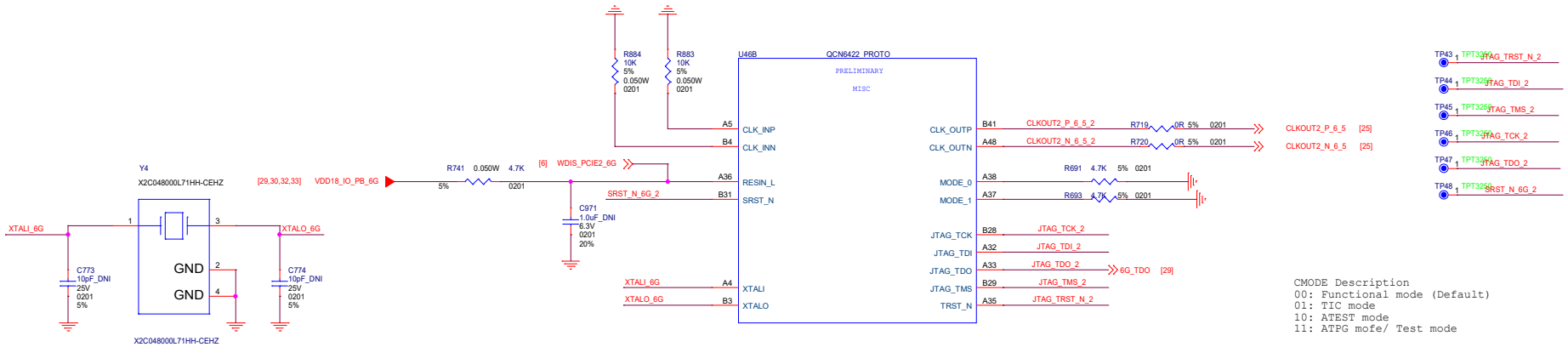
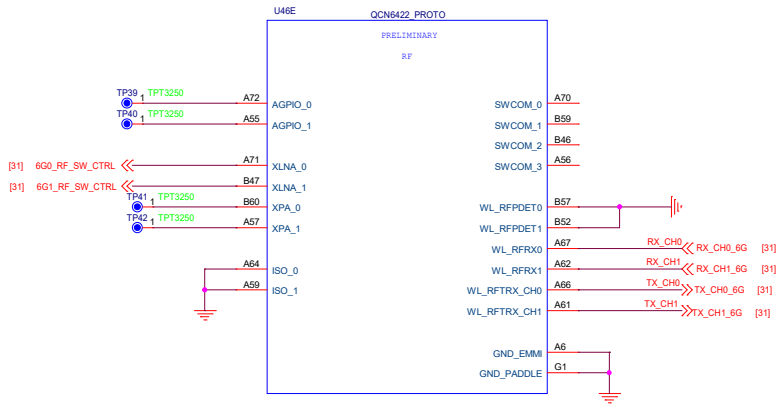
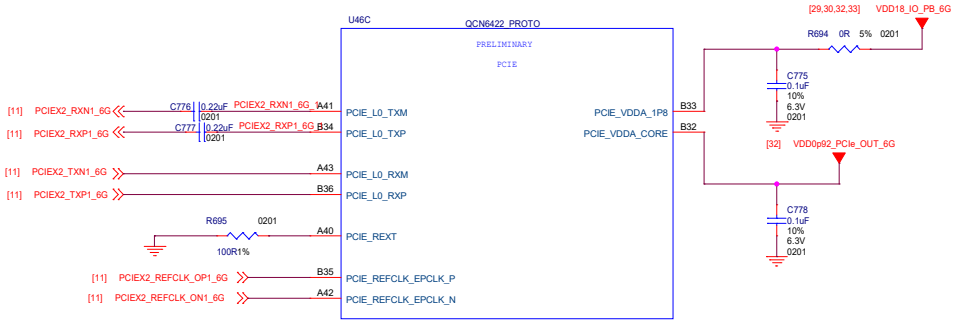
Approval:	Title: 29_6G_Pebble GPIO		
Check:	Size: C	Document Number: LUCKY 7	Rev: PT1
Design:	Date: Thursday, July 18, 2024	Sheet 29 of 35	



CMODE Description
00: Functional mode (Default)
01: TIC mode
10: ATEST mode
11: ATPG mofe/ Test mode





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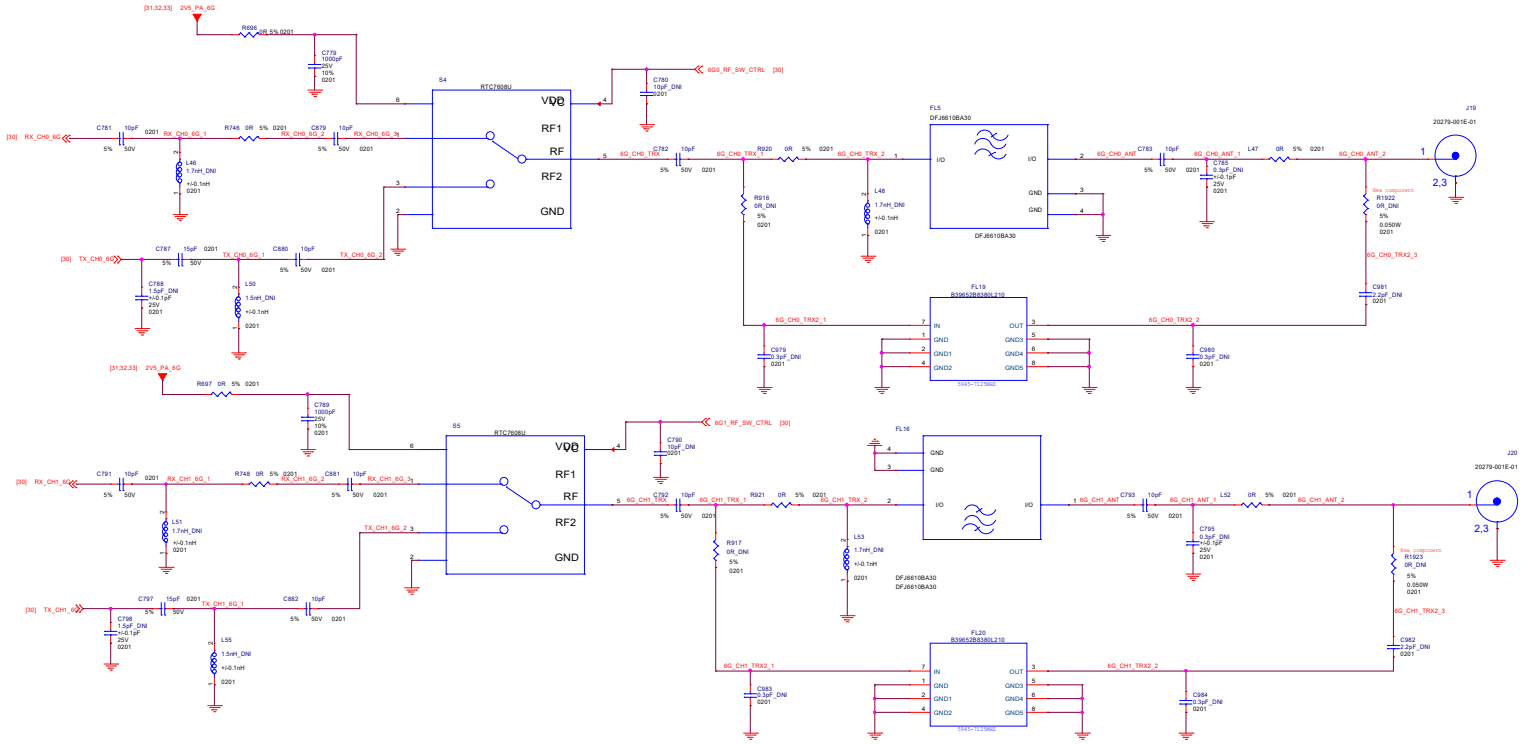
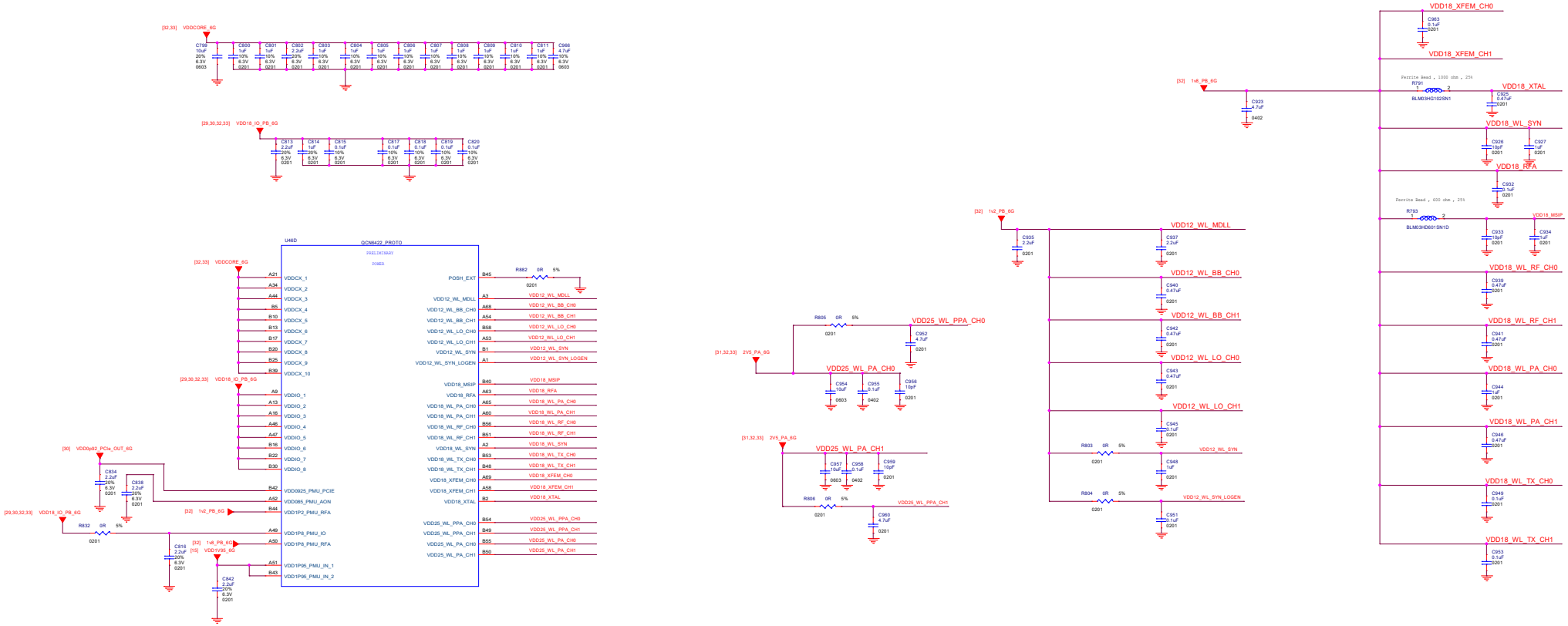
Approval:	Title: 30_6G RF & Clock & PCIE		
Check:	Size: C	Document Number: LUCKY 7	Rev: PT1
Design:	Date: Thursday, July 18, 2024	Sheet 30 of 35	



Inventec Appliances Corporation

Approval:	Title: 31_6G-RF Front-end		
Check:	Size: D	Document Number: LUCKY 7	Rev: P11
Design:	Date: Thursday, July 16, 2015	Sheet 31 of 35	



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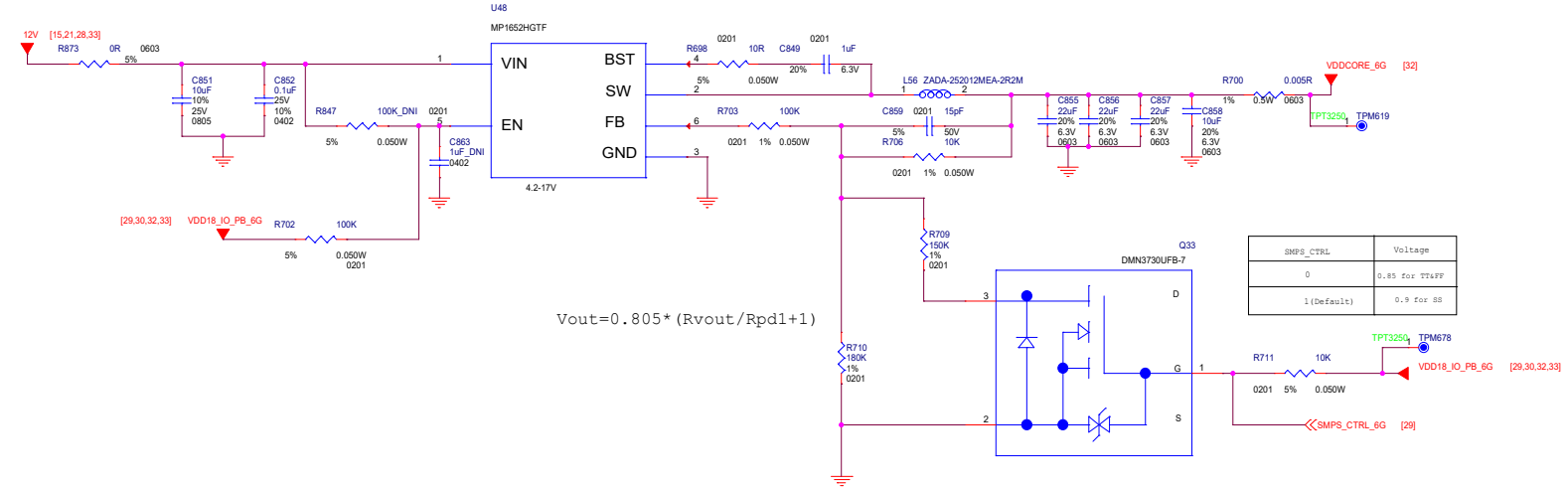
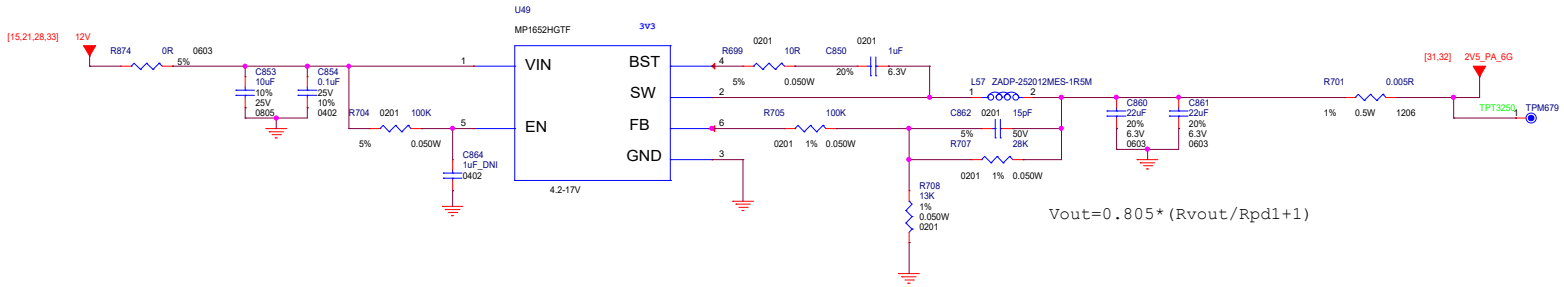
Approval:	Title: 32_6G_power rail & SOC		
Check:	Size: D	Document Number: LUCKY 7	Rev: PT1
Design:	Date: Thursday, July 16, 2020	Sheet 32 of 35	



SMPS_CTRL	Voltage
0	0.85 for TT&FF
1(Default)	0.9 for SS



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Approval:	Title: 33_6G_POWER		
Check:	Size: C	Document Number: LUCKY 7	Rev: PT1
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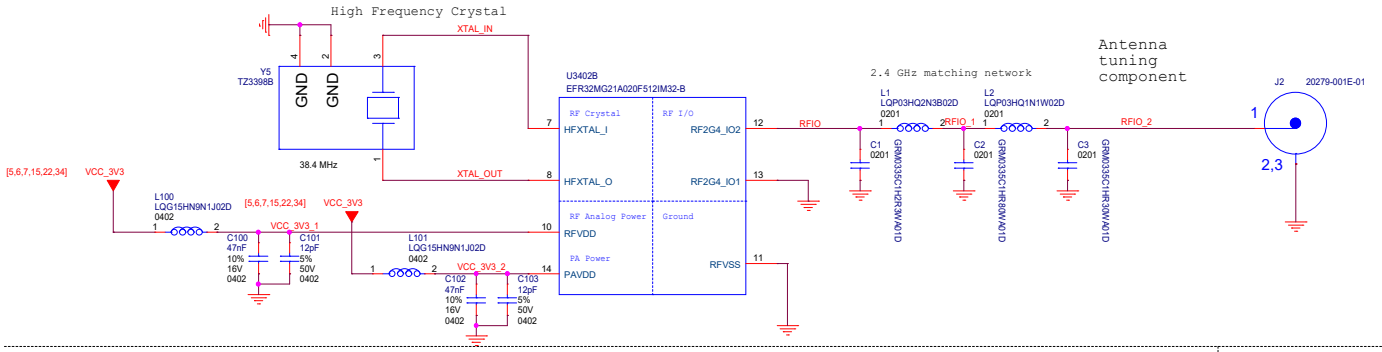
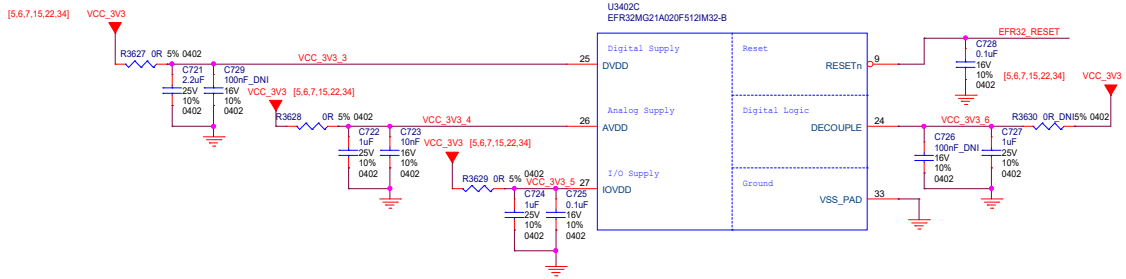
Antenna & Radio Interface

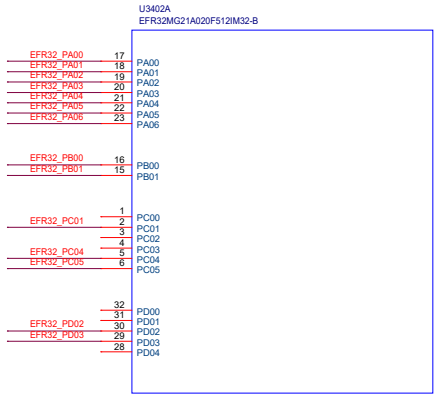


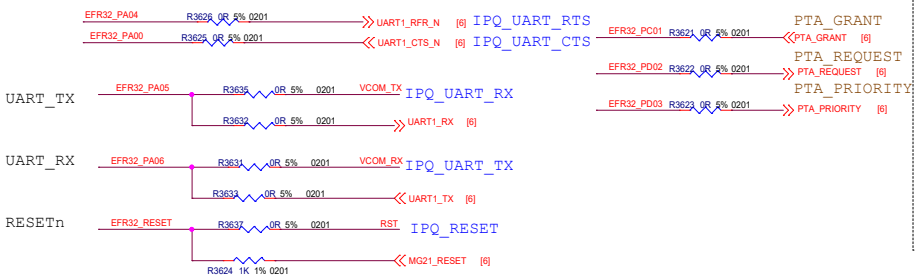
RF Shielding

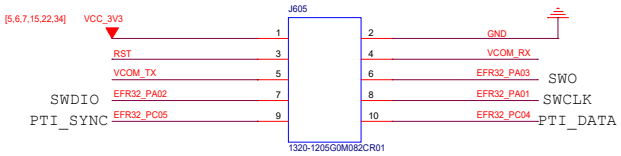
Power & Decoupling

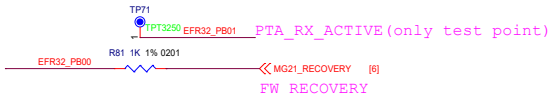


I/O Port Pins









Inventec Appliances Corporation

Approval:	Title: 34_Silicon lab EFR32MG21A020F10		
Check:	Size: C	Document Number: LUCKY 7	Rev: PT1
Design:	Date: Thursday, July 18, 2024	Sheet 34 of 35	

DATE	REV.	Revision History:
11/25	EVT1	1. R118 change to place component. 2. R143 change to place component and R155 change to 4.7K ohm. 3. R75 change to no stuff and R74 change to place component. 4. Move D3522 to the power_54V_PD1_OUT (page.20) and move D3523 to the power_54V_PD2_OUT (page.20) 5. R387 change to 49.9K ohm and R397 change to 30K ohm. 6. Change R3786 size to 0805. Change R3683 & R3703 size to 1210.

Inventec Appliances Corporation

Approval:	Title: 35_Change_List		
Check:	Size: B	Document Number: LUCKY 7	Rev: PT1
Design:	Date: Monday, November 25, 2024	Sheet 35 of 35	