Comparison of Level 1, 2 and 3 MOSFET's

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Comparison of Level 1, 2 and 3 MOSFET's

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Abstract- **The scaling of MOS technology to nanometer sizes leads to the development of physical and predictive models for circuit simulation that cover AC, RF, DC, temperature, geometry, bias and noise characteristics (1). This paper addresses the comparison between level 1,2 and 3 MOSFETs. The results are examined using SPICE (*Simulation Program with Integrated Circuit Emphasis*). Drain current versus drain-source voltage characteristics are plotted to display the differences between them.**

I. INTRODUCTION

The downscaling of transistor dimensions over the past years is an evolutionary process to provide superior performance, reduced size and cost. To assist this miniaturization of devices, new simulators and device models have been invented.

Everywhere from designing of an IC, manufacturing to fabrication technology development, modeling of device plays a major role in the advancement of Metal oxide semiconductor technology. Considering the real time effects is essential while simulating these device models. The SPICE model uses variety of parasitic circuit elements and some process related parameters. The circuit designer can control these parameters and syntax for MOSFET is given by

. MODEL <model name> NMOS [model parameters]
. MODEL <model name> PMOS [model parameters]

II. DEVICE MODELLING

To describe the performance of a device in mathematical terms, device modeling can be used. Theoretical or empirical considerations, or both can be used to derive a model. A few parameters along with the characterization can be used to build a desired model.

Quality of approximation and its complexity are often traded while establishing a model making procedure. When making these tradeoffs, an engineer considers factors such as intended use of the model and the required accuracy.

To create an understanding of the behavior of FET, rather than elemental models for a circuit simulation analytical models were built. With the new innovations and development of SPICE, these models were used as elemental models of the FETs.

III. SPICE MODELS

SPICE is a program used for simulation of electrical circuits. PSPICE (Orcad, Cadence Design Systems), HSPICE (Synopsis), SPECTRE (Cadence Design Systems), Eldo are some of the major commercial circuit simulators available in the market.

SmartSPICE (SiIvaco), Smash (Dolphin Integration), Saber (Analogy), APLAC (APLAC Solutions), TSPICE (Tanner Research) etc. are few more softwares available for simulation of complex circuits.

SPICE simulator and SPICE device models are the two distinct parts of SPICE. The simulator uses mathematical models to replicate the behavior of an actual electronic device or circuit. Simulation software allows for modeling of circuit operation and is an invaluable analysis tool.

Device models used by SPICE (Simulation Program for Integrated Circuit Engineering) simulators can be divided into three classes:

1. First Generation Models (Level 1, Level 2, Level 3 models)

2. Second Generation Models (BISM, BSIM2, HSPICE Level 28)

3. Third Generation Models (Level 7, Level 48, BSIM3, etc.)

Local stress, transistors operating in the sub-threshold region, short channel effects, noise calculations, gate leakage (tunneling), temperature variations and the equations used are better for circuit simulation in the newer generation models.

A. First Generation

Rather than focusing on the mathematical representation, these models express the original purpose of a physically based analytical MOSFET model, with all geometry dependent included in the model equations.

The First model generation is comprised of

1. LEVEL 1 model- When detailed analog models are not needed, these are often used to simulate large digital circuits. They provide a high level of accuracy for timing calculations and low simulation time. For more precision LEVEL 6 IDS model or one of the BSIM models (LEVEL 13, 28, 39, 47, 49, 53, 54, 57, 59, and 60) can be used for a

detailed description.

2. LEVEL 2 model-The bulk charge effects on current are considered in this model.

3. LEVEL 3 model-The accuracy of this model is similar to that of LEVEL 2 but it offers lesser simulation time and has a greater tendency to converge.

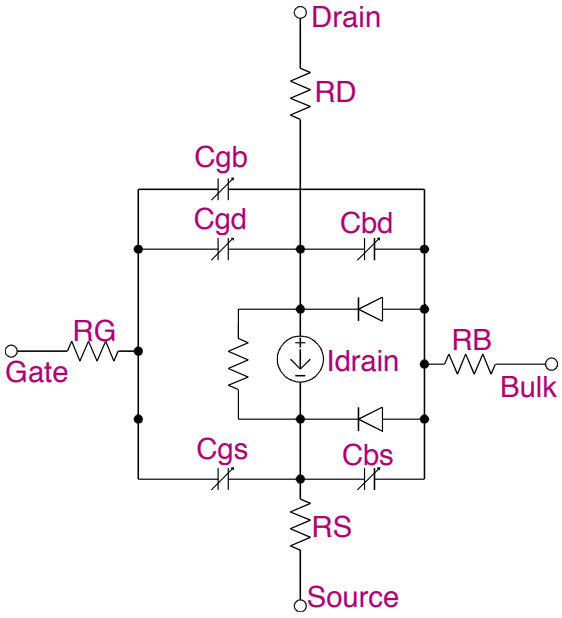

Fig. 1. Schematic of Level 1,2 and 3 MOSFET's (4)

1. LEVEL 1 (Schichman-Hodges Model)

The model is applicable to devices with gate length greater than $10\mu m$. This model is a first order approximation of practical output of long channel MOS device. This model takes into consideration channel length modulation by using a parameter L and body bias effect is taken care by the transconductance. Whenever the channel length reduces below 4 mm, these parameters become dependent on externally applied voltages and other parameters. The drain current (Ids) values will be lesser than the practically obtained values if the channel length falls below this value and the model fails to include the parameters related to short and narrow channel effects (3).

Gradual channel approximation and the square law for the saturated drain current are the simplifications employed in this model (1).

MODEL EQUATIONS:

(a.) Drain current, Ids Equations:

The LEVEL 1 model does not include the carrier saturation effect, carrier mobility degradation or the weak inversion model. The drain current equations for different regions of operation are given below:

Cutoff Region ($V_{gs} \leq V_{th}$)

$I_{ds} = 0.0$

Linear Region $(V_{ds} > V_{gs} - V_{th})$

$$I_{ds} = \text{KP}.\frac{Weff}{Leff}.(1 + \lambda.V_{ds}).\left(V_{gs} - V_{th} - \frac{Vds}{2}\right).V_{ds} \quad (1)$$

Saturation Region $(V_{ds} \geq V_{gs} - V_{th})$

$$I_{ds} = \frac{KP}{2}.\frac{W_{eff}}{L_{eff}}.(1 + \lambda.V_{ds}).(V_{gs} - V_{th})^2 \quad (2)$$

(b.) Effective Channel Length and Width:

The Level 1 model calculates the effective channel length and width from the drawn length and width:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2\ .\ (LD_{scaled} + DEL_{scaled}) \quad (3)$$

$$W_{eff} = M \cdot (W_{scaled}\, WMLT + XW_{scaled} - 2\ .\ WD_{scaled}) \quad (4)$$

(LMLT-Length shrink factor

WMLT-Diffusion layer and width shrink factor

LD_{scaled}- Lateral diffusion into channel from source and drain diffusion

WD_{scaled} − Lateral diffusion into channel from bulk along width

XL, XW- Accounts for masking and etching effects

DEL- Channel length reduction factor.)

(c.) Saturation Voltage, V_{sat}*:*

The channel pinch-off at the drain side develops the saturation voltage for LEVEL 1 MOSFET model which is given by:

$$V_{sat} = V_{gs} - V_{th}$$

The carrier velocity saturation effects are not included in the LEVEL 1 model.

(d.) Threshold Voltage, V_{th} :

$$V_{sb} < 0 \qquad V_{th} = V_{bi} + \Upsilon \cdot \left(\sqrt{\phi} + \frac{1}{2}\frac{V_{sb}}{\sqrt{\phi}}\right) \tag{5}$$

$$V_{sb} \geq 0 \qquad V_{th} = V_{bi} + \Upsilon \cdot (\phi + V_{sb})^{1/2} \tag{6}$$

The built-in voltage (V_{bi}) in the preceding equations are given by:

$$V_{bi} = V_{fb} + \phi \tag{7}$$

$$V_{bi} = VTO - \Upsilon.\sqrt{\phi}$$

(VTO- Zero bias threshold voltage for a large device)

TABLE I

BASIC MODEL PARAMETERS (1)

Name	Units	Default	Description
LEVEL		1.0	LEVEL 1 is the Schichman-Hodges model.
COX	F/m^2	3.453e-4	Oxide capacitance per unit gate area.
LAMBDA, λ	V^{-1}	0.0	Channel-length modulation.

KP (BETA-β)	A/V^2		Intrinsic transconductance parameter.

TABLE II
THRESHOLD VOLTAGE PARAMETERS (1)

GAMMA, γ	$\sqrt{V}$	0.5276	Body effect factor.
NSUB	cm^{-3}	1e15	Bulk surface doping.
PHI, ϕ	V	0.576	Surface inversion potential.
VTO, Vt	V		Zero-bias threshold voltage.

TABLE III
EFFECTIVE WIDTH AND LENGTH PARAMETERS (1)

DEL	m	0.0	Channel length reduction on each side.
LD	m	Default-0.0	Lateral diffusion into channel from source and drain diffusion.
LMLT		1.0	Length shrink factor.
WD	M	0.0	Lateral diffusion into channel from bulk along width.
WMLT		1.0	Diffusion layer and width shrink factor.
XL	m	0.0	Accounts for masking and etching effect.

XW	m	0.0	Accounts for masking and etching effect.

2. LEVEL 2 (Grove-Frohman Model)

LEVEL 2 is an advanced version of LEVEL 1 and implements Meyer's model. LEVEL 1 doesn't account for the short channel effects and is based on the assumption that threshold voltage is constant and varies only with the substrate voltage.

This simplified semi-empirical model gives a detailed description of the mobility degradation by the vertical field, the threshold region and the depletion region. It is used for very long- channel devices with gate length of approximately $10\mu m$. (1)

MODEL EQUATIONS:

(a.) Drain current, Ids Equations:

Drain current for LEVEL 2 models is lower than that of LEVEL 1 models and is given by:

Cutoff Region ($V_{gs} \leq V_{th}$)

I_{ds}=0.0

On Region ($V_{gs} > V_{th}$)

$$I_{ds} = \beta.\left\{\left(V_{gs} - V_{bi} - \frac{\eta.V_{ds}}{2}\right).V_{ds} - \frac{2}{3}.\gamma.[(\phi + V_{ds} + V_{sb})^{1.5} - (\phi + V_{sb})^{1.5}]\right\} \quad (8)$$

$$\eta = 1 + DELTA.\frac{\pi.\varepsilon_{si}}{4.COX.W_{eff}}; \quad (9)$$

DELTA- Controls the curvature of piecewise linear corners.

$$\beta = KP.\frac{W_{eff}}{L_{eff}} \quad (10)$$

(b.) Effective Channel Length and Width:

The drawn length and width are used to calculate the effective channel length and width for LEVEL 2 and can be written as:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2.\,(LD_{scaled} + DEL_{scaled}) \quad (11)$$

$$W_{eff} = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled} - 2\ .\ WD_{scaled}) \quad (12)$$

$$LREF_{eff} = LREF_{scaled} \cdot LMLT + XL_{scaled} - 2.\,(LD_{scaled} + DEL_{scaled}) \quad (13)$$

$$WREF_{eff} = M \cdot (WREF_{scaled} \cdot WMLT + XW_{scaled} - 2.\,WD_{scaled}) \quad (14)$$

(LREF, WREF- Channel length and width reference respectively)U

(c.) Saturation Voltage, V_{dsat}:

Due to channel pinch off at the drain side, the program calculates the saturation voltage. If the corrections for small-size effects are included, then:

$$V_{sat} = \frac{V_{gs}-V_{bi}}{\eta} + 0.5.\frac{\eta^2}{\gamma^2}.\left\{1 - \left[1 + 4.\frac{\gamma^2}{\eta^2}.\left(\frac{V_{gs}-V_{bi}}{\eta} + \phi + V_{sb}\right)\right]^{1/2}\right\} \quad (15)$$

$$V_{dsat} = V_{sat}$$

Considering the velocity saturation effect,

$$V_{dsat} = V_{sat} + V_c - (V_{sat} - V_c)^{1/2} \quad (16)$$

The following equation calculates the V_c value used in the preceding equation:

$$V_c = E_{crit} \cdot L_{eff}$$

E_{crit} = Drain-source critical field.

(d.) Threshold Voltage, V_{th}:

The effective threshold voltage including the device size effects and the terminal voltages is given by:

$$V_{th} = V_{bi} + \gamma.(\phi + V_{sb})^{1/2} \quad (17)$$

The following equation calculates the V_{bi} value used in the preceding equation:

$$V_{bi} = VTO - \gamma\sqrt{\phi} + (\eta - 1)(\phi + V_{sb})^{1/2} \quad (18)$$

LEVEL 2 uses VTO, γ and ϕ to calculate the threshold voltage.

(e.) Channel Length Modulation:

The LEVEL 2 MOS model modifies the I_{ds} current to include the channel length modulation effect:

$$I_{ds} = \frac{I_{ds}}{1 - \lambda V_{ds}} \quad (19)$$

For λ=LAMBDA<0; VMAX >0

$$\lambda = \frac{X_d}{\sqrt{NEFF}.L_{eff}.V_{ds}}.\left\{\sqrt{\left(\frac{VMAX.X_d}{2.\sqrt{NEFF}.u_{eff}}\right)^2 + V_{ds} - V_{dsat}} - \frac{VMAX.X_d}{2.\sqrt{NEFF}.u_{eff}}\right\} \quad (20)$$

NEFF-Total channel charge (fixed and mobile) coefficient

VMAX-Maximum drift velocity of carriers

For λ=LAMBDA<0; VMAX =0

$$\lambda = \frac{X_d}{L_{eff}.V_{ds}}.\sqrt{\frac{V_{ds}-V_{dsat}}{4}+\sqrt{1+\left(\frac{V_{ds}-V_{dsat}}{4}\right)^2}} \quad (21)$$

$$X_d = \sqrt{\frac{2.E_{si}}{q.NSUB}}$$

NSUB-Bulk surface doping

(f.) Mobility Reduction, μ_{eff}:

The mobility of carriers in the channel decreases as the carriers' speeds approach their scattering limited velocity.

If MOB=0, $\mu_{eff} < U0$ (default):

$$\mu_{eff} = U0.\left[\frac{UCRIT.E_{si}}{COX.(V_{gs}-V_{th}-UTRA.V_{ds})}\right]^{UEXP} \quad (22)$$

$V_{gs} < V_{th}$, $\mu_{eff} = U0$:

$$\mu_{eff} = U0.\left[\frac{UCRIT.E_{si}}{COX.(V_{gs}-V_{th})}\right]^{UEXP} \quad (23)$$

TABLE IV
BASIC MODEL PARAMETERS (1)

Name	Units	Default	Description
LEVEL		2.0	LEVEL 2 is the Grove-Frohman model.
COX	F/m^2	3.453e-4	Oxide capacitance per unit gate area.

ECRIT	V/cm	0.0	Critical electric field for carrier velocity saturation.
LAMDA, λ	V^{-1}	0.0	Channel length modulation.
NEFF		1.0	Total channel charge (fixed and mobile) coefficient.
VMAX	m/s	0.0	Maximum drift velocity of carriers
KP (BETA-β)	A/V^2	2.0e-5	Intrinsic transconductance parameter.

TABLE V
THRESHOLD VOLTAGE PARAMETERS (1)

GAMMA, γ	$\sqrt{V}$	0.5276	Body effect factor.
NSUB	cm^{-3}	1e15	Bulk surface doping.
PHI, ϕ	V	0.576	Surface inversion potential.
VTO, Vt	V		Zero-bias threshold voltage.
DELTA		0.0	Narrow width factor for adjusting threshold

TABLE VI
EFFECTIVE WIDTH AND LENGTH PARAMETERS (1)

DEL	m	0.0	Channel length reduction on each side.
LD	m	Default-0.0	Lateral diffusion into channel from source and drain diffusion.

LMLT		1.0	Length shrink factor.
LREF	m	0.0	Channel length reference.
WD	m	0.0	Lateral diffusion into channel from bulk along width.
WMLT		1.0	Diffusion layer and width shrink factor.
WREF	m	0.0	Channel width reference
XL, XW	m	0.0	Accounts for masking and etching effect.

TABLE VII
MOBILITY PARAMETERS (1)

MOB		0.0	MOB=0 or MOB=7. **NOTE:** MOB=7 invokes the channel length modulation and mobility equations of MOSFET LEVEL 3.
THETA	V^{-1}	0.0	Mobility modulation when MOB=7
UCRIT	V/cm	1.0e4	Critical field for mobility degradation
UEXP		0.0	Critical field exponent which characterizes surface mobility degradation

UO	cm^2 /V-s	600 (N) 250 (P)	Low-field bulk mobility.

3. LEVEL 3 (Empirical Model)

LEVEL 3 is developed to overcome the observed shortcomings of Level 2. It is more efficient mathematically and more accurate as compared to LEVEL 2. LEVEL 3 model is an improvement over LEVEL 2 model with simple equations and many empirical constants. As the name suggests this model is derived from empirical relations between practical data obtained from experiments and the theoretical models already existent.

With a structure similar to LEVEL 2, this is a semi-empirical model that places more emphasis on parameter extraction. Drain-induced barrier lowering (DIBL) and mobility degradation by the lateral field like physical effects are also included. These models are applicable to long-channel devices with gate length of approximately 2 μm (1).

MODEL EQUATIONS:

(a.) Drain current, I_{ds} Equations:

Drain current equations for LEVEL 3 are given by:

Cutoff Region ($V_{gs} < V_{th}$)

$I_{ds} = 0$

On Region ($V_{gs} > V_{th}$)

$$I_{ds} = \beta . \left(V_{gs} - V_{th} - \frac{1+fb}{2} . V_{ds} \right) . V_{ds} \quad (24)$$

$$\beta = KP . \frac{W_{eff}}{L_{eff}}; K.P = u_{eff} . COX \quad (25)$$

$$fb = f_n + \frac{\Upsilon . f_s}{4 . \sqrt{\phi + V_{sb}}} \quad (26)$$

f_n specifies the narrow width effect and is given by:

$$f_n = \frac{DELTA}{W_{eff}} . 0.25 . \frac{2\pi . E_{si}}{COX} \quad (27)$$

f_s specifies the short channel effects and is given by:

$$f_s = 1 - \frac{XJ_{scaled}}{L_{eff}} \Rightarrow \left\{ \frac{LD_{scaled}+W_c}{XJ_{scaled}} . \sqrt{1 - \left(\frac{W_p}{XJ_{scaled}+W_p} \right)^2 - \frac{LD_{scaled}}{XJ_{scaled}}} \right\} \quad (28)$$

$$W_p = X_d . \sqrt{\phi + V_{sb}}$$

(b.) Saturation Voltage, V_{dsat}:

Due to the channel pinch-off at the drain side, LEVEL 3 calculates the saturation voltage considering the VMAX parameter which specifies the reduction of the saturation voltage due to the carrier velocity saturation effect.

$$V_{sat} = \frac{V_{gs}-V_{th}}{1+fb} \quad (29)$$

$$V_{dsat} = V_{sat} + V_c - \left({V_{sat}}^2 + {V_c}^2 \right)^{0.5} \quad (30)$$

(c.) Threshold Voltage, V_{th}:

The following equation calculates the effective threshold voltage, including the device size and terminal voltage effects:

$$V_{th} = V_{bi} - \frac{8.14e-22}{COX.Leff^3} \Rightarrow ETA \Rightarrow V_{ds} + \Upsilon . \sqrt{\phi + V_{sb}} \, . f_s . + f_n . (\phi + V_{sb}) \quad (31)$$

The following equation calculates the v_{bi} value used in the preceding equation:

$$V_{bi} = V_{fb} + \phi = VTO - GAMMA . \sqrt{\phi} \quad (32)$$

(e.) Effective Channel Length and Width:

The following equations are used to determine the effective channel length and width for the LEVEL 3 model:

$$L_{eff} = L_{scaled} \cdot LMLT + XL_{scaled} - 2.\,(LD_{scaled} + DEL_{scaled}) \quad (34)$$

$$W_{eff} = M \cdot (W_{scaled} \cdot WMLT + XW_{scaled} - 2\,.WD_{scaled}) \quad (35)$$

$$LREFF = LREF_{scaled} \cdot LMLT + XL_{scaled} - 2.(LD_{scaled} + DEL_{scaled}) \quad (36)$$

$$WREF_{eff} = M \cdot (WREF_{scaled} \cdot WMLT + XW_{scaled} - 2\,.\,WD_{scaled}) \quad (37)$$

(f.)Effective Mobility, μ_{eff}:

The model defines the carrier mobility reduction due to the normal field as the effective surface mobility (μ_s).

For $V_{gs} > V_{th}$,

$$\mu_s = \frac{U0}{1+THETA(Vgs-Vth)} \quad (38)$$

VMAX>0

$$\mu_{eff} = \frac{\mu_s}{1+\frac{V_{ds}}{V_c}} \quad (39)$$

else ,

$$\mu_{eff} = \mu_s$$

(g.) Channel Length Modulation:

For $V_{ds} > V_{dsat}$

VMAX=0

$$\Delta L = X_d\sqrt{KAPPA(V_{ds} - V_{dsat})} \quad (40)$$

VMAX>0

$$\Delta L = -\frac{E_p.{X_d}^2}{2} + \sqrt{\left(\frac{E_p.{X_d}^2}{2}\right)^2 + KAPPA.{X_d}^2(V_{ds} - V_{dsat})} \quad (41)$$

$E_p = \frac{V_c(V_c+V_{dsat})}{L_{eff}.V_{dsat}}$ = Lateral electric field at the pinch off point

TABLE VIII
BASIC MODEL PARAMETERS (1)

Name	Units	Default	Description
LEVEL		3	LEVEL 3 is the empirical model.
COX	F/m^2	3.453e-4	Oxide capacitance per unit gate area.
ECRIT	V/cm	0.0	Critical electric field for carrier velocity saturation.
LAMDA, λ	V^{-1}	0.0	Channel length modulation.
NEFF		1.0	Total channel charge (fixed and mobile) coefficient.
VMAX	m/s	0.0	Maximum drift velocity of carriers
KP (BETA-β)	A/V^2	2.0e-5	Intrinsic transconductance parameter.

TABLE IX
THRESHOLD VOLTAGE PARAMETERS (1)

GAMMA, γ	$\sqrt{V}$	0.5276	Body effect factor.

NSUB	cm^{-3}	1e15	Bulk surface doping.
PHI, ϕ	V	0.576	Surface inversion potential.
VTO, Vt	V		Zero-bias threshold voltage.
DELTA		0.0	Narrow width factor for adjusting threshold.
ETA		0.0	Static feedback factor for adjusting threshold

TABLE X
EFFECTIVE WIDTH AND LENGTH PARAMETERS (1)

DEL	m	0.0	Channel length reduction on each side.
LD	m	Default-0.0	Lateral diffusion into channel from source and drain diffusion.
LMLT		1.0	Length shrink factor.
LREF	m	0.0	Channel length reference.
WD	m	0.0	Lateral diffusion into channel from bulk along width.
WMLT		1.0	Diffusion layer and width shrink factor.
WREF	m	0.0	Channel width reference
XL, XW	m	0.0	Accounts for masking and etching effect.

TABLE XI
MOBILITY PARAMETERS (1)

THETA	V^{-1}	0.0	Mobility degradation factor
UO	cm^2 /V-s	600 (N) 250 (P)	Low-field bulk mobility.

V. PSPICE NETLIST AND OUTPUT WAVEFORMS

A. LEVEL 1

```
Vgs 1 0 2V
Vds 2 0 2V
Vbs 3 0 0V
*NFET
M1 2 1 0 3 L1 L=3u W=3u
*NFET Model
.MODEL L1 NMOS LEVEL=1 RSH=0 TOX=300E-10 LD=0.21E-6
+ XJ=0.3E-6 VMAX=15E4 ETA=0.18 GAMMA=0.4 KAPPA=0.5
+ NSUB=35E14 UO=700 THETA=0.095 VTO=0.781 CGSO=2.8E-10
+ CGDO=2.8E-10 CJ=5.75E-5 CJSW=2.48E-10 PB=0.7 MJ=0.5
+ MJSW=0.3 NFS=1E10
.options post probe
*For I-V Curve Id vs Vgs
.dc Vgs 0 5 0.1
.probe I1(M1)
*For I-V Curve Id vs Vds with Vgs = 2V
.dc vds 0 5 0.1
.probe I1(M1)
*For family of I-V Curves
.dc Vds 0 5 0.1 Vgs 0 5 1
.probe I1(M1)
.end
```

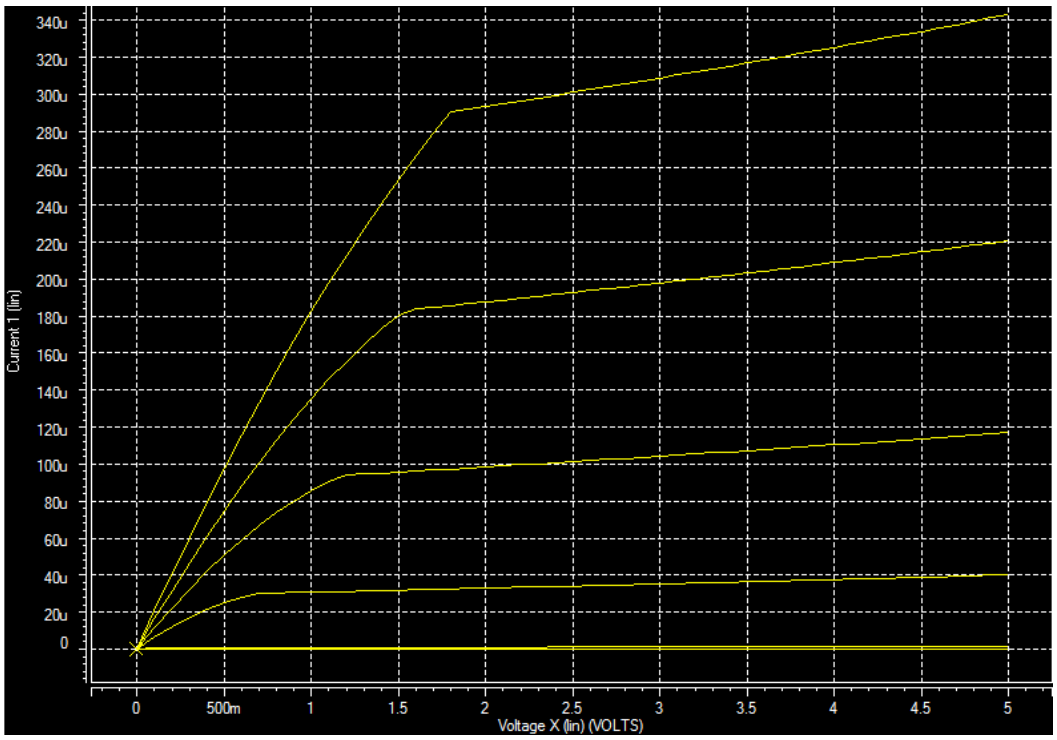

Fig. 2. Variation of Id as a function of gate voltage in LEVEL 1 model

B. LEVEL 2

```
Vgs 1 0 2V
Vds 2 0 2V
Vbs 3 0 0V
*NFET
M1 2 1 0 3 L2 L=3u W=3u
*NFET Model
.MODEL L2 NMOS LEVEL=2 PHI=0.7 TOX=4.08E-8 XJ=0.2 TPG=1
+VTO=0.8096 DELTA=4.586 LD=2.972E-7 KP=5.3532E-5
+UO=632.5 UEXP=0.1328 UCRIT=3.897E4 RSH=6.202
+GAMMA=0.5263 NSUB=5.977E15 NFS=5.925e11 VMAX=5.83E4
+LAMBDA=3.903E-2 CGDO=3.7731E-10 CGSO=3.7731E-10
+CGBO=3.4581E-10 CJ=1.3679E-4 MJ=0.63238 CJSW=5.1553E-10
+MJSW=0.26805 PB=0.4
.options post probe
*For I-V Curve Id vs Vgs
.dc Vgs 0 5 0.1
.probe I1(M1)
*For I-V Curve Id vs Vds with Vgs = 2V
.dc vds 0 5 0.1
```

```
.probe I1(M1)
*For family of I-V Curves
.dc Vds 0 5 0.1 Vgs 0 5 1
.probe I1(M1)
.end
```

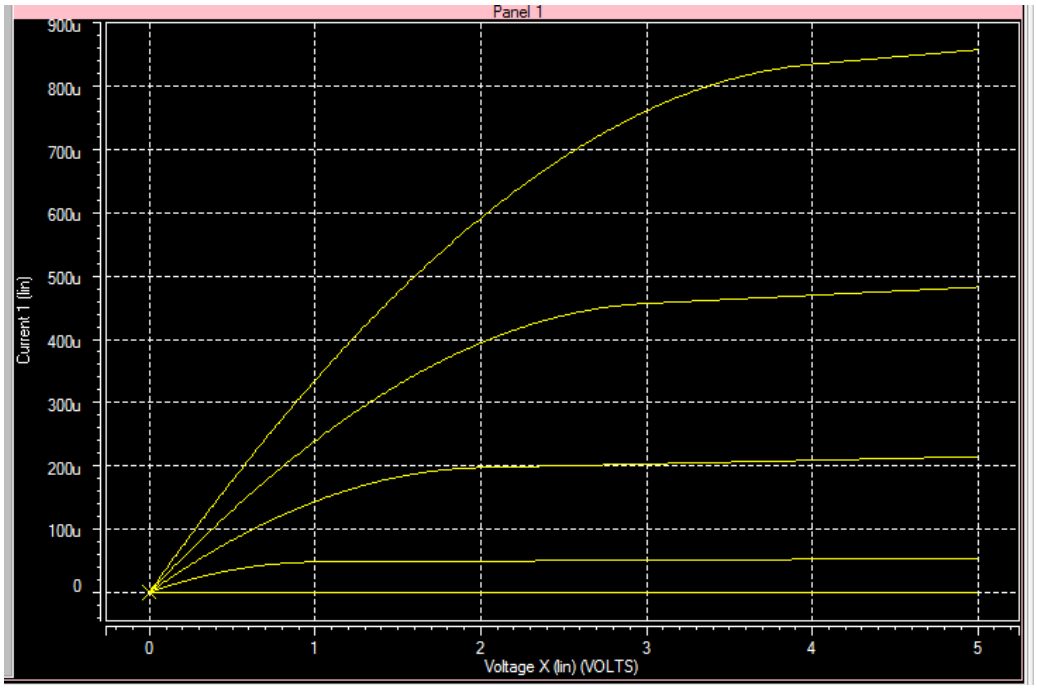

Fig. 3. Variation of Id as a function of gate voltage in LEVEL 2 model

C. LEVEL 3

```
Vgs 1 0 2V
Vds 2 0 2V
Vbs 3 0 0V
*NFET
M1 2 1 0 3 L3 L=3u W=3u
*NFET Model
.MODEL L3 NMOS LEVEL=3 TPG=1 TOX=1.5E-8 LD=2.95E-7 WD=3.00E-7
+UO= 263 VTO=0.5 THETA=0.046 RS=27 RD=27 DELTA=2.27 NSUB=1.45E17
+XJ=1.84E-7 VMAX=1.10E7 ETA=0.927 KAPPA=0.655 NFS=3E11
+CGSO=3.4E-10 CGDO=3.48E-10 CGBO=5.75E-10 XQC=0.4
.options post probe
*For I-V Curve Id vs Vgs
.dc Vgs 0 5 0.1
.probe I1(M1)
*For I-V Curve Id vs Vds with Vgs = 2V
.dc vds 0 5 0.1
```

```
.probe I1(M1)
*For family of I-V Curves
.dc Vds 0 5 0.1 Vgs 0 5 1
.probe I1(M1)
.end
```

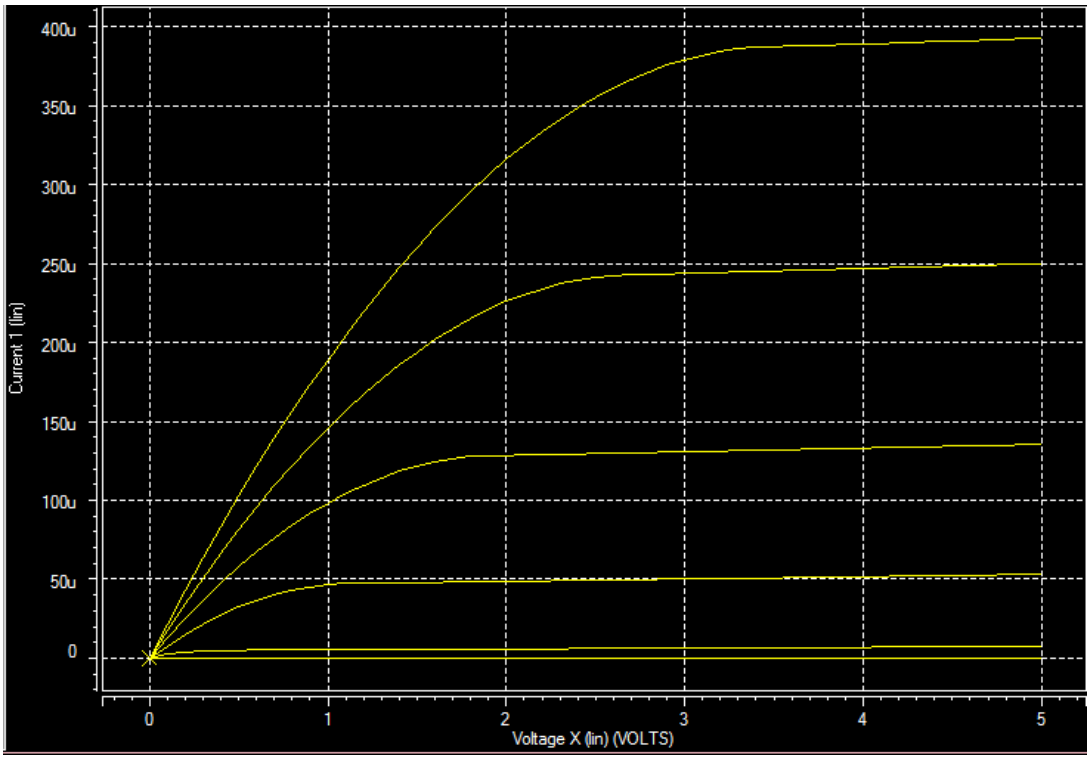

Fig. 4. Variation of Id as a function of gate voltage in LEVEL 3 model

D. TEMPERATURE COMPENSATION

```
vds 1 0 5
vgs 2 0 2
.option ingold=2 numdgt=6 post=2
.temp 25 100
m1 1 2 0 0 nch w=10u L=1u
.print id=lx4(m1) vdsat=lv10(m1)
.model M1 nmos LEVEL=3 tlev=1 tlevc=0 acm=3
+ uo=600 tox=172.6572
+ vto=0.8 gamma=0.8 phi=0.64
+ kappa=0 xj=0
+ nsub=1e16 rsh=0
+ tcv=1.5e-3 bex=-1.5
.op
```

.end

1. CALCULATIONS:

1. At T= 25

beta = 1.2e – 3

V_{tm}= 0.8

phi(t) = 0.64

$$I_{ds} = (1.2e-3).0.5.\frac{(2-0.8)^2}{1+\frac{0.2}{\sqrt{0.64}}} = 6.9123-4$$

2. At T= 100

beta = (1.2e - 3).$(1.251)^{-1.5}$ = 0.570545e-4

V_{tm}= 0.8- (1.5e - 3).75= 0.6875

phi(t) = 0.64. 1.251 – 0.323 = 0.4770

$$I_{ds} = (0.570545\text{e}-4).0.5.\frac{(2-0.6875)^2}{1+\frac{0.2}{\sqrt{0.4770}}} = 5.724e-4$$

2. SIMULATION RESULTS:

At T= 25, id=6.91200e - 04

At T= 100, id=5.72451e - 04

V. COMPARISON

A. LEVEL 1

NSUB (substrate impurity concentration); NSS (Surface state density used to define

surface component of V_{T0}*);* N_A (NMOS); N_D (PMOS); U0 (Surface mobility μ_0); RD (Drain resistance); TOX (Oxide thickness *tox);* RS (Source resistance); RSH (Drain and Source sheet resistance ($\Omega/\square$)) are the parameters used.

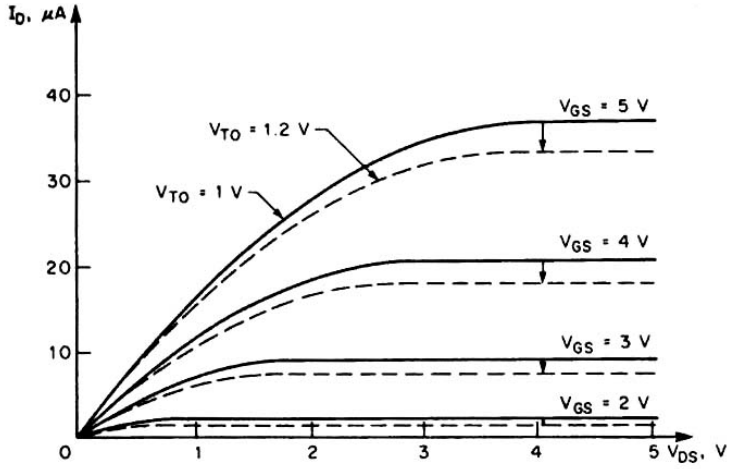

Fig. 5. Variation of Id with model parameter VTO for LEVEL 1 model (Copyright 1988 by McGraw- Hill, Inc).

B. LEVEL 2

Level 2 is an analytical model that takes into account small geometry effects. New parameters added are NFS (Fast surface state density which models sub threshold); NEFF (Total channel charge coefficient); VMAX (Maximum drift velocity for carriers used for modeling velocity saturation); DELTA (Channel width effect on V_T); XJ (Junction depth of source and drain). UCRIT (Critical electric field for mobility degradation), UTRA (Transverse field coefficient for mobility degradation) and UEXP (Exponent coefficient for mobility degradation) and produce a multiplicative surface mobility degradation factor to multiply times KP and appears in Level 2 only.

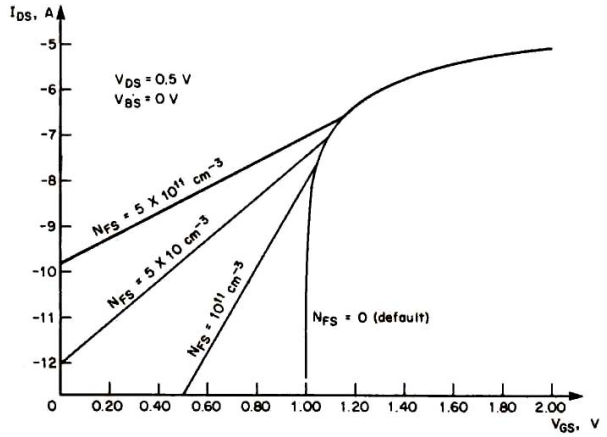

Fig. 6. Variation of Id with gate voltage in LEVEL 2 model (Copyright 1988 by McGraw- Hill, Inc).

C. LEVEL 3

Level 3 as the name describes is more empirical and less analytical than Level 2, which permits simpler computation and improved convergence while sacrificing little accuracy. Level 2 parameters such as NEFF, UTRA, UCRI and UEXP have been deleted. New parameters important to this model are KAPPA (Saturation field factor); ETA (static feedback on VT which models effect of VDS on VT); THETA (Mobility modulation which models the effect of VGS on surface mobility).

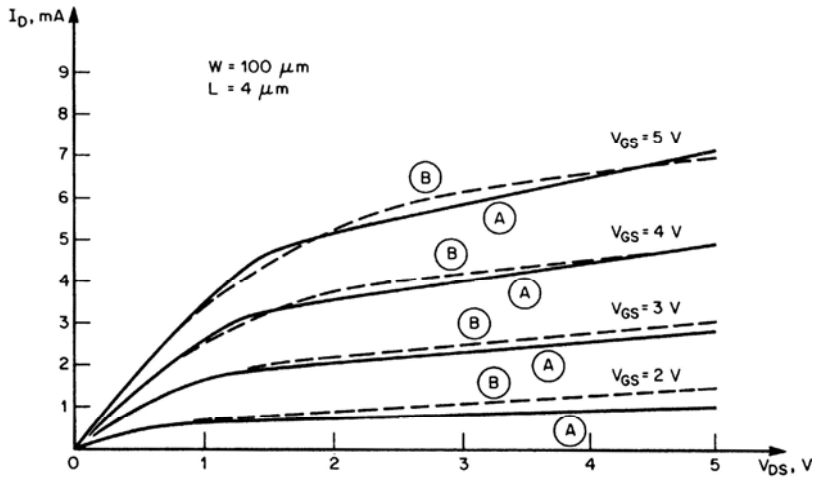

Fig. 7. Id-Vds characteristics of NMOS for LEVEL 2 (A) and LEVEL 3 (B) model.

VI. CONCLUSION

From the above results we can conclude that Level 1 model is too approximated with the number of fitting parameters too small. Also Level 1 can be used for preliminary circuit simulations and appropriate for long channel and uniform-doping devices. The benefit from Level 2 is small. Level 3 has higher accuracy and requires less time for calculations. Level 3 is good for MOSFET down to about 2 microns.

The most challenging task to device models is the high accuracy fitting of device data from different technologies. Along with quality, the ease of parameter extraction, number of parameters, redundancy of parameters, correlation of parameters, etc. should also be considered (2).

Device models are constantly developed, elaborated and refined to achieve best description and prediction of the downscaling devices and to met the new challenges of power dissipation, leakage management, short channel effects, etc. Deep understanding of the underlying physical phenomena is required as well as competent use of mathematical techniques to settle efficient and accurate modeling methodologies that

encompass constantly downscaling technologies. Now a huge emphasis is placed on obtaining physics-based, simple and highly accurate analytical device models.

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