



DV/Dt Circuit - Charges capacitor through diode on turn ON of the breaker s.t. gate voltage and hence output voltage is slewed at the rate of $Dv/Dt = I_{src}/C$, $C = 47$ nF, $I_{src} = 16$ uA typ, $Dv/Dt = 0.340$ V/mS. During turn off the base, of the transistor is pulled low, turning it on s.t. the capacitor is discharged immediately.

Please see Texas Instruments application note SLVA673A for the origin of this design intent.

large capacitance to handle current spikes potentially during events like sit-to-stand?

$I_{inrush} = CL * Dv / Dt$ Use $Dv / Dt = 0.5V / mS$
 $I_{inrush} = 1.2mF * 0.5V / mS = 0.6A$
 $t_{ON} = 54V / 0.5V / mS = 108$ mS
 Use factor of x 1.1, $T_{Fault} = 1.1 * 108$ mS = 126 mS
 $PLIM = \max(V_{smin} * VinMAX / R_{sns}, 2 * VinMAX * I_{inrushmax})$
 $Vinmax = 54V, I_{inrushmax} = 0.8A, V_{smin} = 55mV, R_{sns} = 2m\Omega$
 $PLIM = \max(210W, 75.6W) = 210W$

C_{fault} is purposely reduced to 2.2mS to avoid SOA when tripping the current limit.
 $I_{trip} = 52.5A, ILIM = 27.5A, PLIM = 210W, T_{on}$ for 1.2mF load = 108ms, $T_{fault} = 1.1 * T_{on} = 126ms$

$$R_{PWR} = 1.25 \times 10^5 \times R_s \times P_{FET(LIM)} \quad 1.25E5 * .002 * 210 = 26.7k$$

$$C_T = \frac{t_{FAULT} \times 85 \mu A}{4V} = t_{FAULT} \times 2.13 \times 10^{-5} \quad 126e-3 * 2.13e-5 = 2.7uF$$