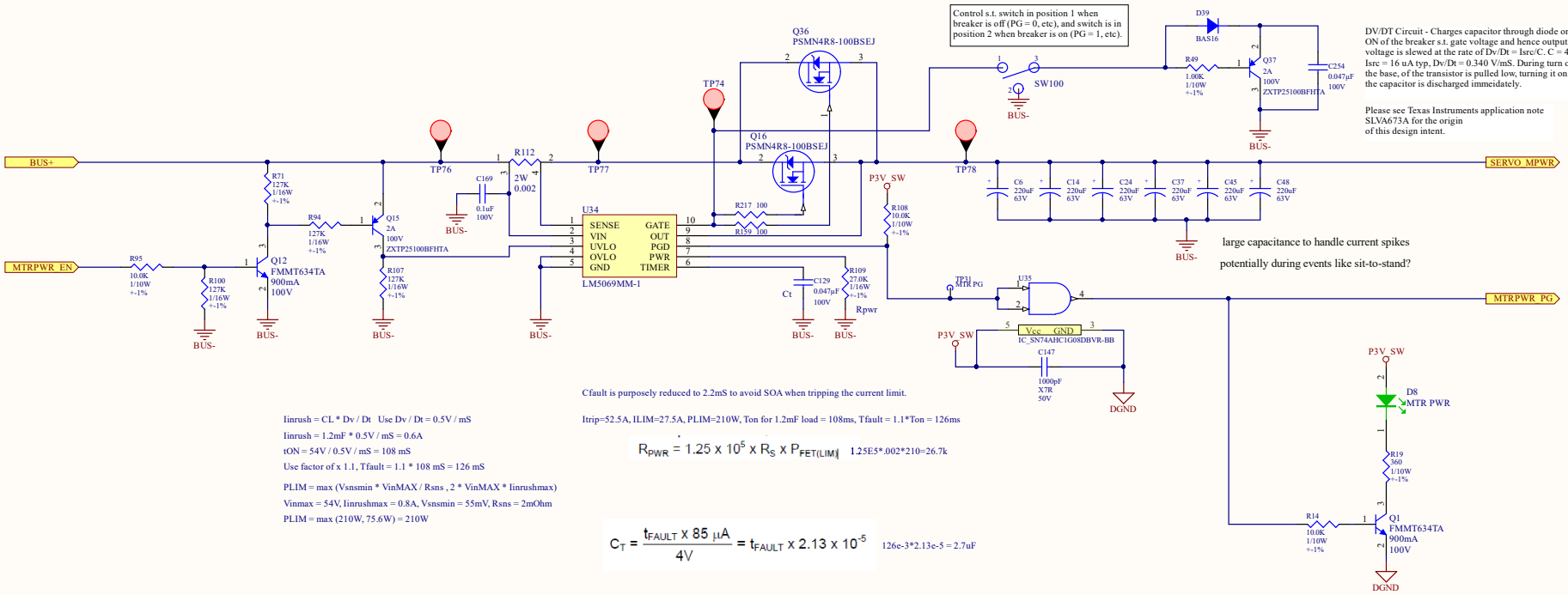

DV/DT Circuit - Charges capacitor through diode on turn ON of the breaker s.t. gate voltage and hence output voltage is slewed at the rate of Dv/Dt = Isrc/C. C = 47 nF, Isrc = 16 uA typ, Dv/Dt = 0.340 V/mS. During turn off the base, of the transistor is pulled low, turning it on s.t. the capacitor is discharged immediately.

Please see Texas Instruments application note SLVA673A for the origin of this design intent.

large capacitance to handle current spikes potentially during events like sit-to-stand?

Cfault is purposely reduced to 2.2mS to avoid SOA when tripping the current limit.

Itrip=52.5A, ILIM=27.5A, PLIM=210W, Ton for 1.2mF load = 108ms, Tfault = 1.1*Ton = 126ms

Iinrush = CL * Dv / Dt Use Dv / Dt = 0.5V / mS

Iinrush = 1.2mF * 0.5V / mS = 0.6A

tON = 54V / 0.5V / mS = 108 mS

Use factor of x 1.1, Tfault = 1.1 * 108 mS = 126 mS

PLIM = max (Vsnsmin * VinMAX / Rsns , 2 * VinMAX * Iinrushmax)

Vinmax = 54V, Iinrushmax = 0.8A, Vsnsmin = 55mV, Rsns = 2mOhm

PLIM = max (210W, 75.6W) = 210W

$$R_{PWR} = 1.25 \times 10^5 \times R_S \times P_{FET(LIM)}$$

1.25E5*.002*210=26.7k

$$C_T = \frac{t_{FAULT} \times 85\ \mu A}{4V} = t_{FAULT} \times 2.13 \times 10^{-5}$$

126e-3*2.13e-5 = 2.7uF

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Sheet Title: MOTOR POWER CIRCUIT BREAKER

Project Name: 104536-AMPLIFIER.PRJPCB

Size: TABLOID | Fab: 104536 | Rev: J

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