Application Report
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Minimizing Ringing at the Switch Node of a Boost Converter

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ABSTRACT

This application report explains how to use proper board layout and/or a snubber to reduce high-frequency ringing at the switch node of a boost converter.

1 Description of the Problem

The circuit in Figure 1 shows the boost converter's *critical loop* created by the parasitic inductances and capacitances, labeled as L_{PAR} and C_{PAR} reference designators. The node where the two switches and inductor of a switching converter meet is called the switch node. It is not uncommon for the parasitic inductances and capacitances to interact and cause voltage oscillations in the 200-MHz+ range at the switch node. If the amplitude of this *ringing* is above the absolute maximum rated voltage of the low-side switch, it can be destructive to the switch. In addition, the conducted emissions and/or electromagnetic interference (EMI) generated by the ringing can cause problems for any nearby ICs.

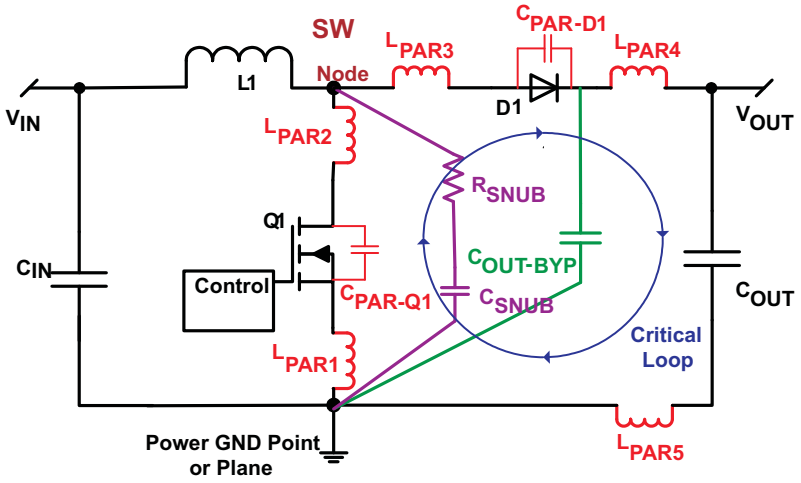

Figure 1. Boost Converter Schematic

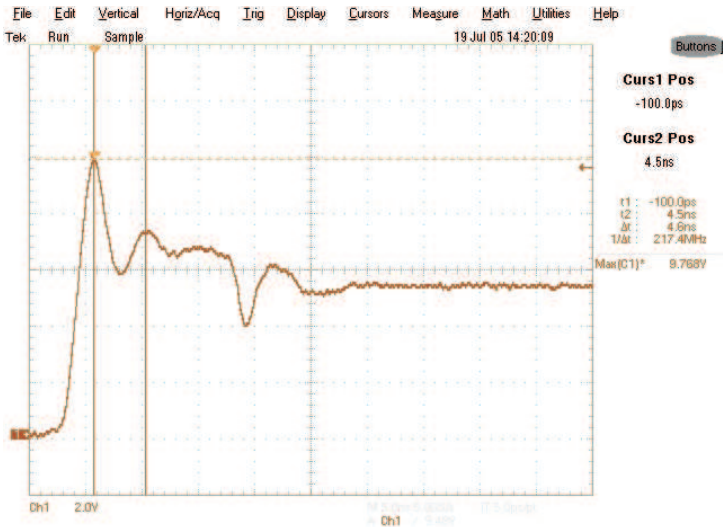

Figure 2. Ringing at Switch Node of Boost Converter

Figure 2 shows a scope plot of the switch node of a boost converter on a 5-ns/div time scale. A scope and scope probe with at least a 500-MHz bandwidth, approximately twice the expected 200-MHz ringing frequency, were used to take the plot. The scope probe's ground loop was minimized to prevent inductive pick-up from distorting the measurement. With V_{IN} = 3.3 V and V_{OUT} = 5 V, the peak voltage at the switch node should be no more than $V_{OUT} + V_{DIODE} \approx$ 5.7 V. However, the peak amplitude of the ringing at the switch node is 9.8 V, which could damage the low-side switch.

The power supply designer has several options during the design phase to minimize this ringing. If a controller is used, the designer should select FETs and diodes with minimal parasitic capacitances and then lay out the board to minimize the distance between both switches and the inductor, thereby minimizing L_{PAR2} and L_{PAR3}. In addition, the designer can minimize L_{PAR1} by reducing the distance between the source pin of the FET and the power ground point or plane. L_{PAR4} and L_{PAR5} can be minimized by placing the bulk output capacitor as close as possible to the diode's cathode and power ground. A high-frequency bypass capacitor [$C_{OUT-BYP}$] between the output (0.01 µF – 2.2 µF) and power ground is also recommended.

Improving board layout may not be possible due to board size restrictions or due to an integrated FET power IC with internal $C_{PAR\#}$, L_{PAR1}, L_{PAR2}, and L_{PAR3}. Therefore, a snubber circuit, consisting of R_{SNUB} and C_{SNUB} from the switch node to power ground may be required. A snubber is an energy-absorbing circuit used to eliminate voltage spikes caused by circuit parasitic inductance when a switch opens. By providing an alternate path to ground for the current flowing through the circuit's parasitic inductance, the snubber reduces the voltage transient and damps the subsequent ringing with the parasitic capacitance that occurs when the switch opens.

The rest of this application report provides steps on how to size the snubber components to damp the ringing without significantly slowing down the switch turnoff rise time or reducing overall efficiency.

After determining the frequency of the ringing, f_{INIT} = 217 MHz, caused by the parasitic inductance [$L_{\Sigma PAR\#}$] and parasitic capacitance [$C_{\Sigma PAR\#}$] from the scope plot in Figure 2, add enough capacitance [C_{ADD}] from the switch node to ground to reduce the ringing frequency by ½. Figure 3 shows the ringing at 113 MHz after 300 pF of capacitance has been added.

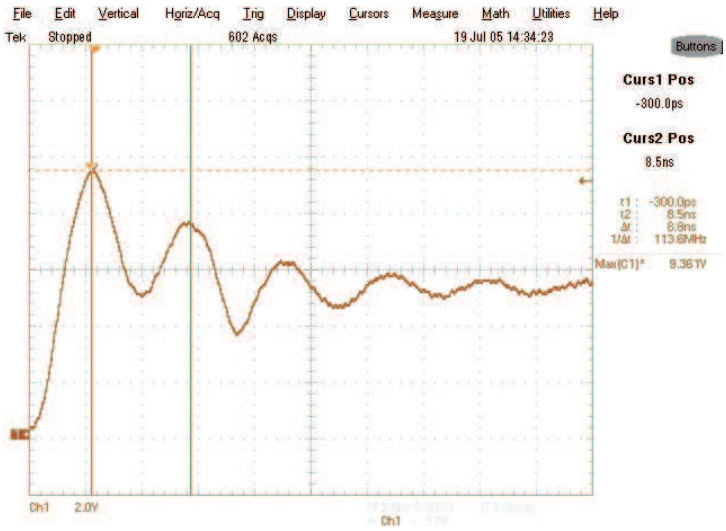

Figure 3. Ringing at the Switch Node of a Boost Converter With 300pF to Ground

Because the resonant frequency of an LC circuit is inversely proportional to the square root of the LC product, the total circuit capacitance [$C_{\Sigma PAR\#}$ + C_{ADD}] is now 4 times its original value [or $C_{\Sigma PAR\#} = C_{ADD}/3$]. This is the minimum value for the capacitance that should be used for C_{SNUB}. The amount of parasitic inductance causing the ringing can be computed from

$$f_{INIT} = \frac{1}{2\pi\sqrt{L_{\Sigma PAR\#}C_{\Sigma PAR\#}}} \quad (1)$$

Rearranging gives

$$L_{\Sigma PAR\#} = \frac{1}{\frac{C_{ADD}}{3} \times \left(2\pi f_{INIT}\right)^2} \quad (2)$$

In this example, $L_{\Sigma PAR\#}$ is 5.4 nH. Finally, the optimal size for the snubber resistor is the characteristic impedance of the original parasitic capacitance [$C_{\Sigma PAR\#} = C_{ADD}/3$ = 100 pF] and stray inductance [$L_{\Sigma PAR\#}$ = 5.4 nH]:

$$R_{SNUB} = \sqrt{\frac{L_{\Sigma PAR\#}}{\frac{C_{ADD}}{3}}} \quad (3)$$

From Equation 3, R_{SNUB} = 7.3 Ω which was rounded up to 10 Ω. After placing C_{SNUB} = 330 pF, the next standard value above the computed C_{ADD}, and R_{SNUB} = 10 Ω from the switch node to ground, a second scope plot of the switch node was taken as shown in Figure 4.

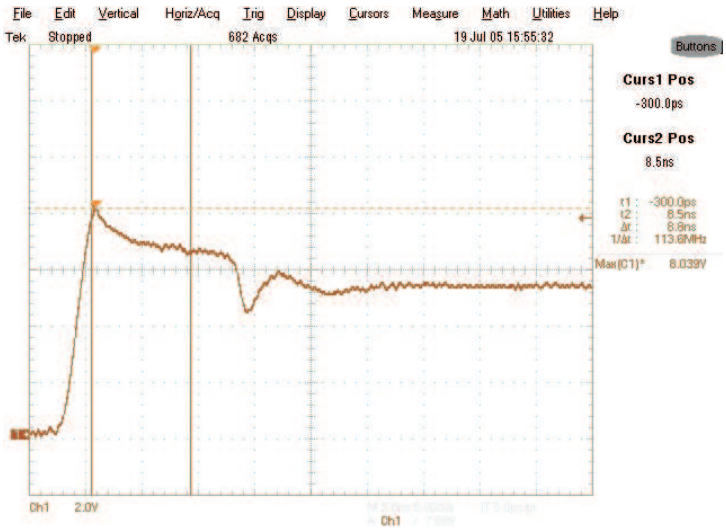

Figure 4. Boost Converter Switch Node After Snubber is Added

Note that the ringing now is gone, the peak amplitude of the ringing is reduced by 1.8 V to 8 V, a 20% reduction, and the switch turnoff time was decreased by only 2 ns. The designer could incrementally increase C_{SNUB} until the switch node corner begins to round (implying that the $L_{\Sigma PAR\#}$, C_{SNUB}, and R_{SNUB} circuit is critically damped with a Q = 1). However, as C_{SNUB} increases, the energy absorbed by the snubber increases, and therefore the power that R_{SNUB} must dissipate increases, while the boost converter efficiency decreases. The power that R_{SNUB} must dissipate is computed as $P_{SNUB} = ½ C_{SNUB} \times V_{PK}^2 \times f_{SW}$ where V_{PK} is the reduced peak amplitude and f_{SW} is the boost converter switching frequency. The designer must ensure that the R_{SNUB}'s package is large enough to dissipate this power. In general, choosing C_{SNUB} at the next standard value above the amount needed to reduce the oscillation frequency by ½ [C_{ADD}] results in approximately a 20% reduction in peak amplitude while only decreasing peak efficiency by a few percent.

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