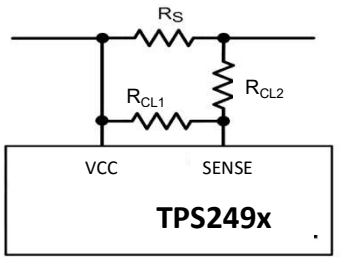
TPS2490/1/2/3 & TPS2480/1/2/3 Hot Swap Design Tool

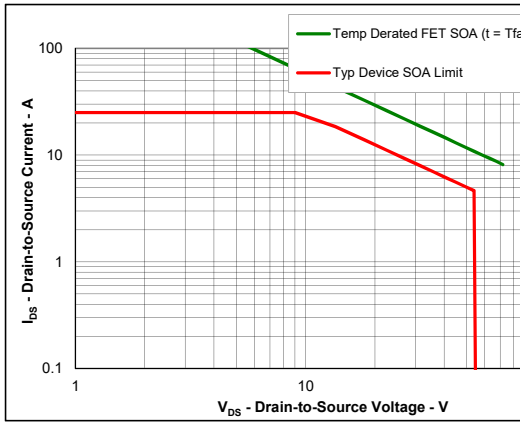
Note: The components calculated in this worksheet are reasonable starting values for a design using the TPS249x and TPS248x series of Hot-swap Controller. As such, they are not optimized for any particular performance attribute. Tolerances of the components are not included in the calculations. See the Instructions tab for additional information.
Consult the TPS249x datasheet for more detail.

	Enter Values in Green Shaded Cells
	Calculated Values are shown in White Cells
	Yellow and Red cells highlight pottential issues with the design. Red highlights items that are higher risk.

Step 1: Operating Conditions	Minimum Input Operating Voltage: $V_{IN(MIN)}$	9	V
	Nominal Input Operating Voltage: $V_{IN(NOM)}$	28	V
	Maximum Input Operating Voltage: $V_{IN(MAX)}$	54	V
	Maximum Load Current: $I_{OUT(MAX)}$	21	A
	Maximum Output Load Capacitance: C_{LOAD}	2000	µF
	Maximum Ambient Operating Temperature: T_{MAX}	71	°C
Step 2: Current Limit and Circuit Breaker	Maximum Recommended Value for Rs	2.12	mΩ
	Use External Resistor Divider to Reduce Effecitve R_S	No	
	Enter the Resistance for R_S	2	mΩ
	Resulting Minimum Current Limit	22.5	A
	Resulting Typical Current Limit	25.0	A
	Resulting Maximum Current Limit	27.5	A
	Maximum Power Dissipation in R_S	1.5	W
Step 3: MOSFET Selection	Q1 FET Name	FDB031N08	
	Estimated MOSFET $R\Theta_{JA}$	60	°C/W
	Number of MosFETs	2	#
	MOSFET On resistance @ $T_{J,DC}$	2.1	mΩ
	Maximum FET Junction Temperature	150	°C
	100µs SOA Current (re-use 1ms data if unavailable) @ $V_{IN(MAX)}$	100.0	A
	1ms SOA Current @ $V_{IN(MAX)}$	10.0	A
	10ms SOA Current @ $V_{IN(MAX)}$	2.0	A
	100ms Current at @ $V_{IN(MAX)}$ (use DC if 100ms not available)	0.9	A
	1s or DC SOA Current at @ $V_{IN(MAX)}$ (use DC if 1s not available)	0.8	A
	FET Power dissapation at full load (per FET)	0.2	W
	Maximum steady state FET Junction Temperature ($T_{J,DC}$)	84.9	°C
	Minimum Power Limit to Ensure Vsns > 5mV & Vprog > 0.4V ($P_{LIM,MIN}$)	135.0	W
	Target Power Limit	250.0	W
	Select R_3	30.0	kΩ
	Calculated R_4	10.00	kΩ
	Actual R_4 (Select next available std. value)	10	kΩ
	Actual PLIM	250.00	W
Step 4: Startup	Load Turn-On Threshold	12	V

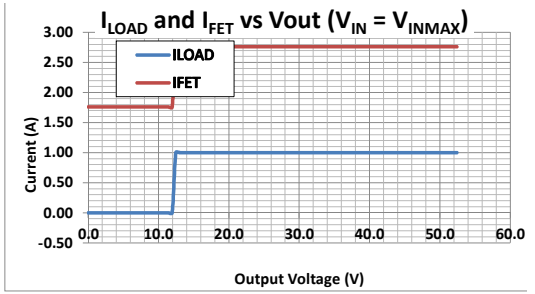
Note: TI recommends choosing a FET with SOA current specified for 100ms and/or 1s or DC. If choosing a FET without these parameters, this calculator will estimate the values via extrapolation, which leaves an inherent associated risk.

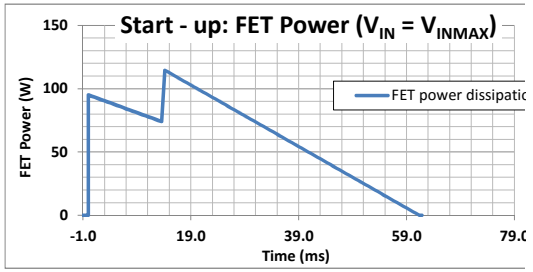




Startup Load Type	Constant Current	
Startup Load Value	1	A
Use External Soft-Start Control	Yes	
Can a "hot" board be hotplugged	No	
Recommended slew Rate (max)	NA	V/ms
Recommended slew Rate (min)	NA	V/ms
dv/dt rate on Vout	1	V/ms
calculated SS capacitance	22.00	nF
actual SS capacitance	25	nF
actual dv/dt rate on Vout	0.88	V/ms
SOA margin during start-up	0.39	
Target Fault Time	0.4	ms
Calculated Timer Capacitance	2.50	nF
Actual Timer Capacitance (pick one smaller than $C_{T,CALC}$)	3	nF
Actual Fault Time (Tfault)	0.48	ms
SOA margin during "hot-short" or "start-into short"	2.34	

Note: This is the typical dv/dt rate, but max value can be larger. This is because the gate source current can vary from 16uA to 28uA. Thus TI recommends keeping the overall SOA margin during start-up >1.5 in order to compensate for this.



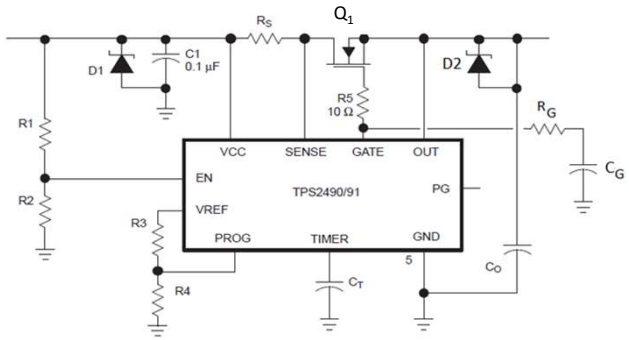


Step 5: UVLO, OVLO & PGD Thresholds

Target Under - Voltage	12	V
Recommended R2	10.00	kΩ
Actual R2	21.5	kΩ
Calculated R1	169.61	kΩ
Actual R1	122	kΩ

Resulting Thresholds:	Minimum	Typical	Maximum	
Resulting Upper UVLO Threshold =	8.81	9.01	9.21	V
Resulting Lower UVLO Threshold =	8.14	8.34	8.54	V

Design Summary



R_S =	2	mΩ
R_{CL1} =	DNP	Ω
R_{CL2} =	short	Ω
R1 =	122	kΩ
R2 =	21.5	kΩ
R3 =	30.0	kΩ
R4 =	10	kΩ
C_T =	3.00	nF
C_1 =	0.10	µF
Q1 =	FDB031N08	
R_G =	1	kΩ
C_G =	25	nF

	Typical	Units
Current limit	25.0	A
Power Limit	250	W
Fault Timeout	0.480	ms
Upper UVLO Threshold	9.0	V
Lower UVLO Threshold	8.3	V

Notes: 1. Although not mandatory, C_{IN} provides transient suppression at the VIN pin
2. A TVS clamp from VIN to GND is absolutely mandatory to clamp the voltage overshoot upon MOSFET turn-off, e.g. during circuit breaker
3. Componet tolerances not accounted for in Min/Max Calculations.