Schematic Review Form
Octasic/Chethan

Pin #	Name	Info	Violations	*Description*
1	CC2	`Routed to CC2 on Type-C connector`		Type-C Configuration channel signal 2
2	CC1	`Routed to CC1 on Type-C connector`		Type-C Configuration channel signal 1
3	CURRENT_MODE	`NC`		Tri-level input pin to indicate current advertisement in DFP (or DFP in DRP) mode while in GPIO mode. Don't care in UFP mode. Provides the flexibility to advertise higher current without I2C. The pin has 250 K internal pull-down. L – Low - Default – 900 mA M - Medium (Install 500 K to VDD5 on the PCB) – 1.5 A H - High (Install 10 K to VDD5 on the PCB) – 3 A
4	PORT	`4.75K Pulldown to GND`		Tri-level input pin to indicate port mode. The state of this pin is sampled when HD3SS3220's ENn_CC is asserted low, and VDD5 is active. This pin is also sampled following a I2C_SOFT_RESET. H - DFP (Pull-up to VDD5 if DFP mode is desired) NC - DRP (Leave unconnected if DRP mode is desired) L - UFP (Pull-down or tie to GND if UFP mode is desired)

5	VBUS_DET	909K pullup to Type-C VBUS		5-28V VBUS input voltage. VBUS detection determines UFP attachment. One 900K external resistor required between system VBUS and VBUS_DET pin.
6	TXp	Routed to USB3 TX on Ethernet bridge		Host/Device USB SuperSpeed differential Signal TX positive
7	TXn	Routed to USB3 TX on Ethernet bridge		Host/Device USB SuperSpeed differential Signal TX negative
8	VCC33	3.3V with one 100nF capacitor to GND	Recommend adding one 1uF capacitor to GND	3.3-V Power supply
9	RXp	Routed to USB3 RX on Ethernet bridge		Host/Device USB SuperSpeed differential Signal RX positive
10	RXn	Routed to USB3 RX on Ethernet bridge		Host/Device USB SuperSpeed differential Signal RX negative
11	DIR	215K pullup to VCC33		Type-C plug orientation. Open drain output. A pull-up resistor (that is, 200 K) must be installed for proper operation of the device.
12	ENn_MUX	100K pulldown with control signal		Active Low MUX Enable: L - Normal operation, and H - Shutdown.
13, 28	GND	GND		Ground

14	RX1n	Routed to Type-C connector through ESD diode and Common mode choke		Type-C Port - USB SuperSpeed differential Signal RX1 negative
15	RX1p	Routed to Type-C connector through ESD diode and Common mode choke		Type-C Port - USB SuperSpeed differential Signal RX1 positive
16	TX1n	Routed to Type-C connector through 100nF capacitor, ESD diode, and Common mode choke		Type-C Port - USB SuperSpeed differential Signal TX1 negative
17	TX1p	Routed to Type-C connector through 100nF capacitor, ESD diode, and Common mode choke		Type-C Port - USB SuperSpeed differential Signal TX1 positive
18	RX2n	Routed to Type-C connector through ESD diode and Common mode choke		Type-C Port - USB SuperSpeed differential Signal RX2 negative
19	RX2p	Routed to Type-C connector through ESD diode and Common mode choke		Type-C Port - USB SuperSpeed differential Signal RX2 positive
20	TX2n	Routed to Type-C connector through 100nF capacitor, ESD diode, and Common mode choke		Type-C Port - USB SuperSpeed differential Signal TX2 negative
21	TX2p	Routed to Type-C connector through 100nF capacitor, ESD diode, and Common mode choke		Type-C Port - USB SuperSpeed differential Signal TX2 positive
22	ADDR	Pulled to GND, hard to tell whether through 100K resistor or directly routed		Tri-level input pin to indicate I2C address or GPIO mode: H (connect to VDD5) - I2C is enabled and I2C 7-bit address is 0x67. NC - GPIO mode (I2C is disabled) L (connect to GND) - I2C is enabled and I2C 7-bit address is 0x47.

				ADDR pin should be pulled up to VDD5 if high configuration is desired
23	INT_N/OUT3	NC		When used as the INT_N, the pin is an open drain output in I2C control mode and is an active low interrupt signal for indicating changes in I2C registers. When used as OUT3, the pin is in audio accessory detect in GPIO mode: H - no detection, and L - audio accessory connection detected.
24	VCONN_FAULT_N	NC		Open drain output. Asserted low when VCONN overcurrent detected.
25	SDA/OUT1	Routed off-page	Need to add a pullup to your I2C voltage	When I2C is enabled (ADDR pin is high or low), this pin is the I2C communication data signal. When in GPIO mode (ADDR pin is NC), this pin is an open drain output for communicating Type-C current mode detect when the device is in UFP mode: H – Default (900 mA) current mode detected, and L – Medium (1.5 A) or High (3 A) Current Mode detected.
26	SCL/OUT2	Routed off-page	Need to add a pullup to your I2C voltage	When I2C is enabled (ADDR pin is high or low), this pin is the I2C communication clock signal. When in GPIO mode (ADDR pin is NC), this pin is an open drain output for communicating Type-C current mode detect when the device is in UFP mode: H – Default or Medium current mode detected, and L – High current mode detected.
27	ID	NC		Open drain output. Asserted low when CC pin detected device attachment when port is a source (DFP), or dual-role (DRP) acting as source (DFP).

29	ENn_CC	Pulled to GND, hard to tell whether through 100K resistor or directly routed		Enable signal for CC controller. Enable is active low.
30	VDD5	5V with one 100nF capacitor to GND	Recommend adding one 1uF capacitor to GND	5-V Power supply

Comments