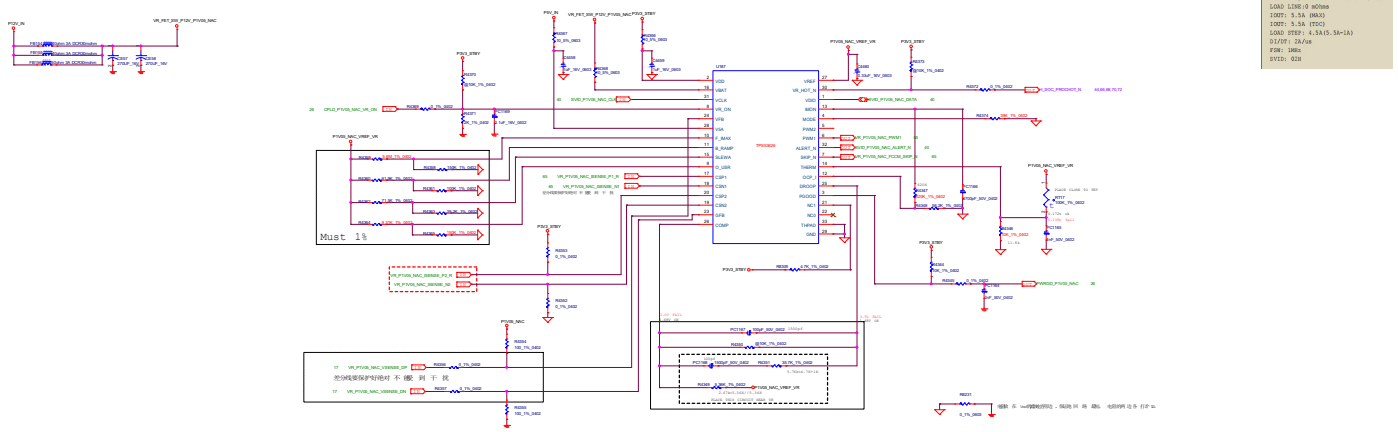
P1V05_NAC_VR



SVID address can be set by the voltage on SLEWA pin.

Table 10. Address Selection

SLEWA VOLTAGE V_{SLEWA} (V)	BASE ADDRESS
$V_{SLEWA} \le 0.30$	0
$0.35 \le V_{SLEWA} \le 0.45$	1
$0.55 \le V_{SLEWA} \le 0.65$	2
$0.75 \le V_{SLEWA} \le 0.85$	3
$0.95 \le V_{SLEWA} \le 1.05$	4
$1.15 \le V_{SLEWA} \le 1.25$	5
$1.35 \le V_{SLEWA} \le 1.45$	6
$1.55 \le V_{SLEWA} \le 1.65$	7

pin15 Vslewa 电压值决定Base Address

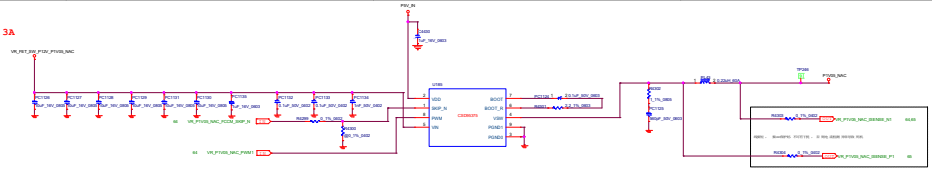
Or if you use if for VCCIO & VMCP, there's default setting for SVID address. You can refer to datasheet for more details.

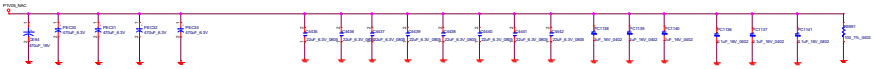
Table 6. R_{MODE} Values and Corresponding Settings

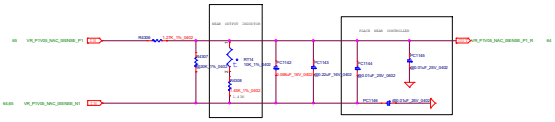
MODE RESISTANCE R_{MODE_nom}	MODE	RAIL	SVID ADDRESS	I_{LIM} (APK)	RAMP (mV)	V_{BOOT} (V)	SLEW RATE (mV/µs)	I_{MAX} (A)	LOWER LEVEL
150	Default	VCCIO	02H	600	60	1.0	10	21	Zero LL
100		VMCP	03H			0.9		10	Zero LL
75		VCCIO	02H			1.0		21	Non-Zero LL
56		VMCP	03H			0.9		10	Non-Zero LL
39	Non-Default Mode Controller programmed through pin-strapping								Zero LL
30									Zero LL
24									Non-Zero LL

P1V05_NAC_VR

3.3A





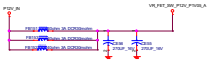


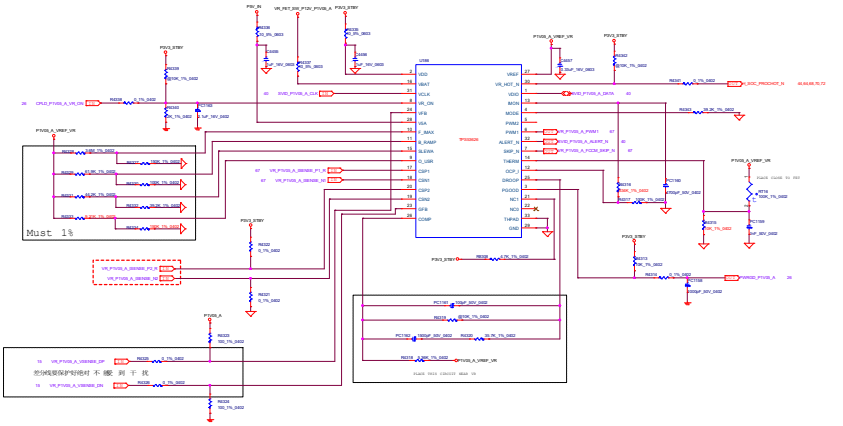
ROUTE ISENSE SIGNALS AS DIFF PAIR
10 MIL WIDTH, 5 MIL SPACING IN A QUIET INTERNAL LAYER

P1V05_A_VR

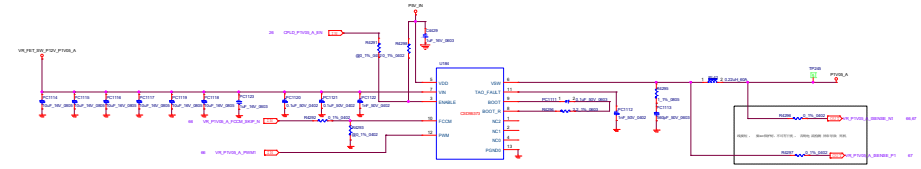
模拟地数字地参考GND板子要分开单点接地

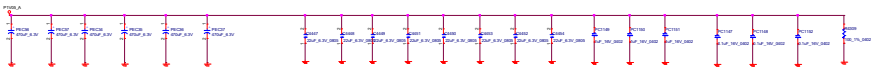
VR SPECS:
VOUT= 1.05V
VBOUT:1.05V
AC & RIPPLE TOL: +/-25mV
TOTAL DC,AC & RIPPLE TOL: +/-30mV
LOAD LINE:0 mOhms
IOUT: 9.7A (MAX)
IOUT: 7.7A (TDC)
LOAD STEP: 6.5A(9.5A-3.0A)
DI/DT: 15A/us
FSW: 1MHz
SVID: 03H

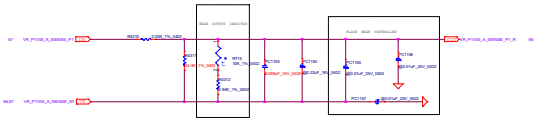




P1V05_A_VR 9.7A



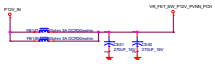


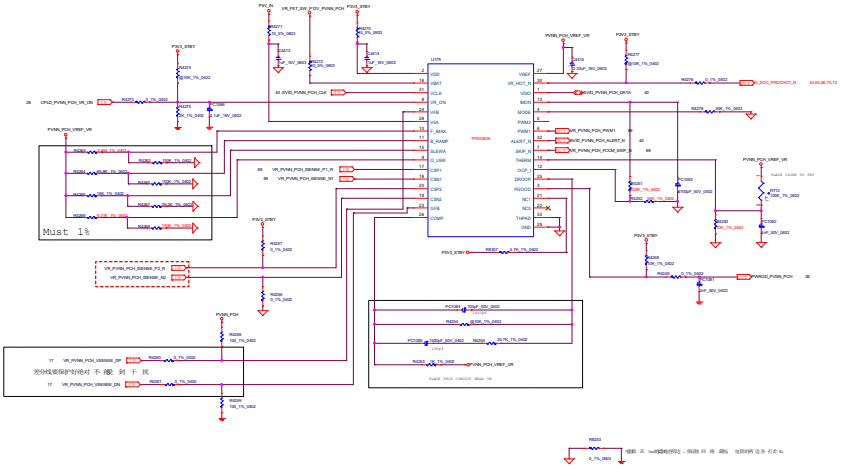


ROUTE ISENSE SIGNALS AS DIFF PAIR
10 MIL WIDTH, 5 MIL SPACING IN A QUIET INTERNAL LAYER

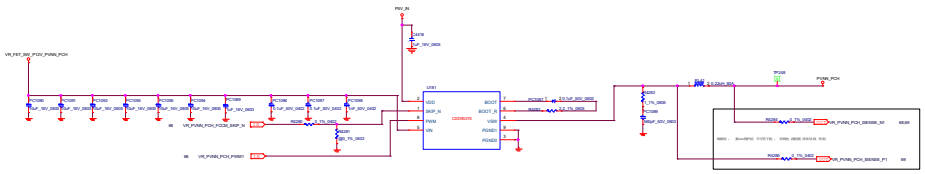
PVNN_PCH_VR

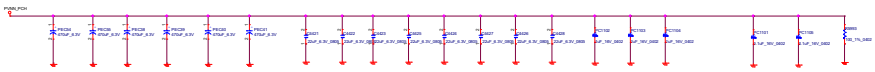
VR SPECS:
VOUT= 0.55V~1.05V
VBOOT:1.0V
AC & RIPPLE TOL: +/-26.6V @ 0.77V
TOTAL DC,AC & RIPPLE TOL: +/-4.5%
LOAD LINE:0 mOhms
IOUT: 5.5A (MAX)
IOUT: 5.2A (TDC)
LOAD STEP:2.4A(5.5A-3.1A)
DI/DT: 20A/us
FSW: 1MHz
SVID: 05H

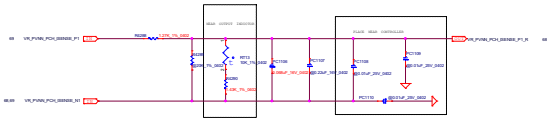




PVNN_PCH_VR 2.5A

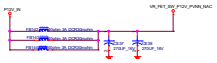




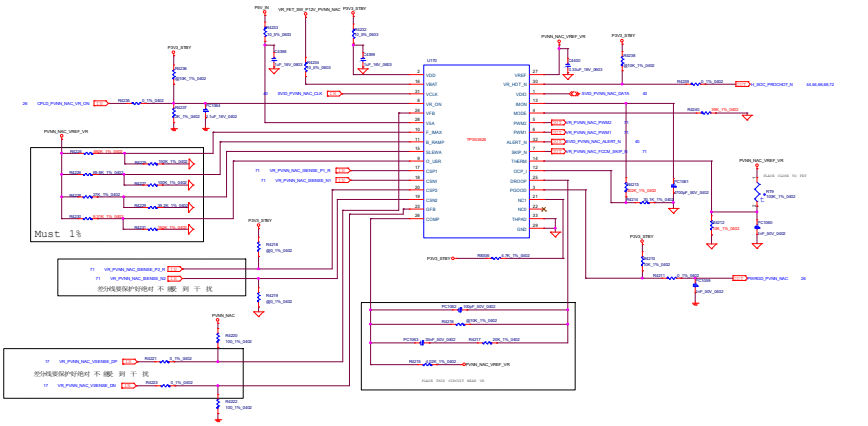


ROUTE ISENSE SIGNALS AS DIFF PAIR
10 MIL WIDTH, 5 MIL SPACING IN A QUIET INTERNAL LAYER

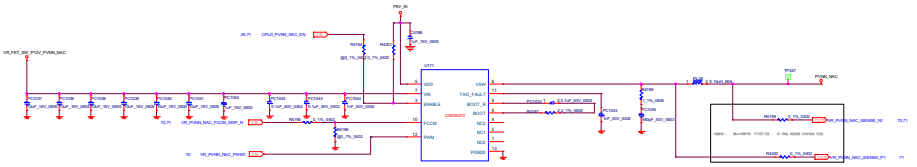
PVNN_NAC_VR

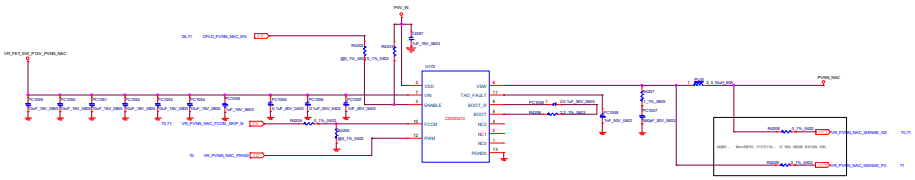


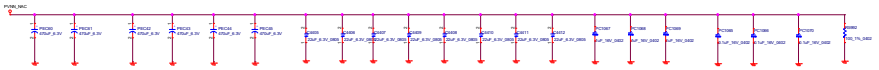
VR SPECS:
VOUT=SVID(0.55-1.05V)
VBOOT:1.0V
AC & RIPPLE TOL: +/-44mV @ 0.8V
TOTAL DC,AC & RIPPLE TOL: +/-6.5%
LOAD LINE:0 mOhms
IOUT: 51A (MAX)
IOUT: 44A (TDC)
LOAD STEP: 20A(51A-31A)
DI/DT: 25A/us
FSW: 1MHz
SVID: 04H

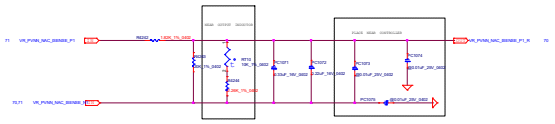


PVNN_NAC_VR 26.4A

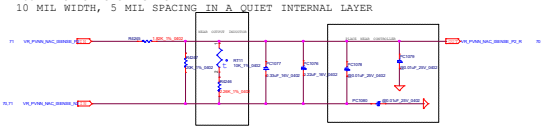






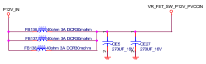


ROUTE ISENSE SIGNALS AS DIFF PAIR
10 MIL WIDTH, 5 MIL SPACING IN A QUIET INTERNAL LAYER



PVCCIN_VR

SVID: 00H
VBOOT:1.8V
VR SPECS:
IOUT: 73A (MAX)
TOTAL DC,AC & RIPPLE TOL: +/-26mV
LOAD LINE:2 mOhms
AC & RIPPLE TOL: NA
DI/DT:180A/uS
IOUT: 38A (TDC)
VOUT=SVID(1.5V-2V) VNOMINAL:1.8V
LOAD STEP: 37A(36A-73A)
FSW: 800KHz



Non-Default Mode
Controller programmed through pin-strapping

调整MODE电阻，NL SLEWA上拉电阻；
20200728

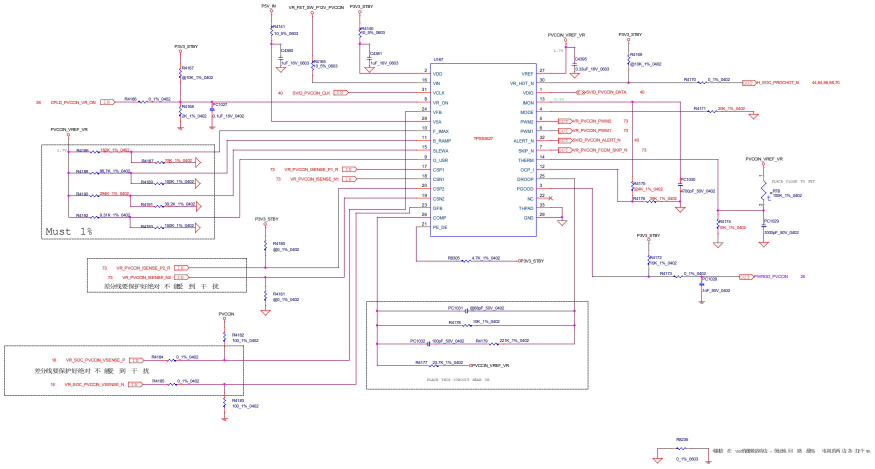
设计需要注意点：

1. mode电阻设置；
2. IMON电阻设置；
3. ISENSE反馈线路设置；
4. 配置电阻设置；
5. 补偿线路设置；
6. SVID走线；

Table 6. Overshoot Reduction (OSR) Function

MODE RESISTOR R_{MODE} (kΩ)	MODE OF OPERATION		
	PS3	LOAD LINE	OSR
20	OFF	Non-Zero	ON
24			OFF
30		Zero	ON
39			OFF
56	ON	Non-Zero	ON
75			OFF
100		Zero	ON
150			OFF

support undershoot reduction(USR) and overshoot reduction (OSR) to provide fast transient response, lowest output capacitance and high efficiency.
Choose a higher ramp value to improve jitter performance if transient response is less of a concern
This value depends on the board layout, output capacitor and individual requirements
Non-Default Mode
Controller programmed through pin-strapping
The current monitor puts out an analog voltage, proportional to the load current, on the IMON pin.
The analog current monitor should be set so that at the maximum processor current (ICC(max)) the IMON voltage should be 1.7 V. This corresponds to a digital SVID output current value of 'FF' in SVID register 15
After PMU_PLTRST_N is de-asserted and the BIOS starts to run, at some point the platform power management requires the VR to report the output currents over the SVID bus. The SoC will read Imon setting from VRs via SVID periodically.



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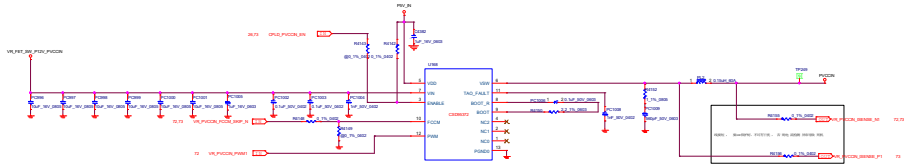
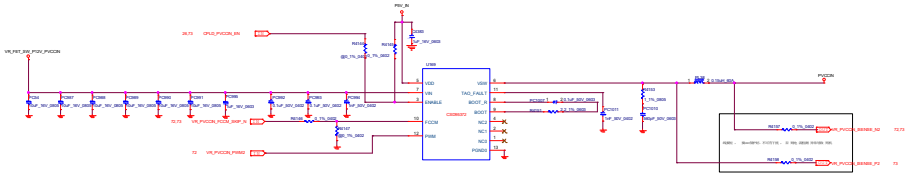
PVCCIN_VR 21A





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