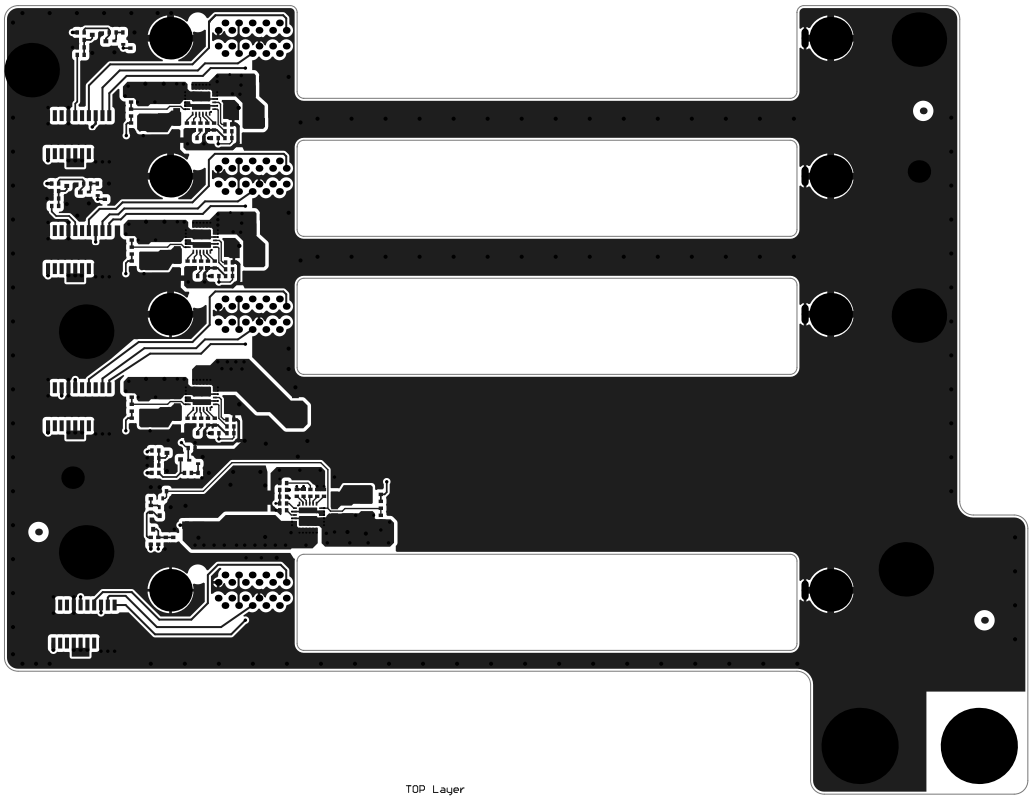
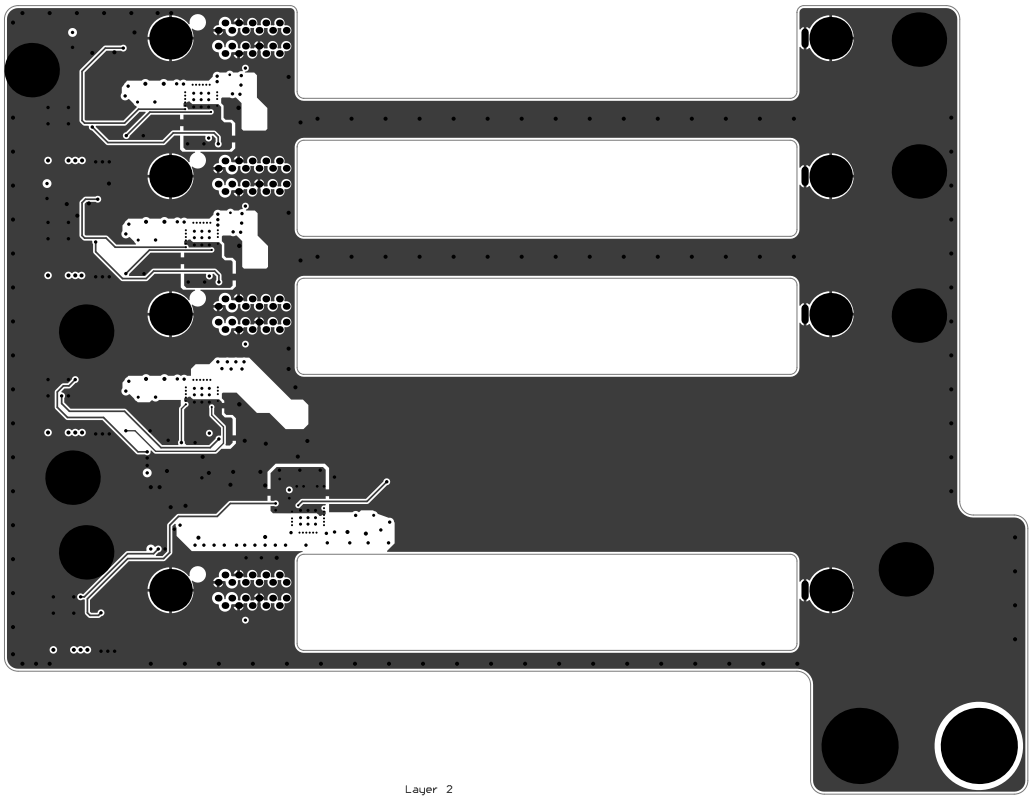
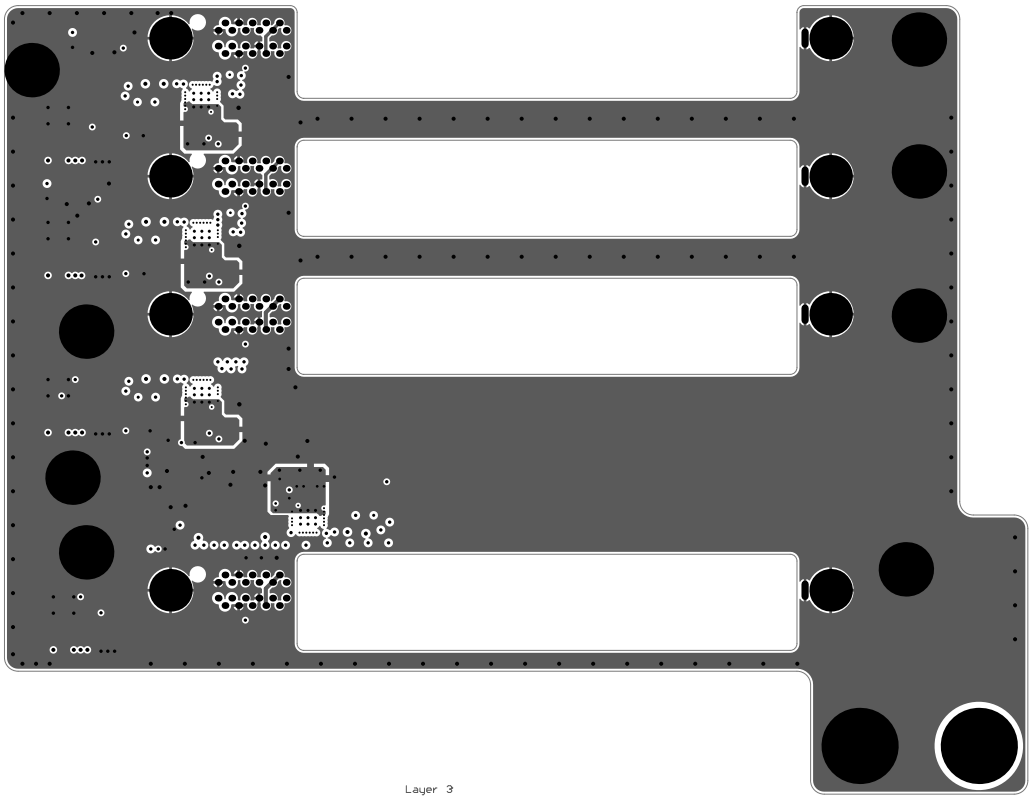


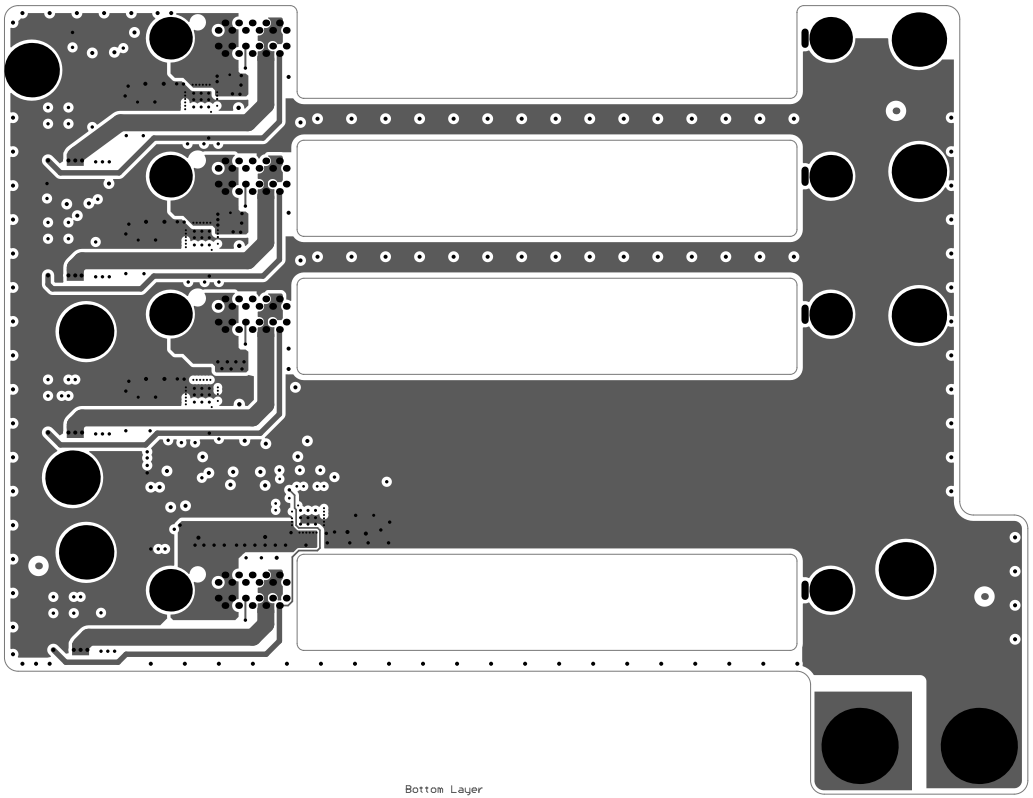
TOP Layer



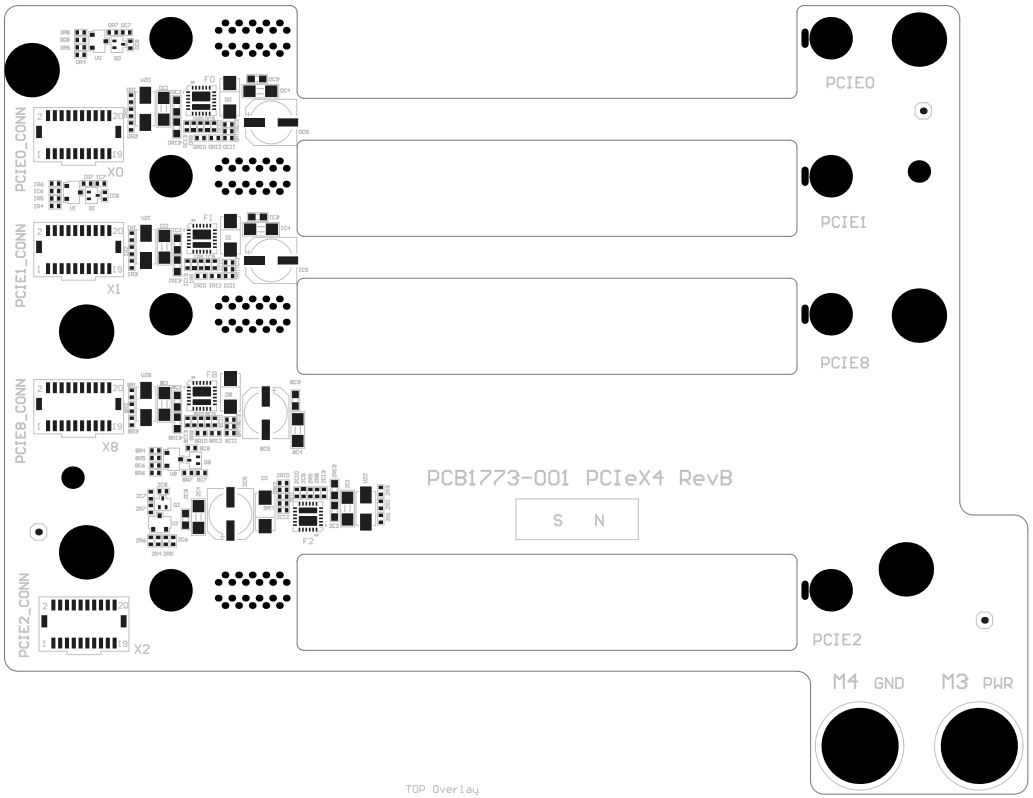
Layer 2



Layer 3

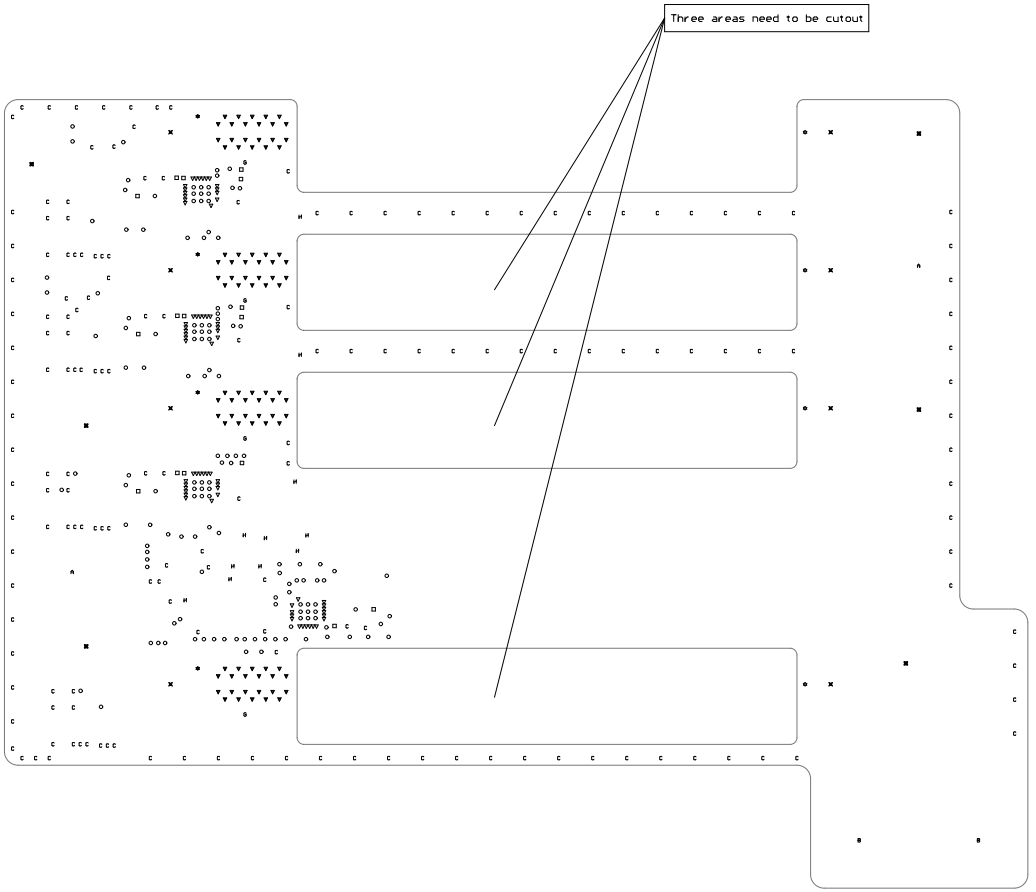


Bottom Layer


PCIE0
PCIE1
PCIE8
PCIE2
M4 GND
M3 PWR
PCIE0_CONN
PCIE1_CONN
PCIE8_CONN
PCIE2_CONN
X0
X1
X8
X2
PCB1773-001 PCIeX4 RevB
S N
TOP Overlay

Symbol	Count	Hole Size	Plated	Hole Type	Drill Layer Pair	Via/Pad	Pad Shape	Template	Description	Hole Tolerance (+)	Hole Tolerance (-)
A	2	3.300mm (129.92mil)	PTH	Round	Top Layer - Bot_PWR	Pad	Rounded	c330h330z800x800(Tol5-5)		0.050mm (1.97mil)	0.050mm (1.97mil)
B	2	5.500mm (216.54mil)	PTH	Round	Top Layer - Bot_PWR	Pad	Rounded	c1120h550(Tol5-5)		0.050mm (1.97mil)	0.050mm (1.97mil)
G	4	0.150mm (5.91mil)	PTH	Round	Top Layer - Bot_PWR	Via	Rounded	v50h15m0mx0(Tol5-5)		0.050mm (1.97mil)	0.050mm (1.97mil)
✡	4	0.660mm (25.98mil)	PTH	Slot	Top Layer - Bot_PWR	Pad	Rounded	r106_286h66_246r100(Tol8-8)		0.075mm (2.95mil)	0.075mm (2.95mil)
✡	4	1.900mm (74.80mil)	NPTH	Round	Top Layer - Bot_PWR	Pad	Rounded	c0hn190m200(Tol5-5)		0.050mm (1.97mil)	0.050mm (1.97mil)
✠	6	3.500mm (137.80mil)	PTH	Round	Top Layer - Bot_PWR	Pad	Rounded	c800h350(Tol5-5)		0.050mm (1.97mil)	0.050mm (1.97mil)
✖	8	4.220mm (166.14mil)	PTH	Round	Top Layer - Bot_PWR	Pad	Rounded	(Mixed)		0.050mm (1.97mil)	0.050mm (1.97mil)
H	11	0.250mm (9.84mil)	PTH	Round	Top Layer - Bot_PWR	Via	Rounded	v60h25m0mx0			
□	16	0.200mm (7.87mil)	PTH	Round	Top Layer - Bot_PWR	Via	Rounded	(Mixed)			
▽	68	0.100mm (3.94mil)	PTH	Round	Top Layer - Bot_PWR	Via	Rounded	v30h10m0mx0(Tol5-5)		0.050mm (1.97mil)	0.050mm (1.97mil)
▼	88	0.720mm (28.35mil)	PTH	Round	Top Layer - Bot_PWR	Pad	Rounded	c100h72(Tol5-5)		0.050mm (1.97mil)	0.050mm (1.97mil)
O	139	0.200mm (7.87mil)	PTH	Round	Top Layer - Bot_PWR	Via	Rounded	(Mixed)		0.050mm (1.97mil)	0.050mm (1.97mil)
C	170	0.250mm (9.84mil)	PTH	Round	Top Layer - Bot_PWR	Via	Rounded	(Mixed)		0.050mm (1.97mil)	0.050mm (1.97mil)
	522 Total										

Slot definitions : Routed Path Length = Calculated from tool start centre position to tool end centre position.
Hole Length = Routed Path Length + Tool Size = Slot length as defined in the PCB layout



Layer	Name	Material	Thickness	Constant	Board Layer Stack
1	Top Overlay				
2	Top Solder	Solder Resist	0.79mil	4	
3	Top Layer	Copper(plated)	2.36mil		
4	Dielectric1	FR-4	7.87mil	4.8	
5	Layer 2	Copper	1.30mil		
6	Dielectric2	FR-4	38.19mil	4.8	
7	Layer 3	Copper	1.30mil		
8	Dielectric3	FR-4	7.87mil	4.8	
9	Bottom Layer	Copper(plated)	2.36mil		
10	Bottom Solder	Solder Resist	0.79mil	4	
11	Bottom Overlay				

1. Fabricate and test per IPC-6012, Class 2.
2. Finish: ENIG.
3. There are to be no non-functional pads on all internal signal layers.
4. All dimensions on the drill drawing layer are in MM.
5. General Hole Tolerance Drilled holes +/- 1mil and Finished holes +/- 2mil
6. Soldermask shall be liquid photoimageable. Blue soldermask under white silkscreen.
7. The thickness of board is 1.6mm+/-10% .
8. The impedance is 50ohm +/-10% for 0.295mm width on Top layer.
9. Add year/weak in blank location and SN place the specified position.
10. High-voltage insulation test(5 pcs power)
    Test conditions: voltage/current -1500V/0.1mA, the Creepage Voltage 500V/S, 1500V is maintained for 3 to 5 seconds.