1. We need to understand when does the DRA75 will release its Reset signal?

Our understanding is, after initial power up sequence, PMIC will de-assert its reset out signal(RESET\_OUT) and is given as input to the “porz” pin of DRA75 processor as shown in below figure. Hence DRA75 will release its reset out based on porz input.

Also please clarify what is the condition of “NRESWARM” pin of PMIC during initial power up sequence, as this warm reset signal is out from “rstoutn” pin of DRA75 processor.



1. DRA75 datasheet : Page #180 has below power up sequence.

Note 14 say there is delay of 2ms delay between resetn and rstout of DRA75 processor.





From above diagram, DRA75 will release its reset aftet 2ms delay of resetn input. Which means DRA75 will will assert LOW to the PMIC for warm reset? Please clarify.?