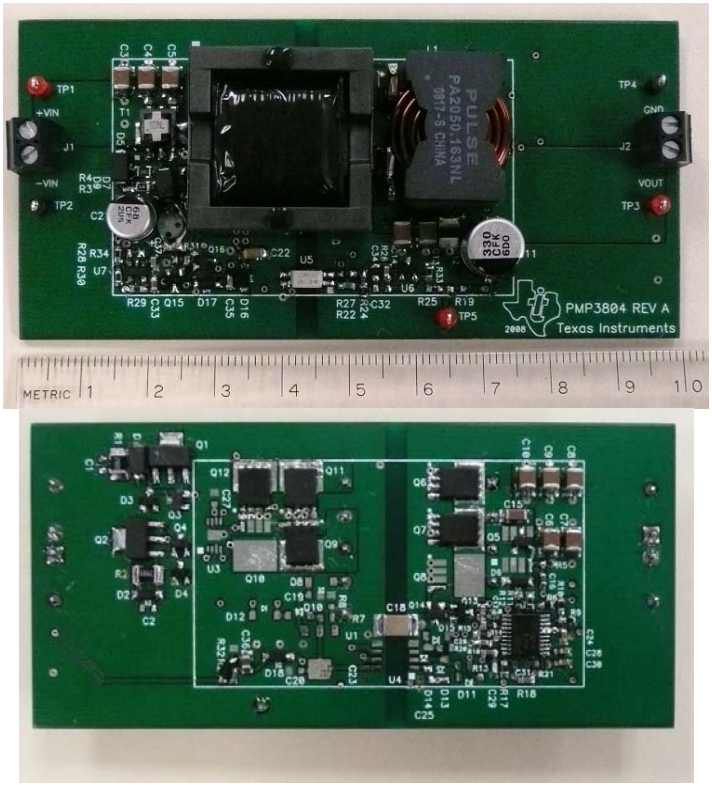
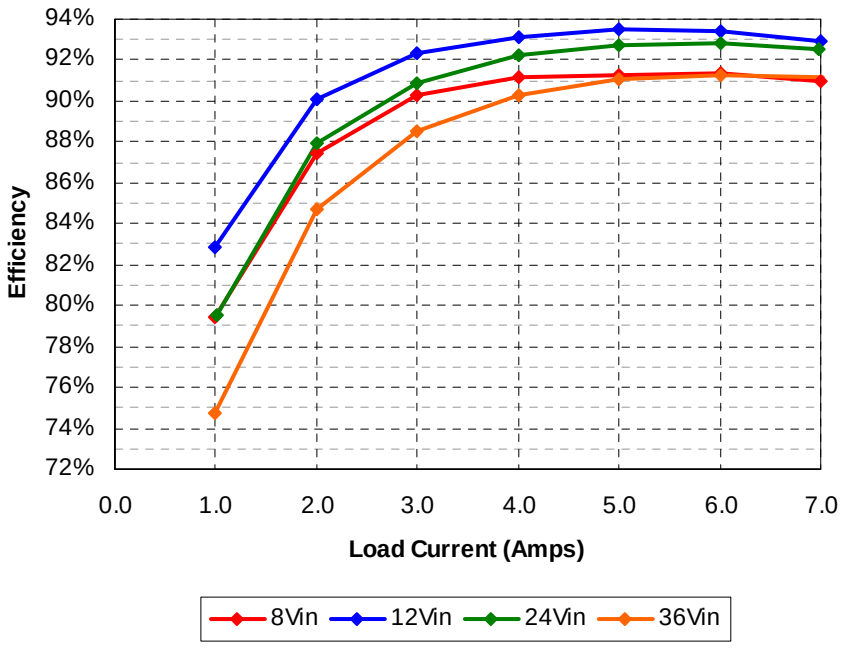
1 Photo

The photograph below shows the top view and bottom view of the PMP5123 Rev A demo board. The circuit is built on a PMP3804 Rev A PWB.



2 Efficiency

The efficiency data is shown in the tables and graph below.

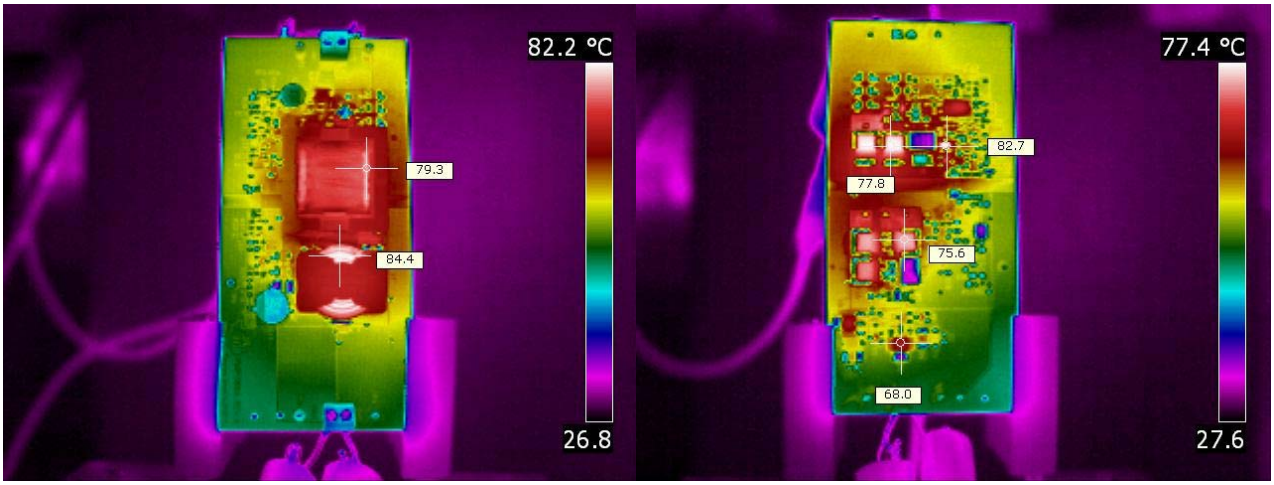


Iout	Vout	Vin	Iin	Pout	Losses	Efficiency	Iout	Vout	Vin	Iin	Pout	Losses	Efficiency
0.000	12.13	8.00	0.381	0.00	3.048	0.0%	0.000	12.13	12.00	0.212	0.00	2.544	0.0%
1.000	12.13	8.00	1.908	12.13	3.134	79.5%	0.994	12.13	12.00	1.212	12.06	2.487	82.9%
2.002	12.12	8.00	3.467	24.26	3.472	87.5%	1.996	12.13	12.00	2.240	24.21	2.669	90.1%
3.002	12.12	8.00	5.04	36.38	3.936	90.2%	2.998	12.13	12.00	3.281	36.37	3.006	92.4%
4.001	12.12	8.00	6.65	48.49	4.708	91.2%	4.003	12.12	12.00	4.34	48.52	3.564	93.2%
5.00	12.12	8.01	8.29	60.61	5.791	91.3%	5.00	12.12	12.00	5.40	60.60	4.200	93.5%
6.00	12.12	7.99	9.97	72.76	6.904	91.3%	6.00	12.12	12.00	6.49	72.72	5.160	93.4%
7.00	12.12	8.01	11.64	84.84	8.396	91.0%	7.00	12.12	12.00	7.61	84.84	6.480	92.9%
Iout	Vout	Vin	Iin	Pout	Losses	Efficiency	Iout	Vout	Vin	Iin	Pout	Losses	Efficiency
0.000	12.13	24.01	0.131	0.00	3.145	0.0%	0.000	12.14	36.01	0.110	0.00	3.961	0.0%
1.008	12.13	23.99	0.641	12.23	3.151	79.5%	0.999	12.14	36.00	0.451	12.13	4.108	74.7%
2.002	12.13	23.99	1.151	24.28	3.328	87.9%	2.000	12.13	35.99	0.796	24.26	4.388	84.7%
2.998	12.13	23.93	1.672	36.37	3.645	90.9%	3.001	12.13	36.02	1.142	36.40	4.733	88.5%
4.002	12.13	23.99	2.194	48.54	4.090	92.2%	3.999	12.13	36.01	1.492	48.51	5.219	90.3%
5.00	12.13	24.00	2.726	60.65	4.774	92.7%	5.00	12.13	35.97	1.851	60.65	5.930	91.1%
6.00	12.13	24.00	3.267	72.80	5.604	92.9%	6.00	12.13	35.99	2.215	72.78	6.938	91.3%
6.99	12.12	24.00	3.813	84.72	6.793	92.6%	7.01	12.13	36.02	2.589	85.03	8.224	91.2%

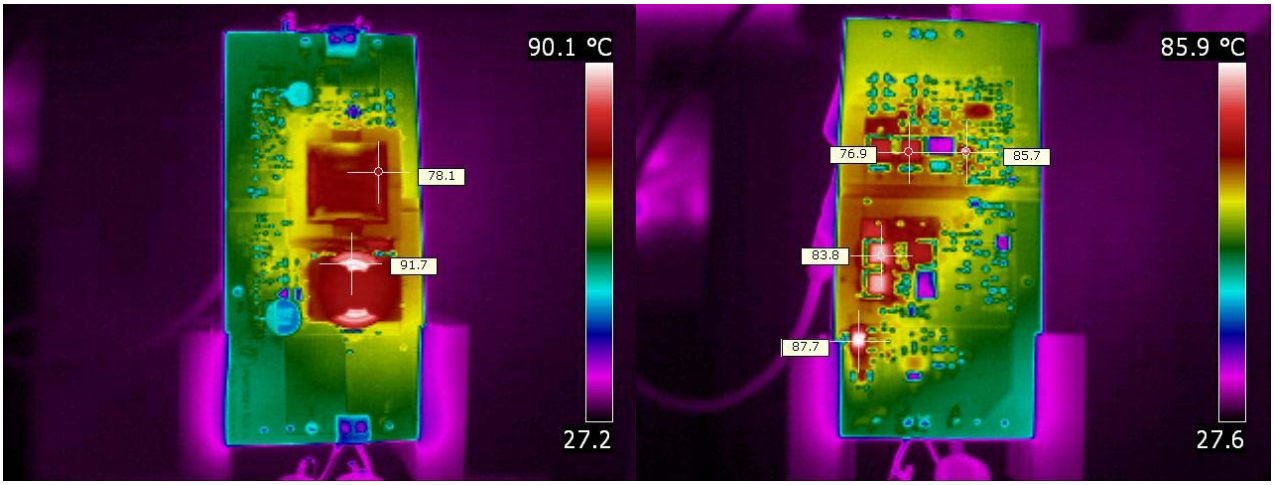
3 Thermal Images

The thermal images below show a top view (left) and bottom view (right) of the board. The ambient temperature was 26ºC with no forced air flow. The output was loaded with 7A.

3.1 12V Input

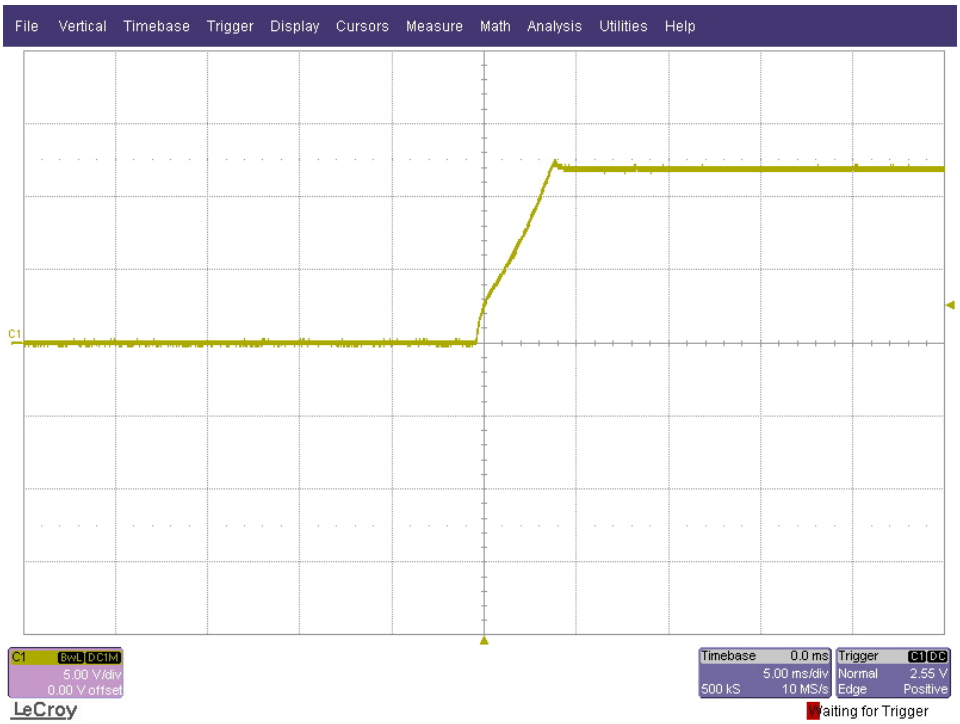


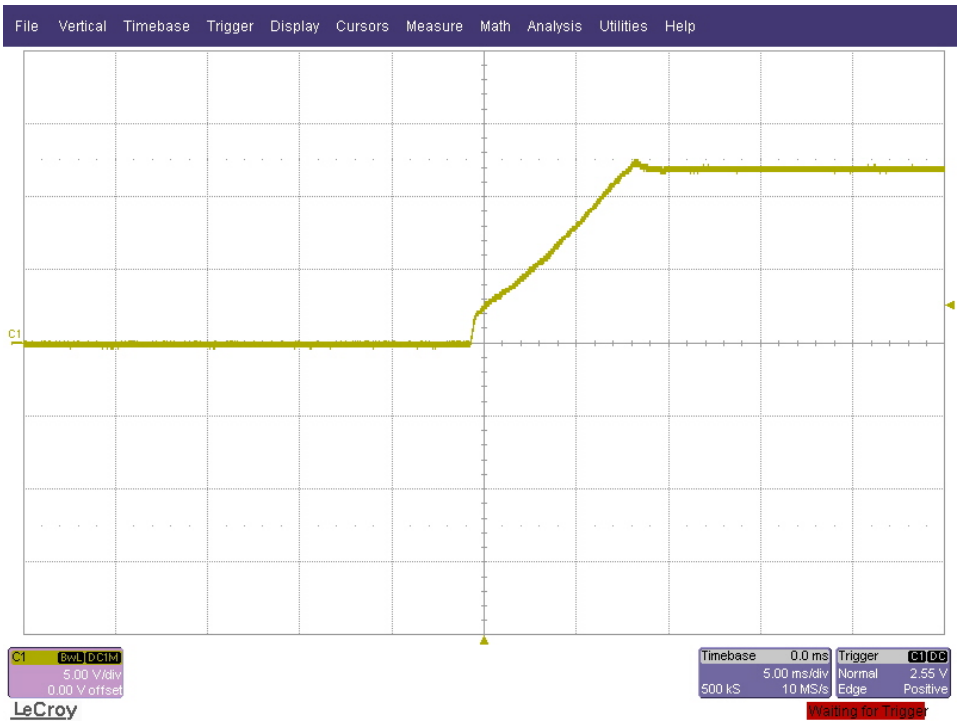
3.2 24V Input



4 Startup

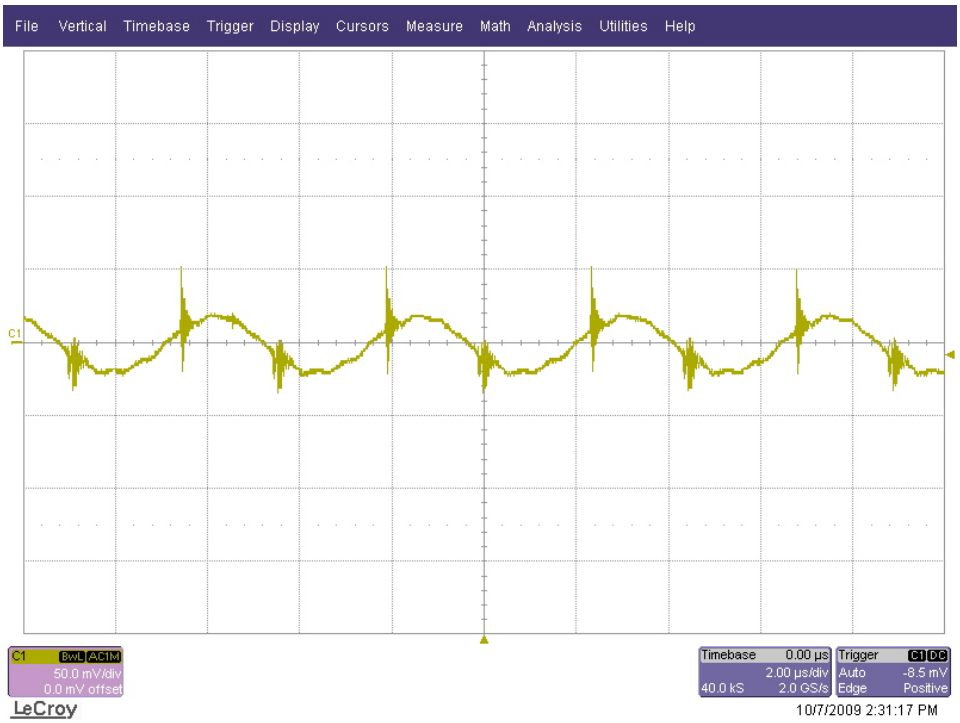
The output voltage at startup is shown in the images below. The input was 12VDC. For the top image, the output was unloaded. For the bottom image, the output was loaded with 7A.





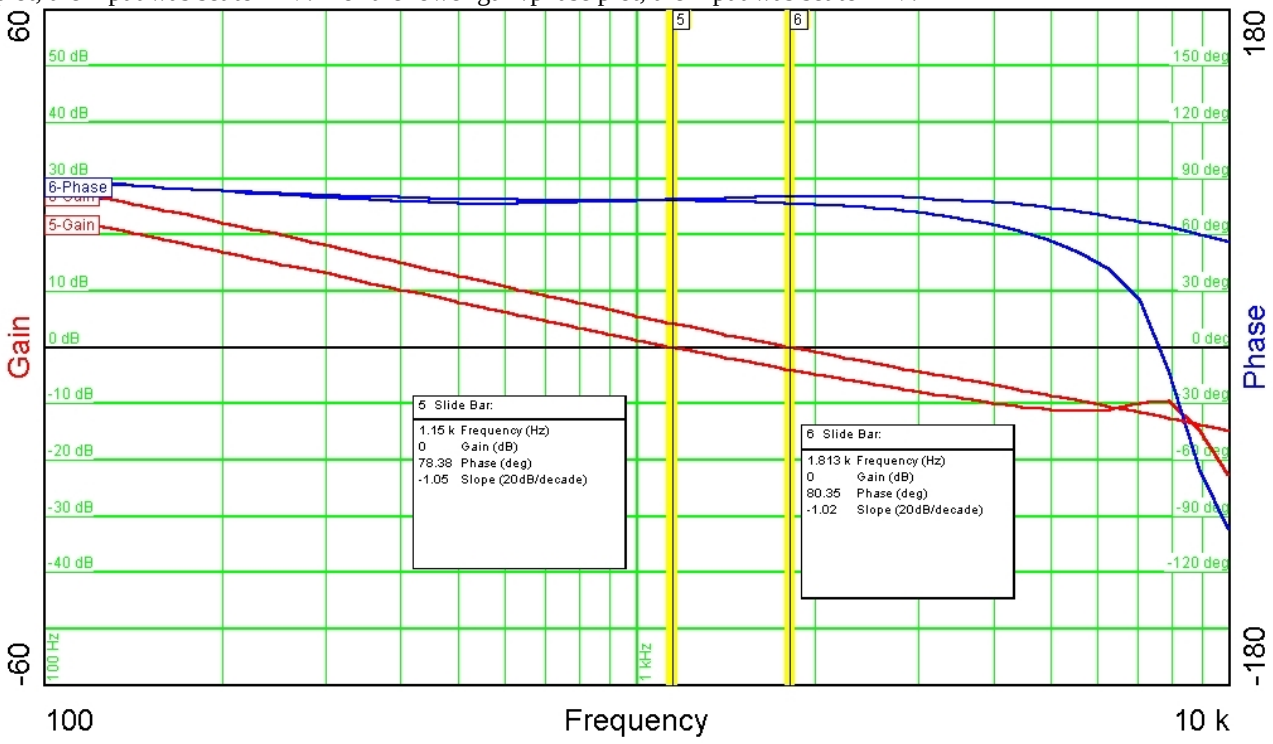
5 Output Ripple Voltage

The output ripple voltage during full load operation (7A load) is shown in the plot below. The input voltage was set to 12VDC.



6 Loop Response

The image below shows the loop response of the converter. The output was loaded with 7A. For the upper gain/phase plot, the input was set to 24V. For the lower gain/phase plot, the input was set to 12V.



7 Load Transients

The image below shows the response to a 3A to 6A load transient. The input voltage was set to 12VDC.
Channel 1: Vout (ac coupled) 500mV/div Channel 4: Iout 2A/div

8 Switching Waveforms

The images below show the drain-to-source voltage waveforms on the switching MOSFETs. The output was loaded with 7A. For the top image, the input was set to 36V. For the bottom image, the input was set to 8V.

Channel 1: Q6 and Q7 Vds Channel 2: Q11 and Q12 Vds
Channel 3: Q9 Vds