



4/15/2022

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DESIGN CONSIDERATIONS

DESIGN NOTE:  
Example text for informational  
design notes.


DESIGN NOTE:  
Example text for critical  
design notes.

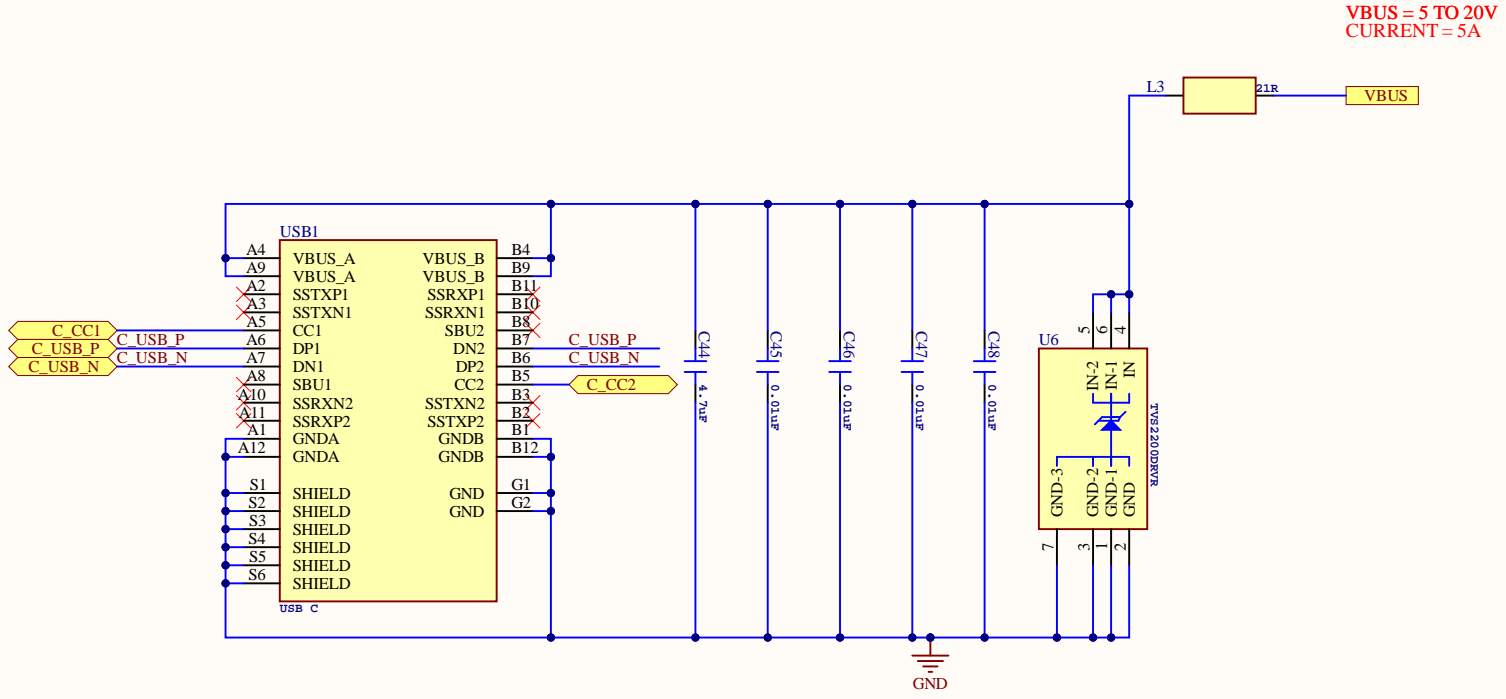
DESIGN NOTE:  
Example text for cautionary  
design notes.


LAYOUT NOTE:  
Example text for critical  
layout guidelines.

<b>Title:</b>		<b>Designer:</b>		
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# BLOCK DIAGRAM

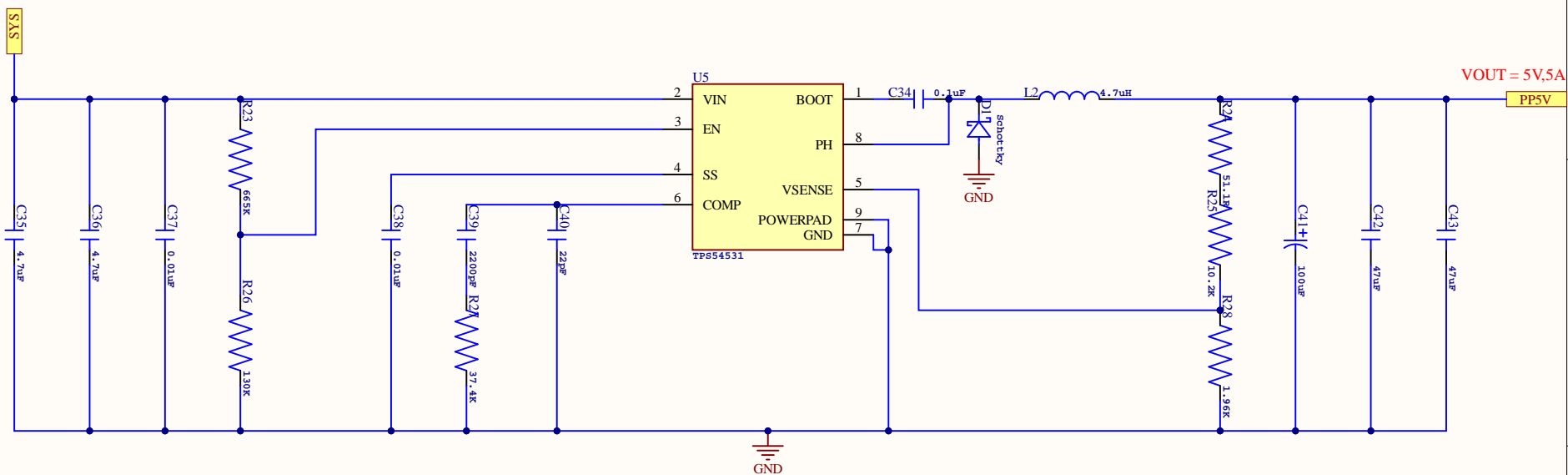
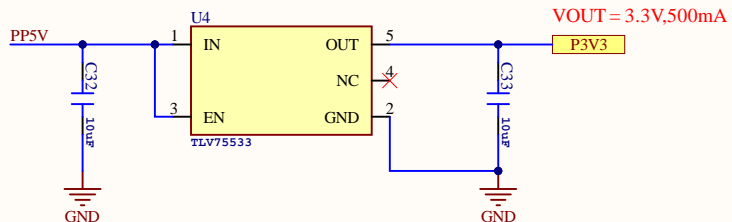
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<b>Address:</b>		Brainchild Engineering	



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**Title:**

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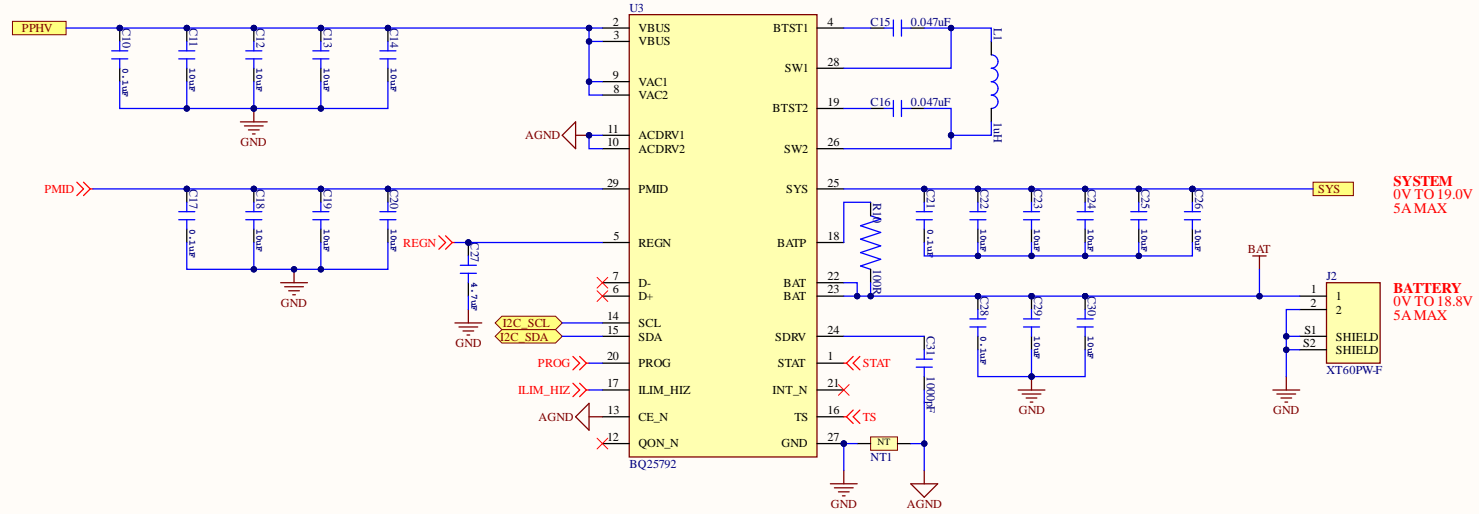
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**Address:**

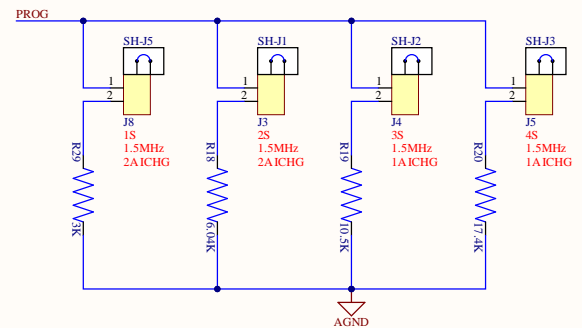
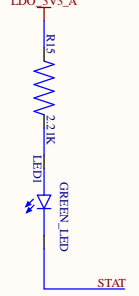
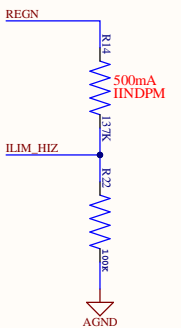
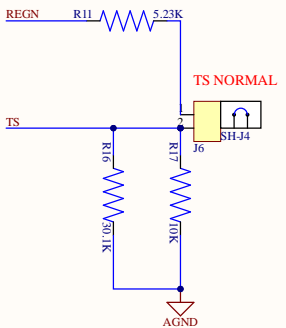
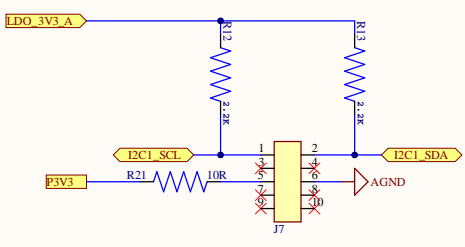
**Designer:**



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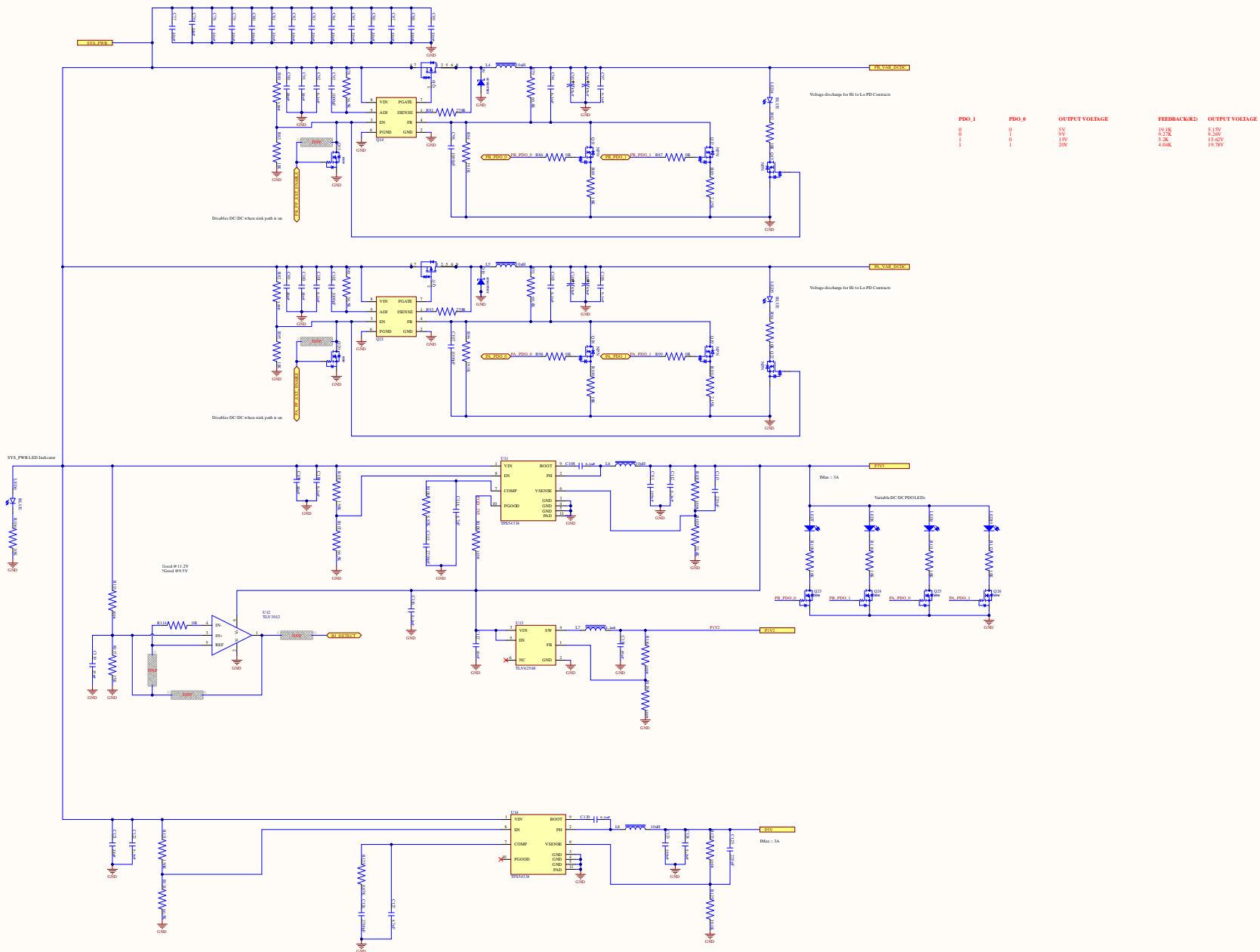
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 TS >> TS  
 PROG >> PROG  
 ILIM\_HIZ >> ILIM\_HIZ  
 REGN >> REGN



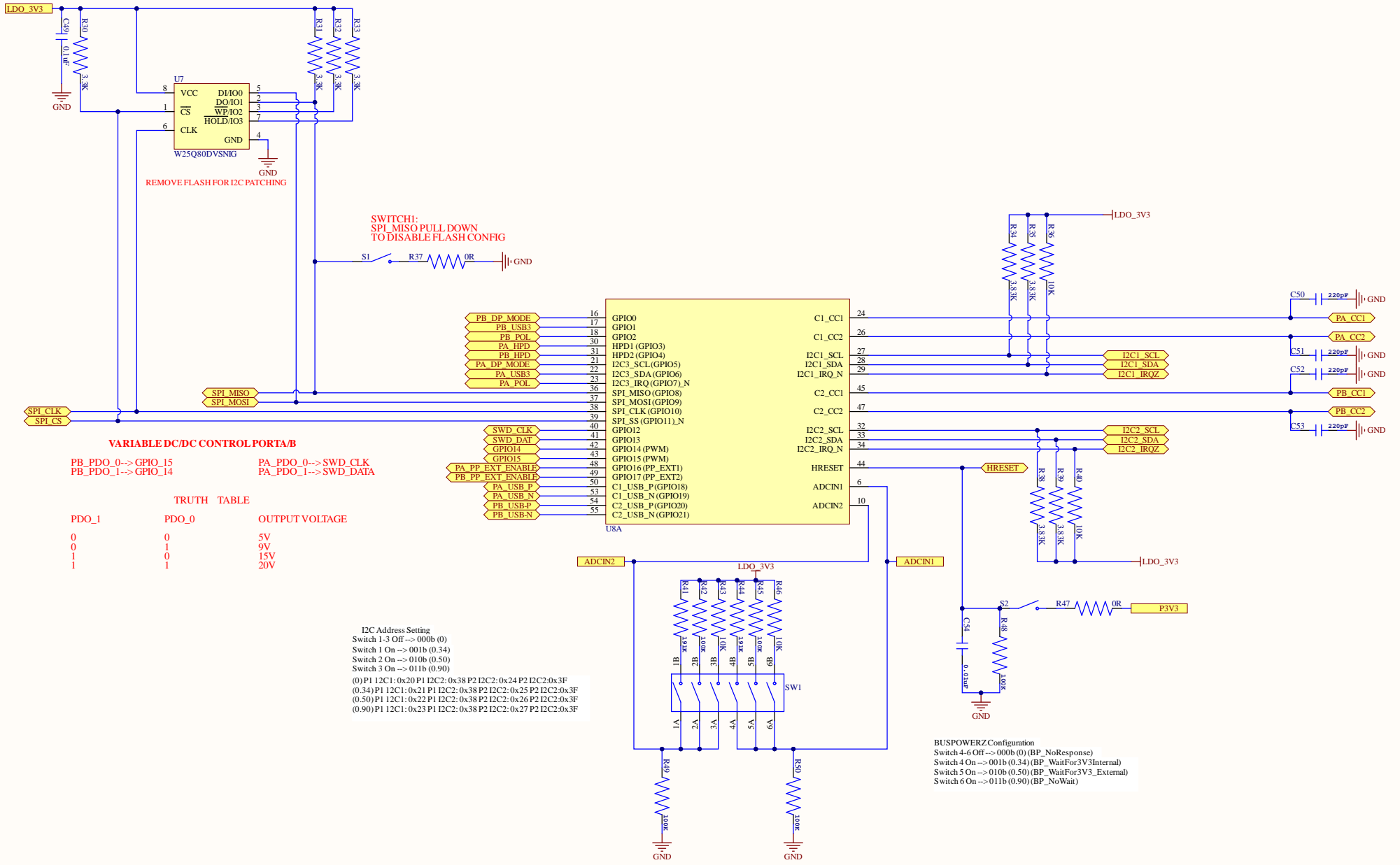
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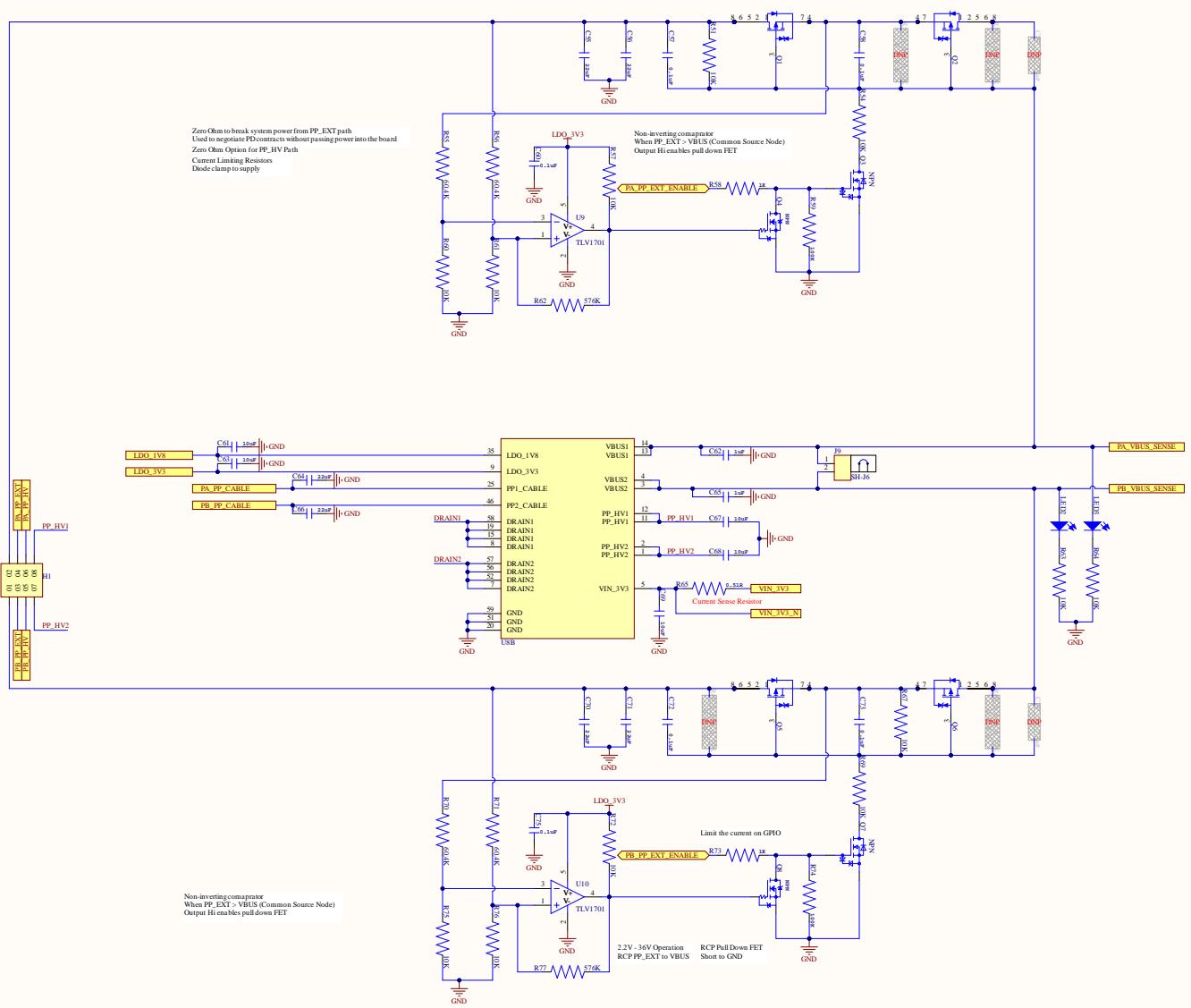
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P0.1	P0.8	OUTPUT VOLTAGE	FEEDBACK/2	OUTPUT VOLTAGE
0	0	15V	5.12V	15.18V
1	1	25V	8.25V	25.25V
		15V	5.25V	15.00V
		25V	8.00V	25.00V



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Zero Ohm to break system power from PP\_EXT path  
Used to negotiate PD contracts without passing power into the board  
Zero Ohm Option for PP\_HV Path  
Current Limiting Resistors  
Diode clamp to supply

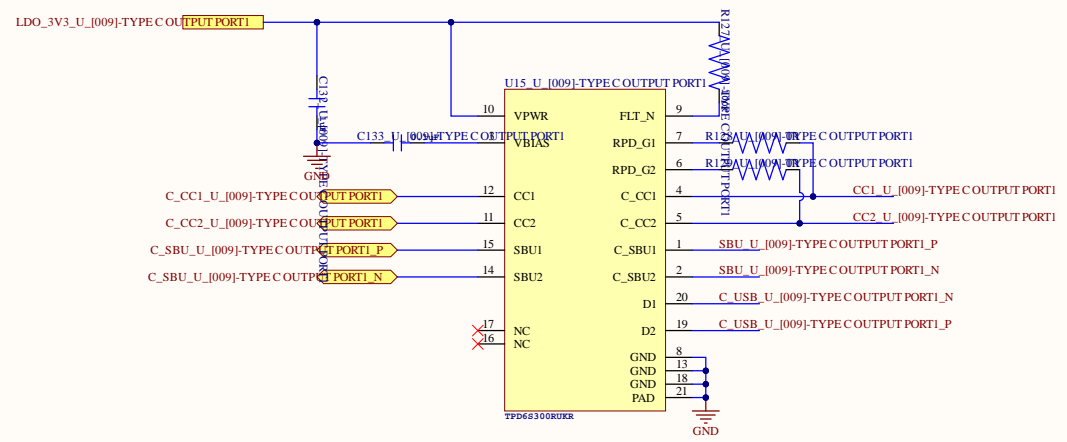
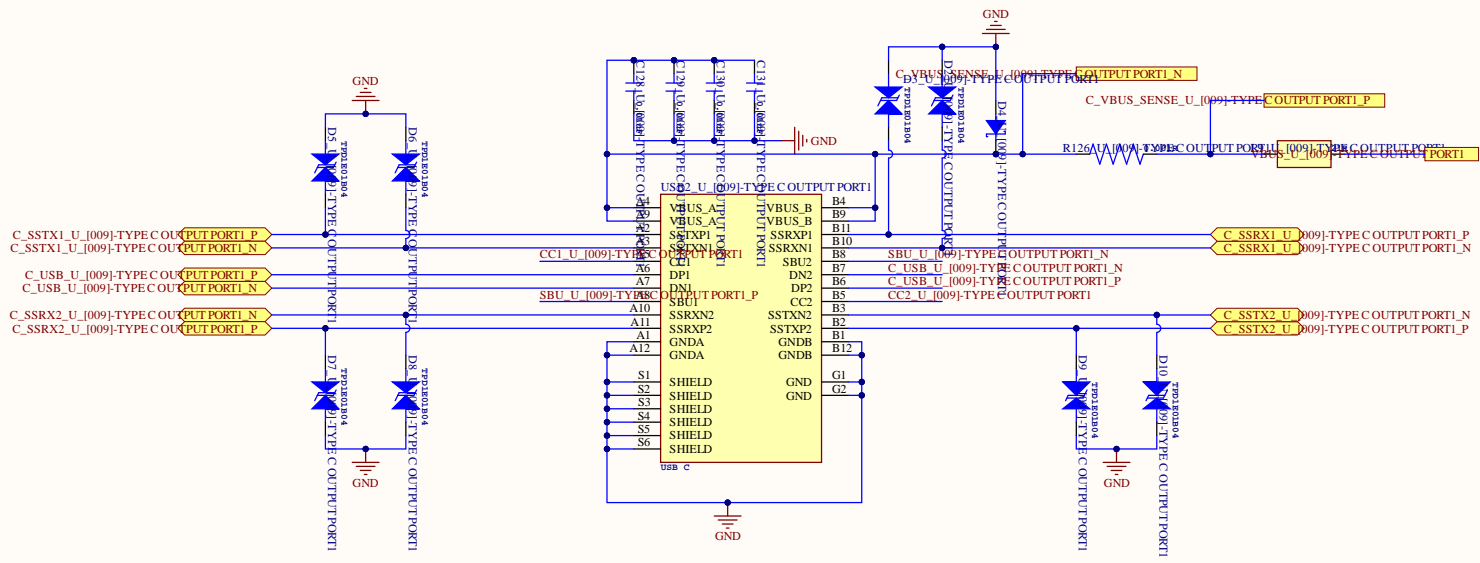
Non-inverting comparator  
When PP\_EXT > VBUS (Common Source Node)  
Output Hi enables pull down FET

Non-inverting comparator  
When PP\_EXT > VBUS (Common Source Node)  
Output Hi enables pull down FET

Limit the current on GPIO  
RCP Pull Down FET  
Short to GND

2.2V - 36V Operation  
RCP PP\_EXT to VBUS

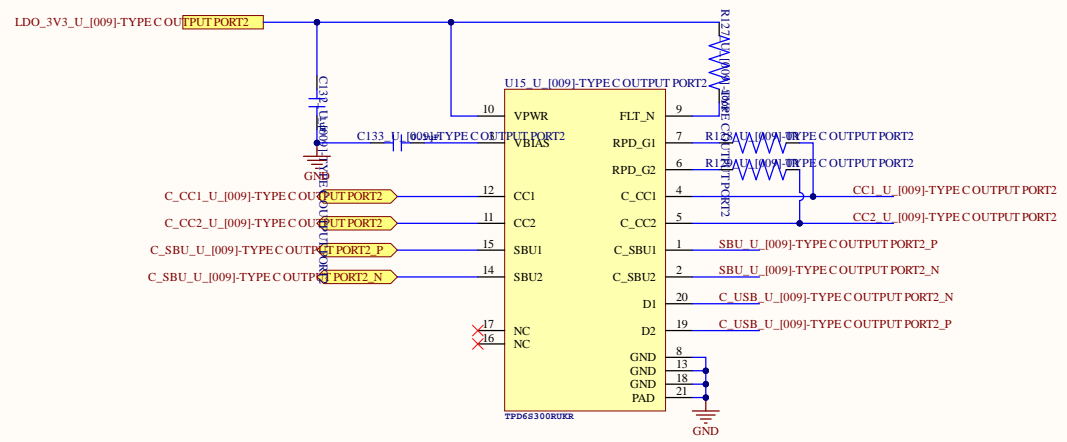
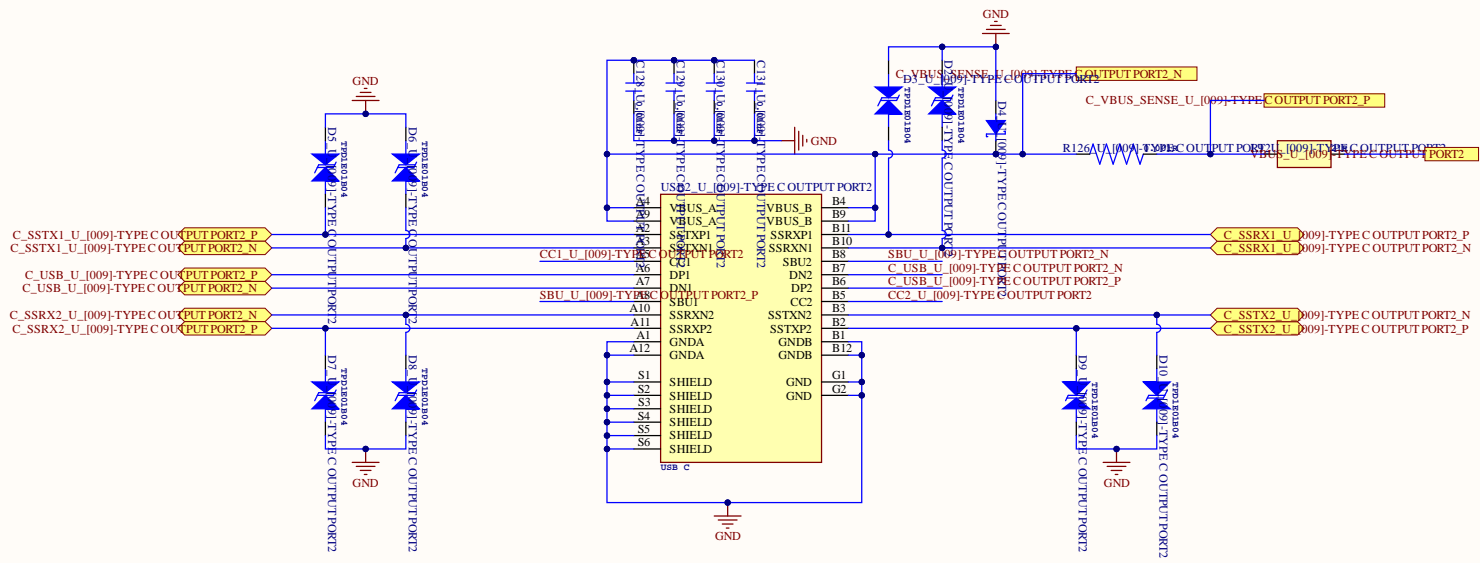
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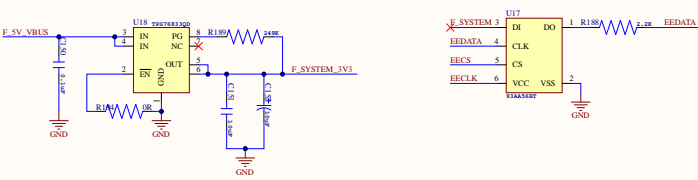
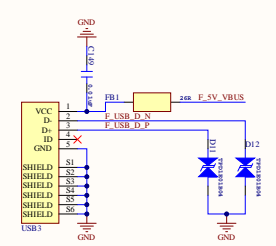
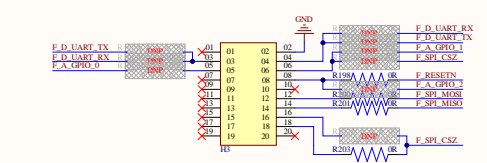
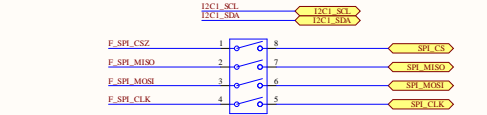
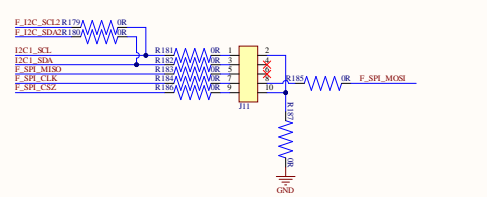
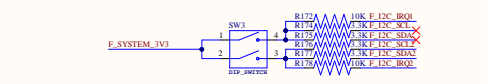
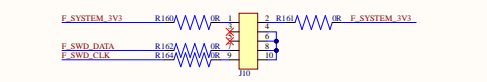
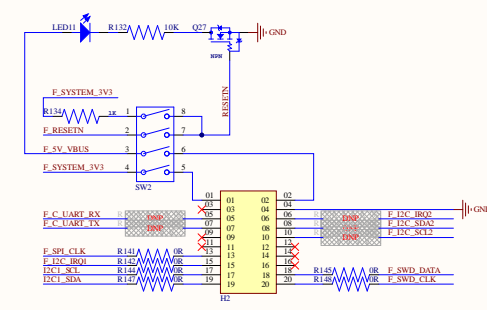
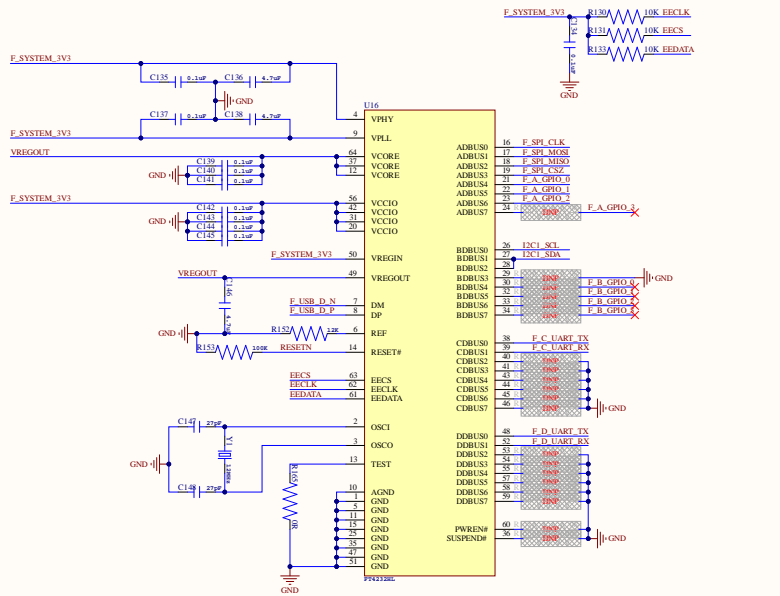


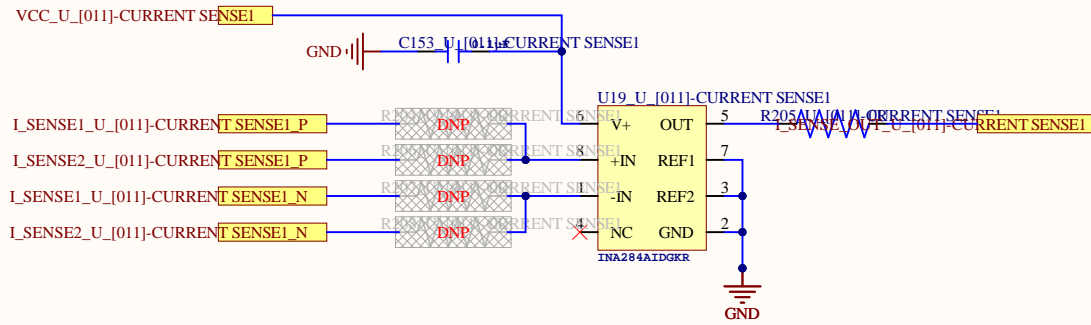
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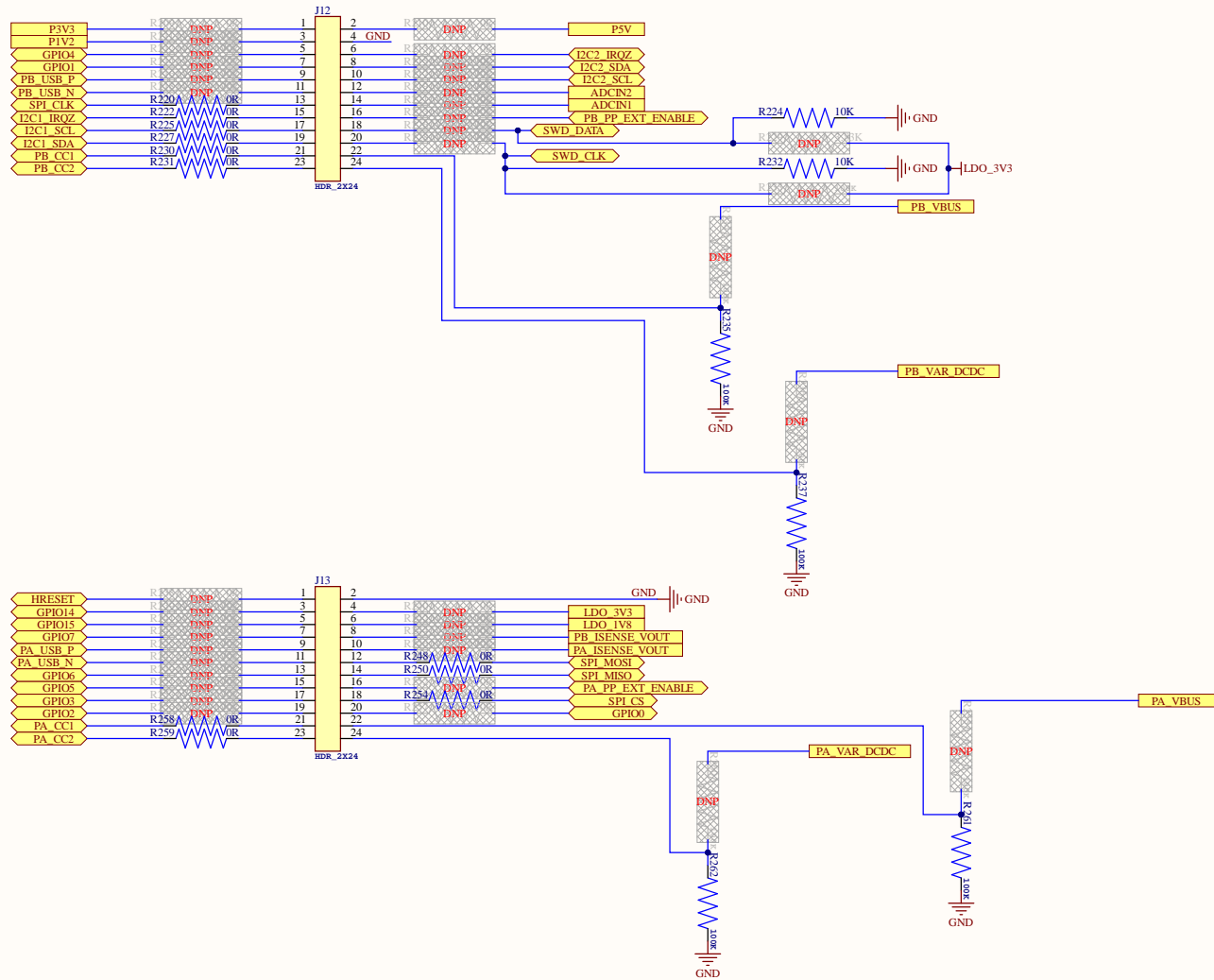







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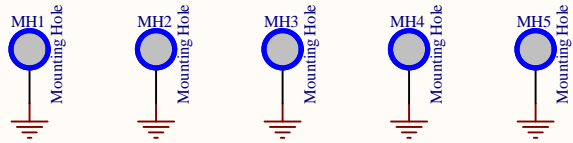





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# BOARD MECHANICS

## MOUNTING HOLES



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